

Micro processor.

Unit - 1 Introduction.

- Introduction to microprocessor (MP)

↳ History

↳ Definition of MP

↳ Evolution of MP

↳ Types of MP

↳ Archi of 8085 MP & operation

Functional

- Archi of 8085 MP & operation
- Functional block diagrams of 8085
- Pin diagram of 8085
- Memory interfacing

Ramesh Gaonkar - 1 , 3 May 2009

Unit - 2 :- Basic concepts of Interfacing with
I/O devices, interfacing with I/P devices
I/O mapped interfacing.

Memory mapped I/O interfacing.

Operations → Data transfer, Arithmetic operation,
logical operations. Branch operation, programming
techniques.

Unit - 3 : Instruction set

Data transfer instruction - 8 & 16 bit instruction.

Arithmetic operation instruction related to
memory.

Logical operation - Rotate, compare, counter etc

Hexa decimal counter - 0-15

Program for generating pulse wave form, debugging

Kreator

Stack subroutine

8085 Interrupts $\xleftarrow{\text{hardware}}$ $\xrightarrow{\text{software}}$ vectors, non-vectors

Unit - 4 - Programs - ***

1. BCD to Binary conversion
2. Binary to BCD conversion
3. BCD to seven segment code
4. Binary to ASCII
5. ASCII to Binary
6. BCD addition
7. BCD subtraction
8. BCD multiplication
9. BCD subtraction with carry.

Unit - 5

8255 programmable peripheral interface.

DMA controller 8237

Interrupt controller - Programmable

8254 programmable counter

Unit - 1Introduction to uP.

History

Transistor - 1947. 1971 - Microprocessor

IC - 1959

Microcontroller - 1976.

In 1947, transistors were invented by William H. Shockley.

In 1959, IC's were developed.

Integrated Ckt (IC) - It is a device in which no. of transistors & components can be fabricated on a single chip (silicon wafer).

Moore's law.

1965 - Birth of Moore's law

"Component density (no. of transistors on a single chip chip of IC) would double in every 18 months"

1971 - First Microprocessor (uP) (development)
↳ 4004 → used in prog. calculator.

Evolution of MP.

1971 - development of first uP.

i.e. Intel 4004

↓ further.

Intel 8008

↓ later

Intel 8080

8085

8086

Technology

Technology	No. of transistors on single chip
SSI	→ 10 - 100
MSI	→ 1100 - 1000
LSI	→ 1000 - 20,000
VLSI	→ 20,000 - 50,000
ULSI	→ > 50,000

Min size of transistor :

- A Q1. When & where transistors were invented
- S Q2. What is an IC?
- Q Q3. When was first Microprocessor introduced?
- U Q4. What is Moore law?
- E Q5. What is the currently min. size of transistor.

Micro controllers

1976 - First micro controller

⇒ comes under Generation of Micro processor.
evolution of MP.

First generation - 1971 to 1973

e.g. 4004 & 8008

Second generation - 1973 to 1978

- Based on N-MOS
- e.g. 8080, M6800, Zilog Z80
Motorola
- consist of 8 bit MP

Third generation - 1979 to 1980

Speed was 4 times better than 2nd gen.

e.g. ^{Intel} 8086, 80186, 80286, 386

Krator

It is based on C-MOS technology.

Fourth generation - 1981 - 1995

32 bit UP comes under this gen
eg - Intel 80386, M 68020, Intel 80486.
Based on N-MOS

Fifth generation - 1995 to till now.

64 bit UP.

Diagrams

25/1

MPU CPU

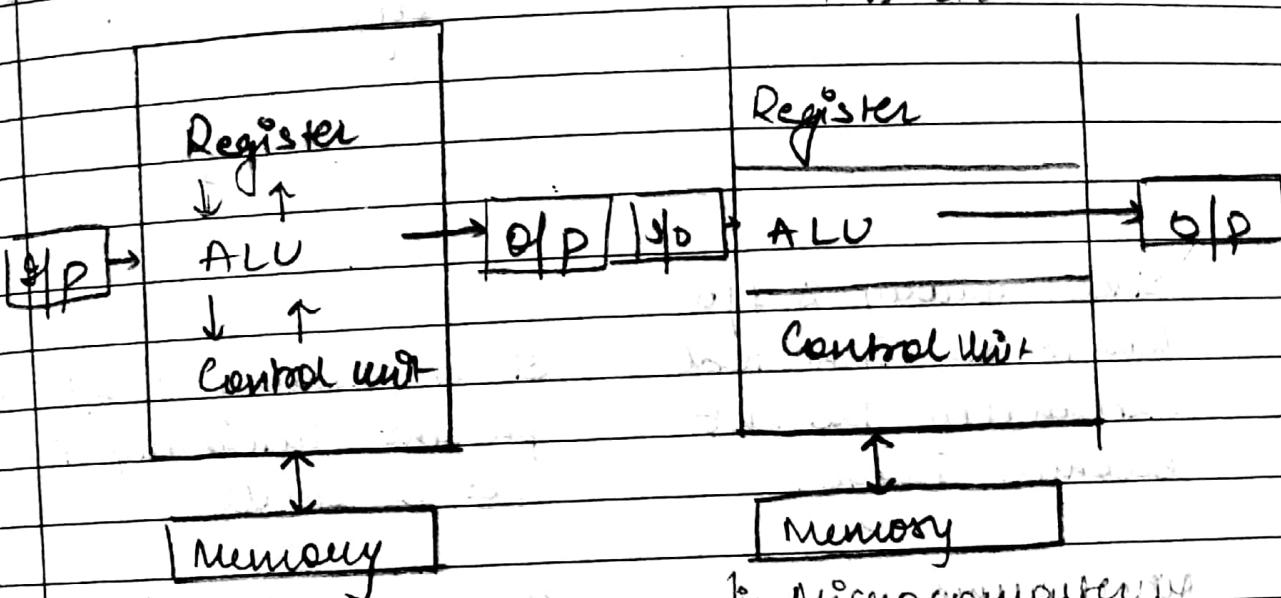


fig - CPU

fig - Micro computer

MPU	ROM
Timer counter	RAM
Serial I/O	I/O port

fig - Micro controller

Diff. b/w

Microprocessor

It is a CPU on a single chip

heart of comp. sys.

Fig - 2

back page

Since memory & I/O has to be connected externally the ckt becomes large.

Since memory & I/O components are all external, each instruction will need ext. operation hence slower.

Hence Slower.

Microprocessors are based on von neumann architecture where program & data are stored in same memory module.

Microcontroller

It is a computer on a single chip.

It is the heart of embedded sys

fig - 3

back page

Since memory & I/O are present internally the ckt is small

Since components are inter connected most of the operations internal first.

Hence speed is faster.

Microcontroller are based on Harvard architecture where program & data memory are separate.

eg -

Robot

Work. Eg - Washing machine
toys

$$(23)x = (43)y \quad \downarrow \quad (23)y = (15)_{10}$$

$$23 = 2xy' + 3y$$

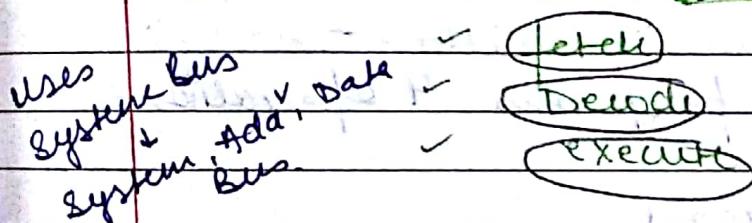
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6

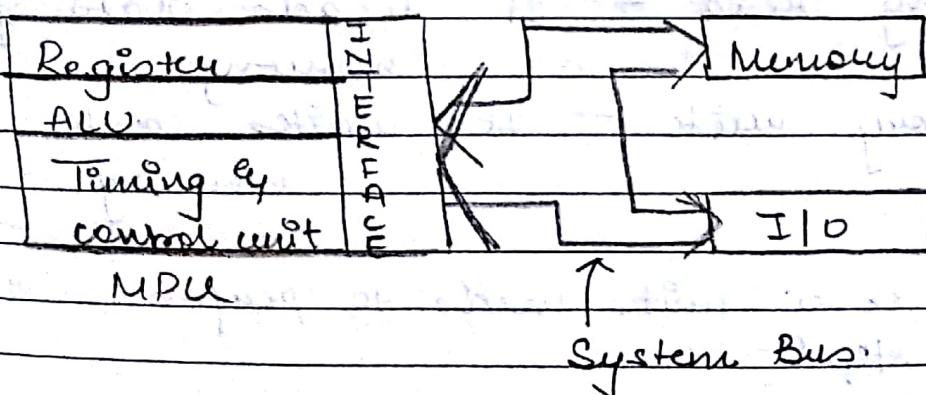
Microprocessor - A microprocessor is multipurpose programmable clock driven register based electronic device that read binary information instruction from storage device called memory accept binary data as input & processes data acc. to those inst. & provide result as output.

Working of Microprocessor.

The instructions are stored sequentially in the memory. The microprocessor fetches the first instruction from its memory decode it & execute this instruction.



The sequence of fetch, decode & execute is continued until the microprocessor comes across an instruction to stop.

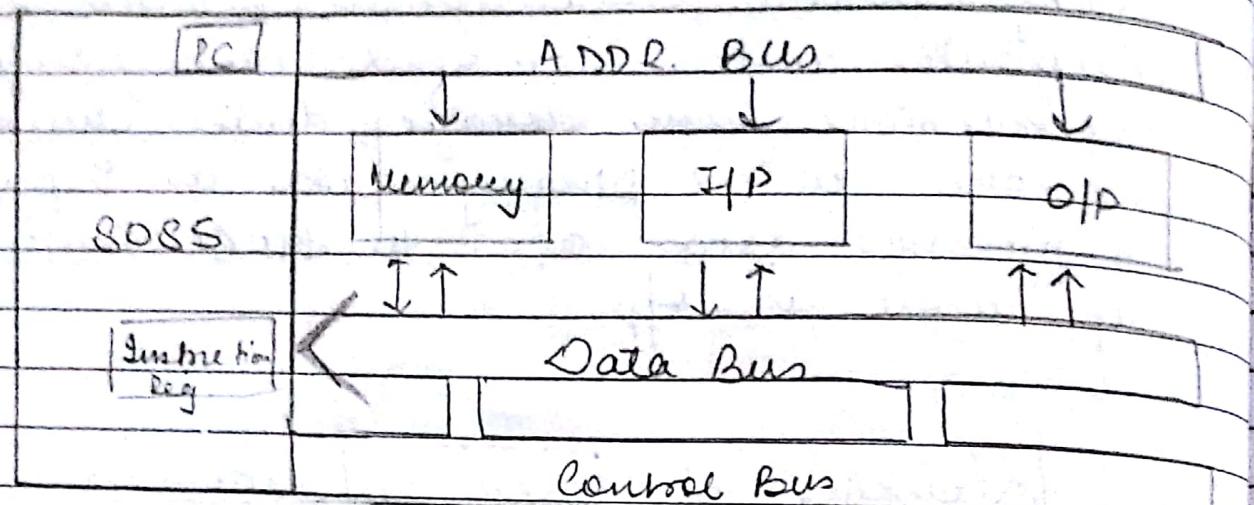


Add. bus
of 8085 \rightarrow 16 bit

Data Bus
 \rightarrow 8 bit

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Functions of Microprocessor.



1. Microprocessor initiated operation
2. Internal Data operation
3. Peripheral or externally initiated op.

1. Microprocessor initiated operation -
Microprocessor unit performs 4 operations

1. Memory read
2. Memory write
3. I/O read
4. I/O write

- Memory read - It reads data from memory
- Memory write - It writes data to memory.

Microprocessor unit needs to perform the following steps:-

16 bit $\rightarrow 2^{16}$ Combinations

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G. G.
OKB

Step1. Identify memory of peripheral location.

Step2. Transfer data/information.

Step3. Provide Timing & synchronization signals.

2 Internal Data operations -

L.1 These operation store & bit data, perform

s.2 Perform arithmetic & logical operation

s.3 Test for condition.

s.4 Sequence execution of instruction

s.5 Store data temporarily during the executions

3 Externally initiated operations -

1. Reset - Ext. devices of signal can initiate following operations for which individual pins on microprocessor chip are assigned.
2. Interrupt
3. Ready
4. Hold used in DMA.

Types of uP

Size

- 4 bit
- 8 bit
- 16 bit
- 32 bit
- 64 bit

Application

- General purpose
- Microcontroller
- Special purpose

Speed

- RISC
- CISC

Up . as a CPU

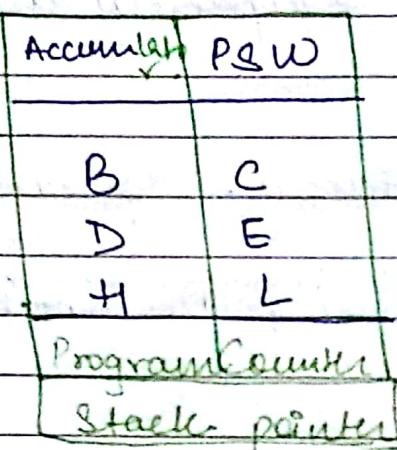
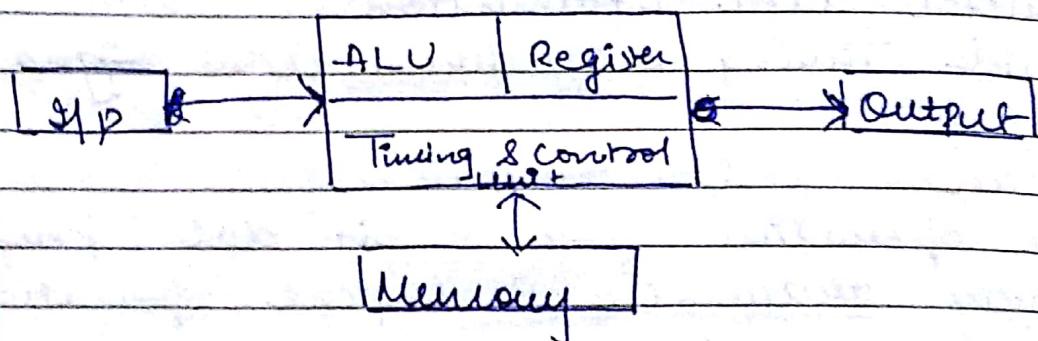


fig - General purpose reg.

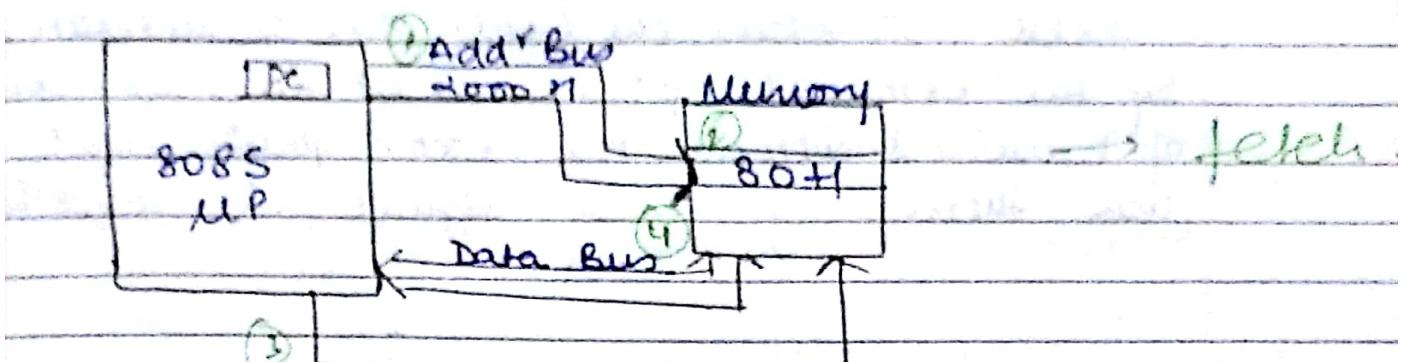
16 - bit add line

8 - bit data

$$2^{16} \times 8 = 64 \text{ KB}$$

e.g. 16 KB

↓
14 bit add line.



MERD ← multiple operations are to be performed

fig - Microprocessor Initiated operation.

Microprocessor Architecture & operation

The process of manipulation & communication is determined by logic design of microprocessor called architecture.

Exp. 2 point 3. Ext initiated operation

Reset - When the reset pin is activated by the ext. device all internal operations are suspended & the program counter is cleared.

Now the program execution can again begin at zero memory address.

Interrupt - MP can be interrupted from the normal execution of instruction & asked to execute some other inst. called a service routine.

Ready - The 8085 has a pin called ready. If the signal at this ready pin is low, the microprocess enters into wait state.

This signal is used to synchronize slower peripherals with the CPU.

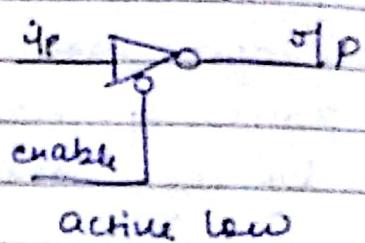
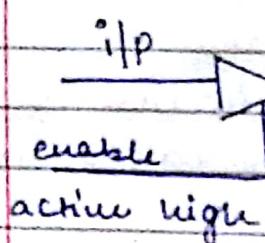
READY

held - when the hold pin is activated by the external pin the I/O releases control of buses & allow the ext. peripheral to use them. eg hold signal is used in DMA.

1) I/O

Logic devices called interfacing

The state devices.



- Tri state logic devices has 3 state
1. logic '0'
 2. logic '1'
 3. high impedance

When 3rd line called enable is activated the tri state device functions the same way as ordinary logic device.

When 3rd line is disabled, the logic device goes into high impedance state. Means it is disconnected from the system.

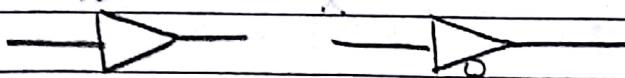
* Uses.

- Microprocessor communicate with one device at a time by enabling the tri state line of interfacing device.

Author

Buffer.

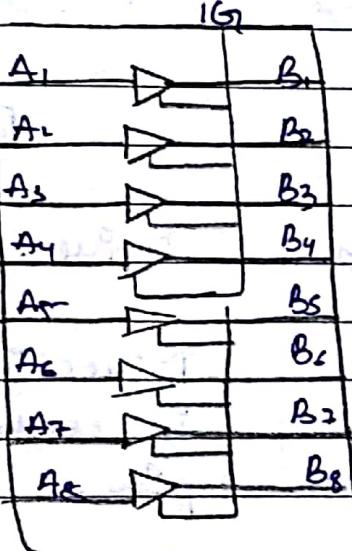
It is used to (↑)es the driving capability of logic ckt, it is also known as Driver.



buffer enable Tristate Buffer.

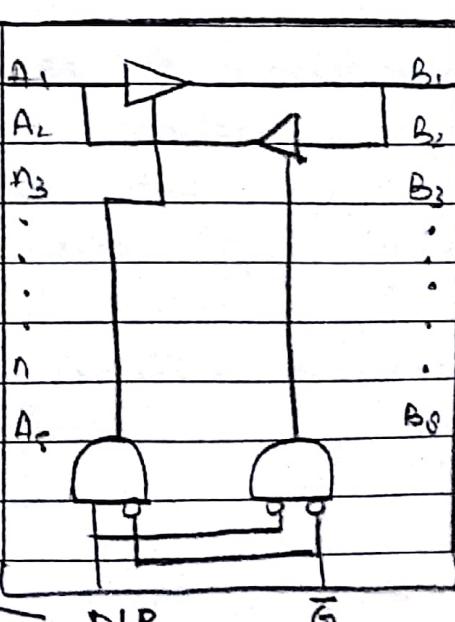
example of tristate Buffer :-

(1) Unidirectional octal Buffer.



74LS245,

2G
74LS244.



to DIRECTION
control

Enable Direction Direction
 \bar{G} Control

0	1
0	0
1	X

Data flow from A to B
 from B to A.
 $\times - \times$

Octal Buffer is Unidirectional. Octal Buffer is used as a driver for add'l Bus.

Bidirectional Octal Buffer - Used as driver for data bus

Unidirectional

① Driver for add'l Bus

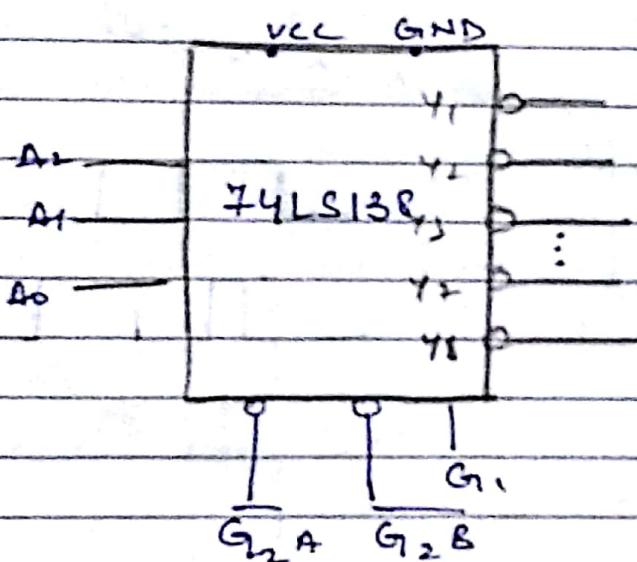
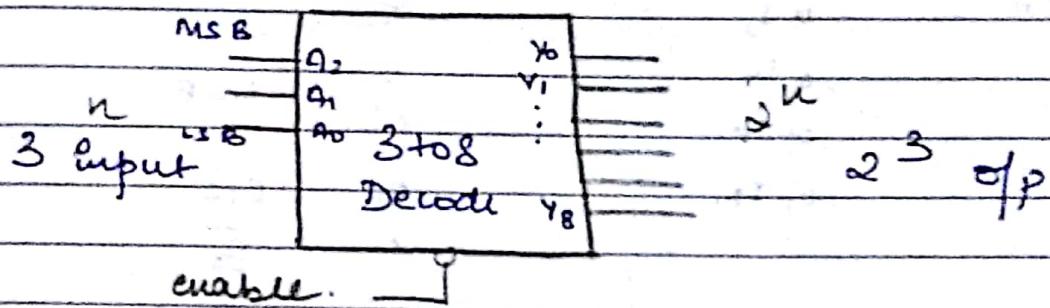
Bidirectional

Driver for Data Bus

Direction of data flow is controlled by DIR pin.

When DIR is high
 data flow from A to B
 When low, it flows (data flow) from B to A

Decoder - It is the combinational logic ckt which identify & decode each combination of the signals present at the input.

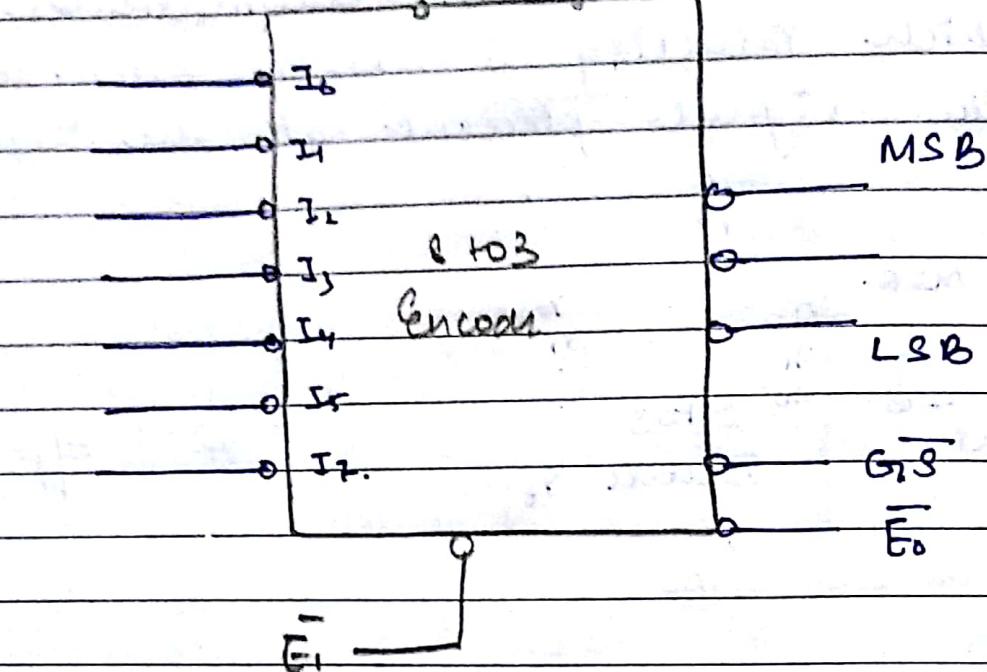


Encoder - The process of encoder is inverse of decoding. The encoder is the logic ckt that provides the appropriate code as an o/p. for each i/p signal.

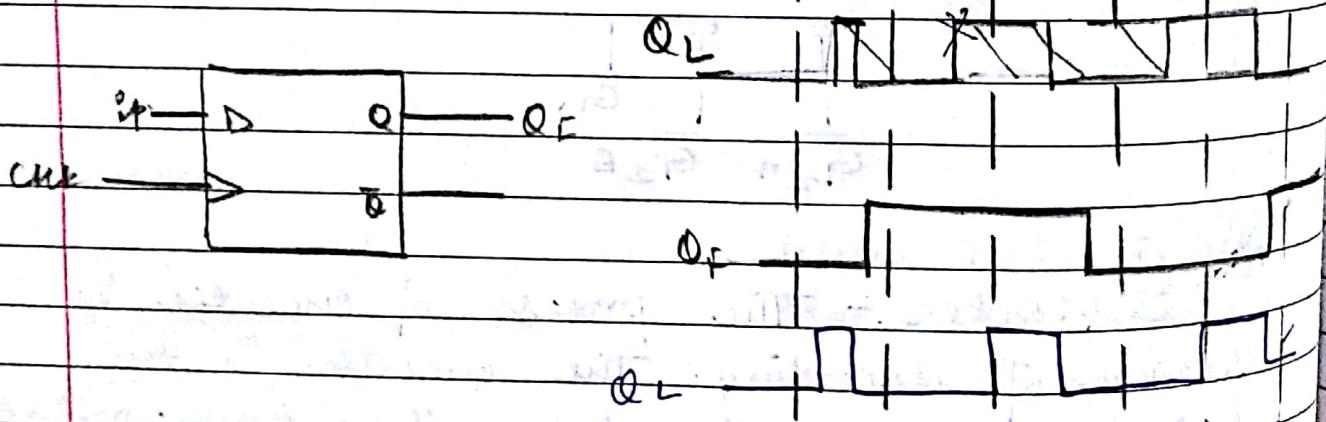
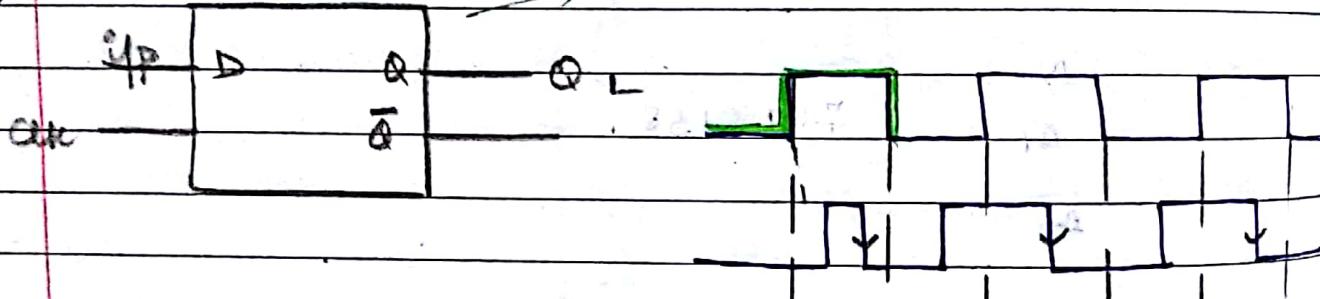
IC - 74LS148. Priority encoder.

74LS148.

VCC GND

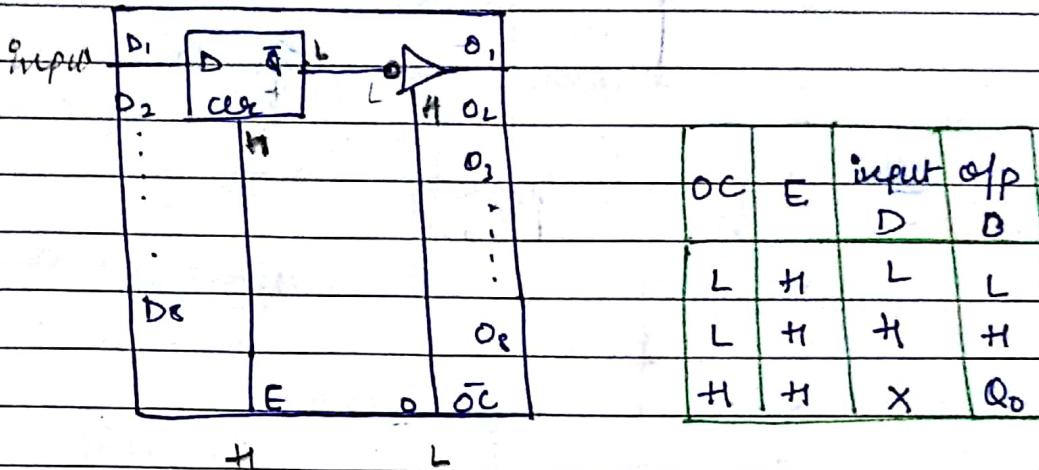


↓ latch → level : consist



Kazan

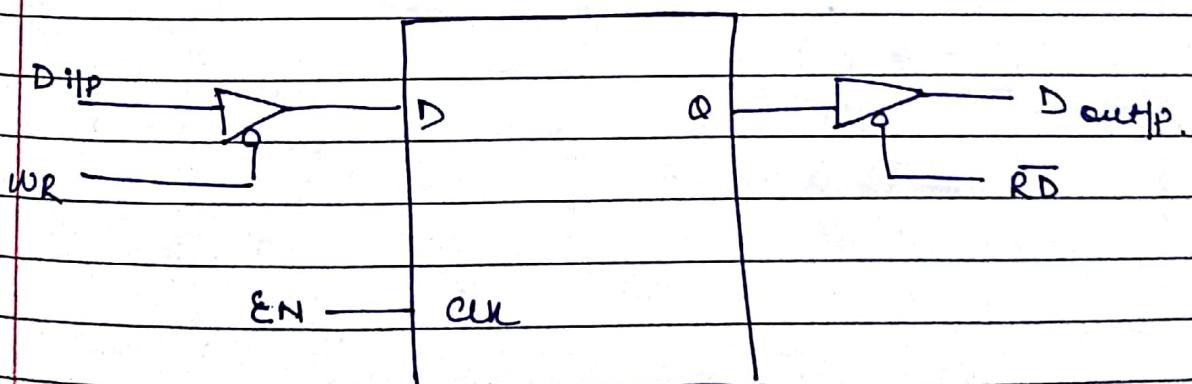
IC 74LS 373



A latch is used to interface o/p devices when we use the microprocessor.

unit sends the o/p, data are available on the data bus for only few micro seconds. ∴ a latch is used to hold data for display.

$\text{clk} \Rightarrow L$ | $\bar{Q} \Rightarrow L$ for hold position
 $\bar{Q} \Rightarrow L$ for o/p use
 \therefore output will go to high impedance.



1 bit Memory cell

4 bit Single Reg

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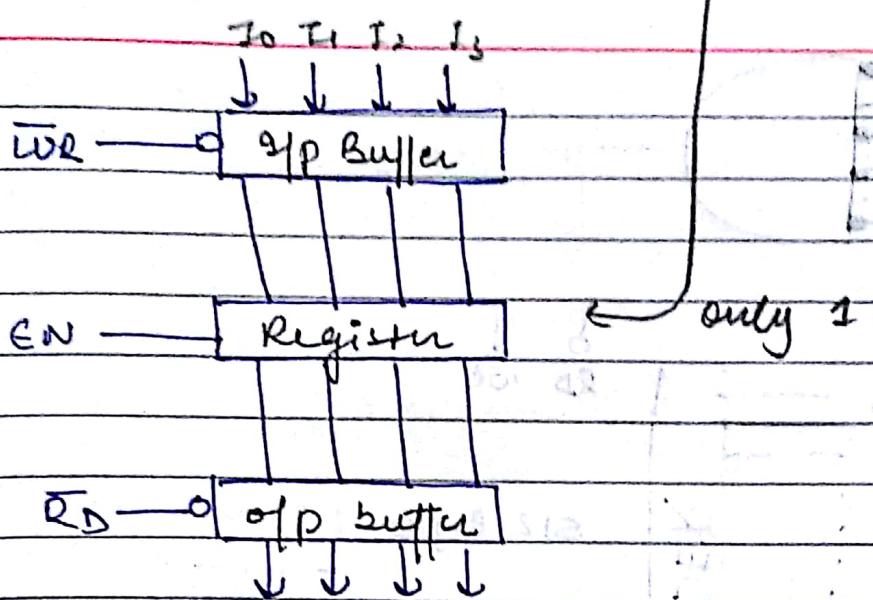
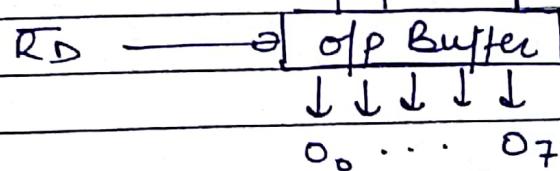
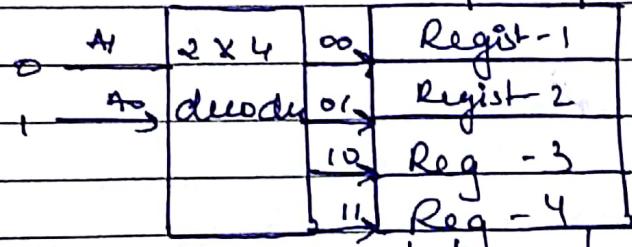
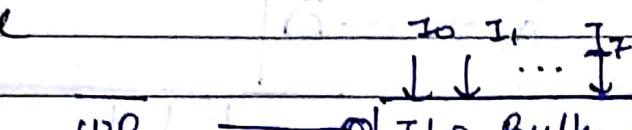
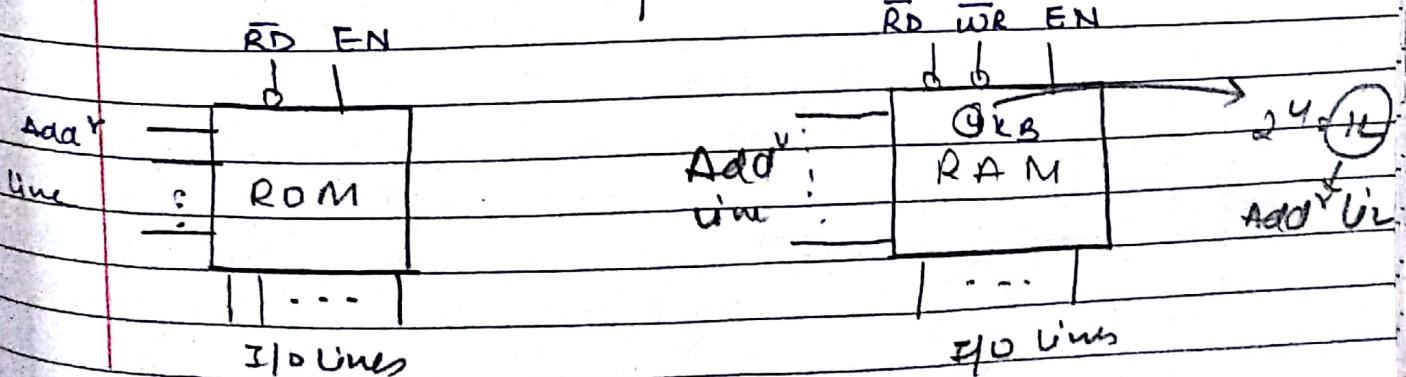


fig - Internal



Model of Ram & Rom



eq

A₇
A₆

A₅



A₂

RD WR EN

DECODE R
DECODER

S12 Bytes

RAM

A₀

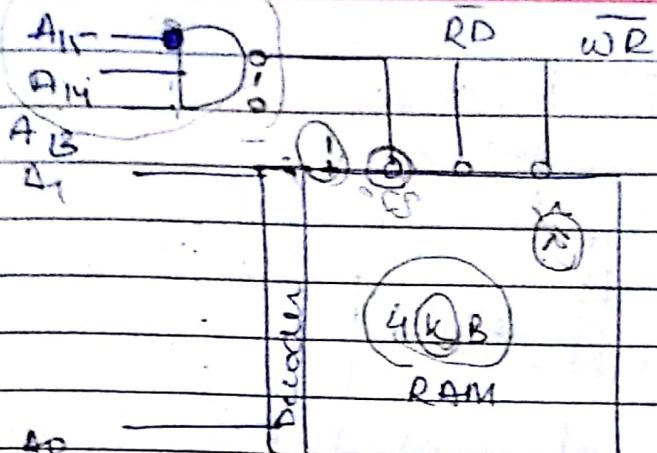
8 bit.

3 feb
diagram

Q11

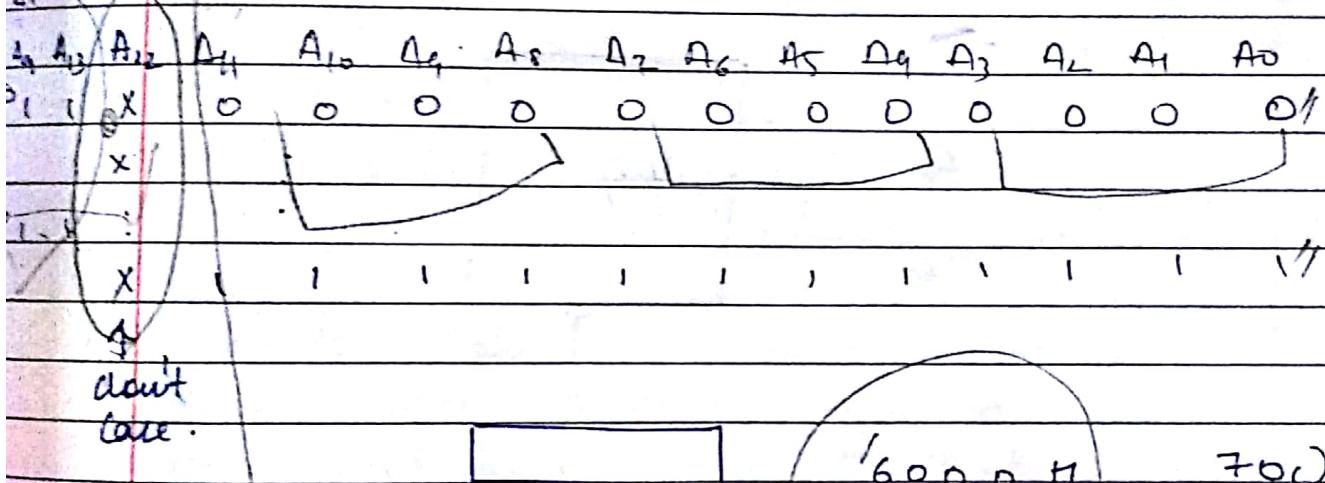
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Q1

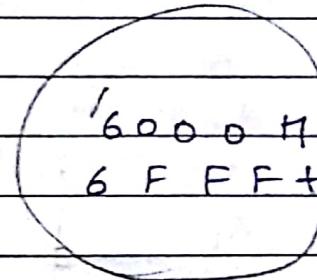


A_0

No. of add. line \Rightarrow $2^{12} \Rightarrow \underline{\underline{12}}$



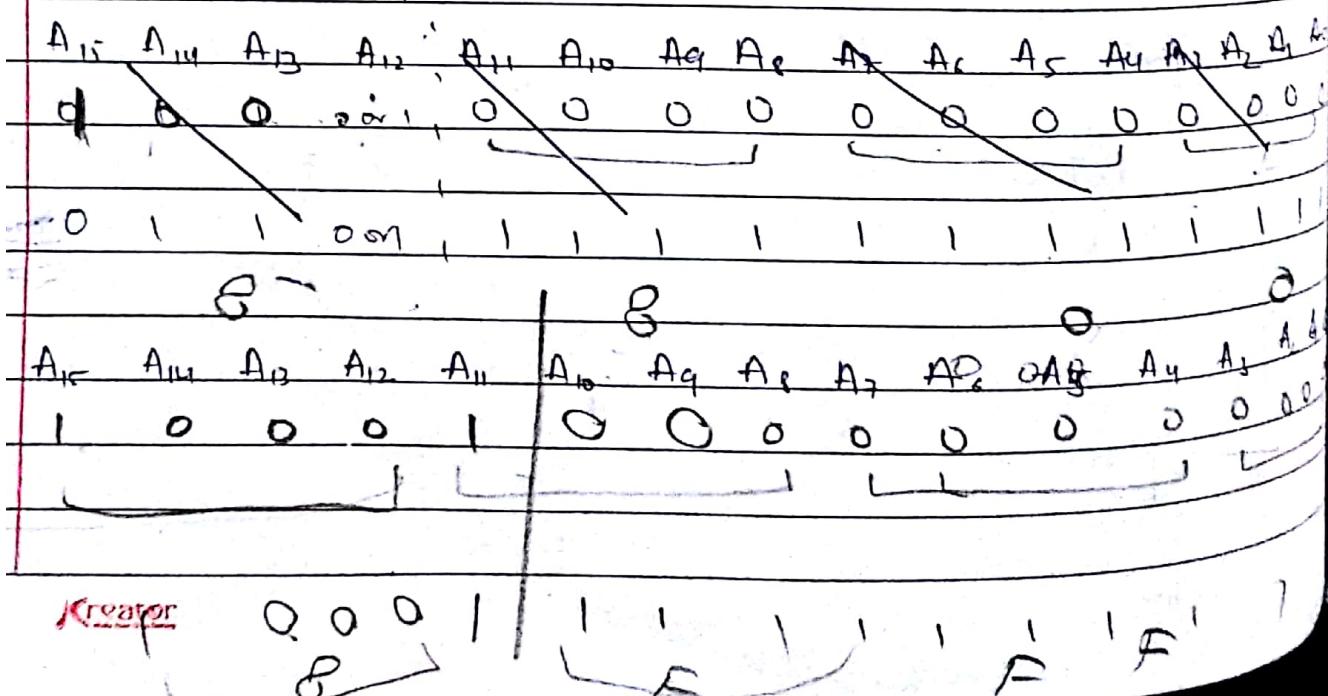
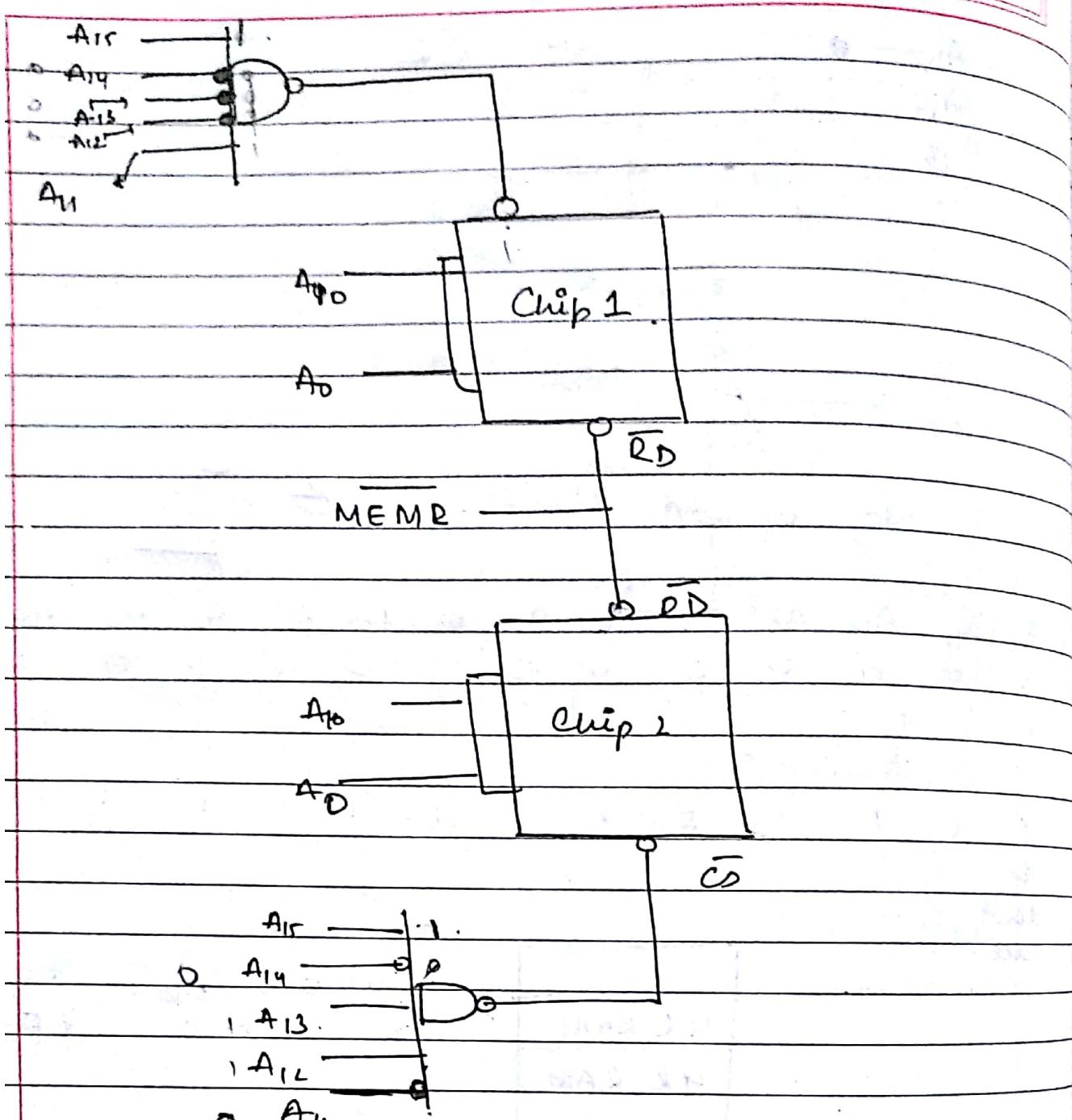
4K RAM
4K RAM



Q

P.T.O

Kramer



$$1B = 8 \text{ byte}$$

8800 → 8FFF.

memory chip size is

Q If $\frac{1}{2}KB$ RAM
 $\frac{1}{2}KB$ chip.

2048×8 how

many chips are req to make 16KB memory.

$$\frac{2^9 \times 8 \cdot 5}{2^{10} \times 4} \rightarrow B$$

<u>Q</u>	2048×8	1024×4	256×1 → giving 6 th 8 th 25 th banana
	$\frac{16 \text{ KB}}{(K=2^{10} + 2^{10})}$	$2 \text{ KB} \rightarrow 2^4$	$1 \text{ KB} \rightarrow 2^3$ → req.
	$2^{14} \rightarrow 2048$ → 8 chip	$2^0 \rightarrow 4 \text{ chip}$	$2^4 \rightarrow 2^5 \rightarrow 32 \text{ chip}$ $2^{10} \div 2^5 \rightarrow 32$

Q. 4KB RAM.

Starting Addr AA00H.

No. of add' lines $\rightarrow K = 2^{10}, 4 = 2^2$

$$10+2 \rightarrow 12$$

Q $\frac{12}{2} = 6$ add' lines

$\frac{12}{2} \rightarrow 6$ add' lines

$\rightarrow 000 \rightarrow FFF$

initial state AA00 + 000 → AA00

final state AA00 + FFF →

$\left. \begin{array}{cccc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{array} \right\} \begin{array}{c} 1111 \\ F \end{array} \quad \left. \begin{array}{cccc} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{array} \right\} \begin{array}{c} 1111 \\ F \\ F \\ F \end{array}$

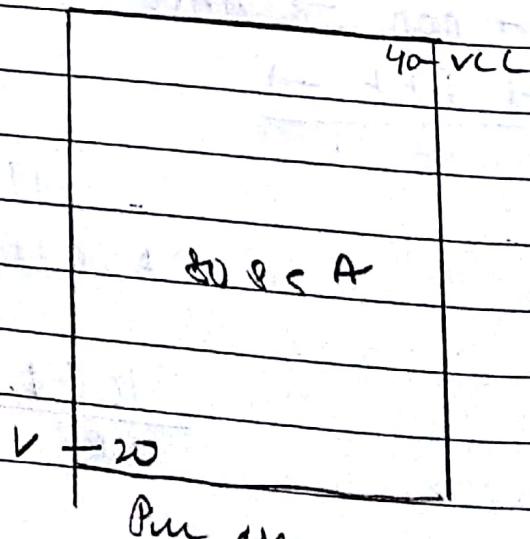
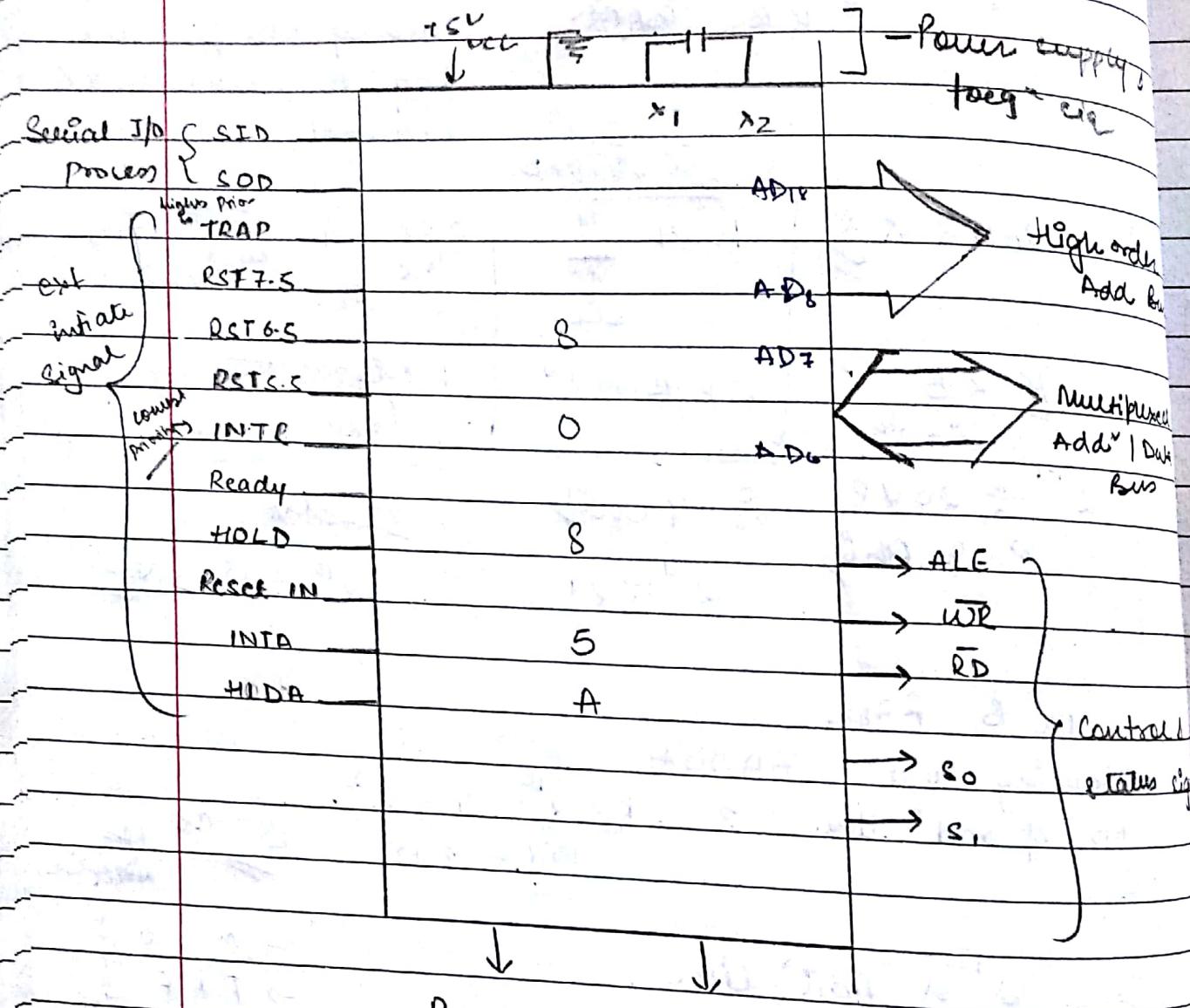
11
1010
1111

1010
1111

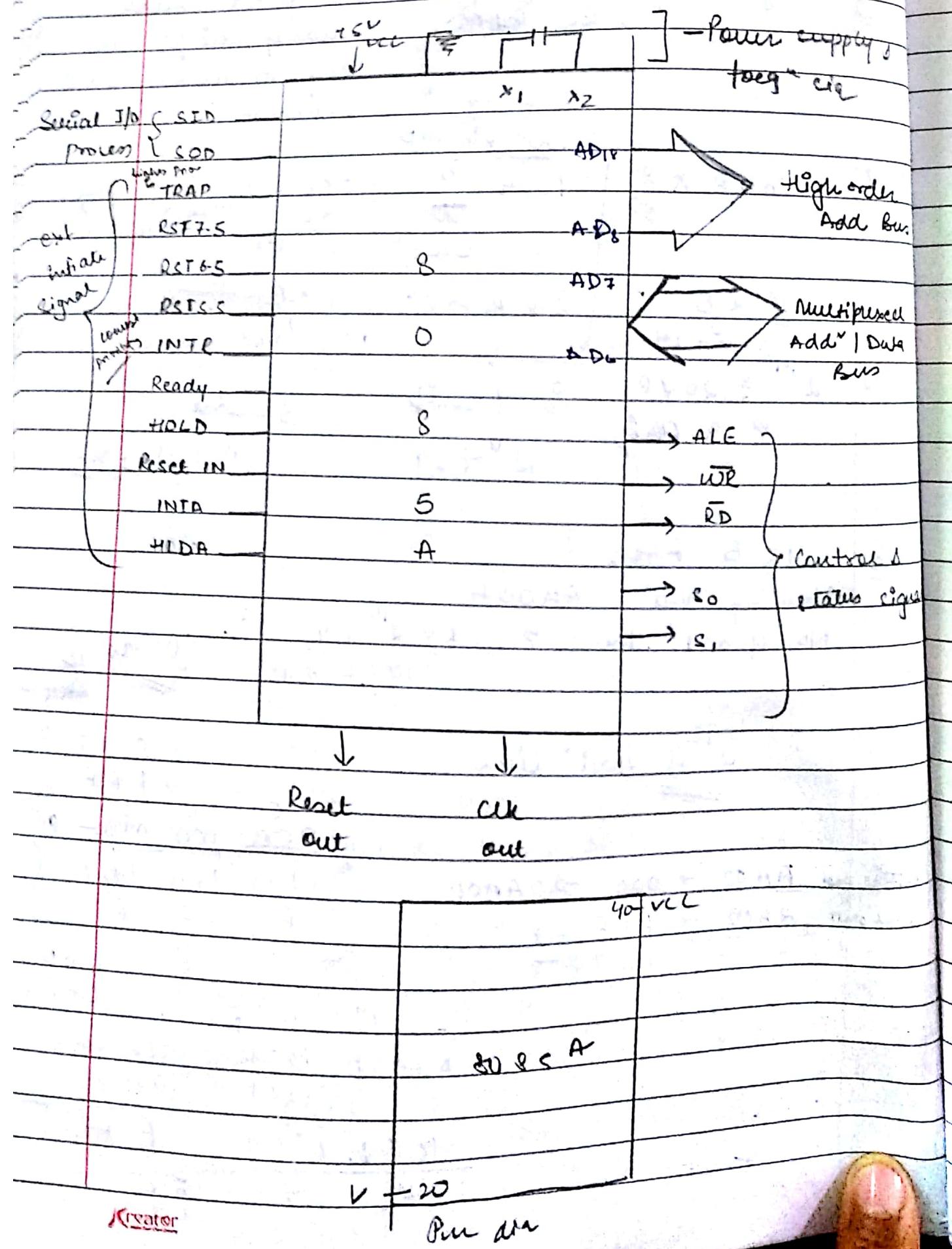
1000 1001
B 9 FF

Kreator

Features of 8085 micro processor



Features of 8085 micro processor



Features of 8085 microprocessor :-

i) It is an 8 bit general purpose microprocessor such as it can accept process or provide 8 bit data simultaneously.

It operates on single 5V power supply connected to VCC bit

It can operate with a 3 mega hertz freq.

It has 16 add^r lines, hence it can access 64KB memory.

It provides 8 bit I/O add^r to access 2^8 i.e. 256 I/O codes.

In 8085 the lower 8 bit address bus A₀ to A₇ & data bus D₀ to D₇ are multiplexed to reduce no. of external pins. But due to this external hardware (Latch) is required to separate add^r & data Bus.

It supports 74 different instructions/operations & 255 instructions.

Features of 8085 Pin diagram.

All the signals of 8085 chip can be classified into 6 groups

- ① Power supply & freq^u signal
- ② Add^r Bus

(3) Data Bus

Serial I/O port

Externally initiated signal

Control & status signal

Explanation

(1) Address Bus - The 8085 has 16 signal lines that are used as the address bus. These lines are split into 2 segments

↳ A₁₅ to A₈ C Unidirectional Add^r Bus↳ A₇ to A₀.(2) Multiplexed add^r & data Bus - (A_{D7} to A_{D0})They are used as the low order add^r bus as well as data bus.The low order add^r can be separated from these pins by using a latch.(3) Control & Status signal - This group of signal includes two control lines signal - Read & Write signal. Three status signals I/O/M, S0 & S₁ to identify the nature of the operation and one special signal ALE to indicate the beginning of operation.

• ALE (Address latch enable)

This signal is used to latch the low order address from the multiplexed bus to generate a separate set of 8 address lines A₇ to A₀.• Read (R_D)

Read signal indicates that the selected I/O memory device is to be read & data

are available on data bus. The data on the data bus are to be written into a selected memory & I/O location.

- IO/\bar{M}

This is the status signal used to diff. b/w I/O and memory devices. When IO/\bar{M} is high it indicates an I/O operation, when it is low it indicates Memory operations

- S, & SO

These status signal similar to IO/\bar{M} can identify various operations.

Machine cycle	IO/\bar{M}	S, SO	Control signal
• Opcode	0	1 1	$\overline{RD} = 0$
Fetch	0		
• Memory Read	0	1 0	$\overline{RD} = 0$
• Memory Write	0	0 1	$\overline{WR} = 0$
• I/O Read	1	1 0	$\overline{RD} = 0$
• I/O Write	1	0 1	$\overline{WR} = 0$
• Interrupt Acknowledge	1	1 1	$\overline{INTA} = 0$

Power Supply by

Freq. Signal

Power supply

↳ V_{CC} : +5V power supply

↳ V_{SS} : GND

↳ X₁ & X₂ - A crystal oscillator is connected at these two pins & clock output - This signal can be used as the system clock for other devices.

Externally I/O signal using
interrupt

INTR - Interrupt request

This is the general purpose interrupt.

INTA - Interrupt Acknowledge.

This is used to acknowledge the interrupt.

RST 7.5, RST 6.5, RST 5.5 - Restart interrupt

These are vectored. A maskable interrupt that transfers the program counter to specific memory location.

$$\text{RST } 7.5 \times 8 = (60)_{10} = (003C+1)$$

$$\text{RST } 6.5 \times 8 = (52)_{10} = (0034+1)$$

$$\text{RST } 5.5 \times 8 = (44)_{10} = (002C+1)$$

Non maskable, highest priority

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$$\text{TRAP } (\text{RST 4-5}) \times 8 = (36)_0 = 01024 + \dots$$

Is an interrupt.

TRAP - This is the non maskable interrupt & has highest priority.

TRAP > RST 7-S > RST 6-S > RST 5-S > INTR

Priority order of interrupt.

affib

o Hold - This signal indicates that a peripheral such as DMA controller is requesting the use of address bus & data bus.

Hold o HLDA - This signal acknowledge the whole request by releasing the address and control data buses of microprocessor.

o Ready - This is used to interface with the slow peripheral (Memory & I/O) devices to the CPU. When ready signal goes low, the CPU waits for an integral no. of clock cycle until it goes high.

Ready signal is used to delay the up, read or write cycle until a slow peripheral is ready to send or receive data.

Wait signal state

(Bar)

$\downarrow \rightarrow$ Remember (bar) * \Rightarrow Active low

- Reset in - When this signal on this pin goes low, the program counter is set to 0. The bytes are restated \Rightarrow the CPU unit is reset.
- Reset OUT - This signal indicates that the CPU is being reset \Rightarrow this signal can be used to reset other devices.

Serial I/O Port.

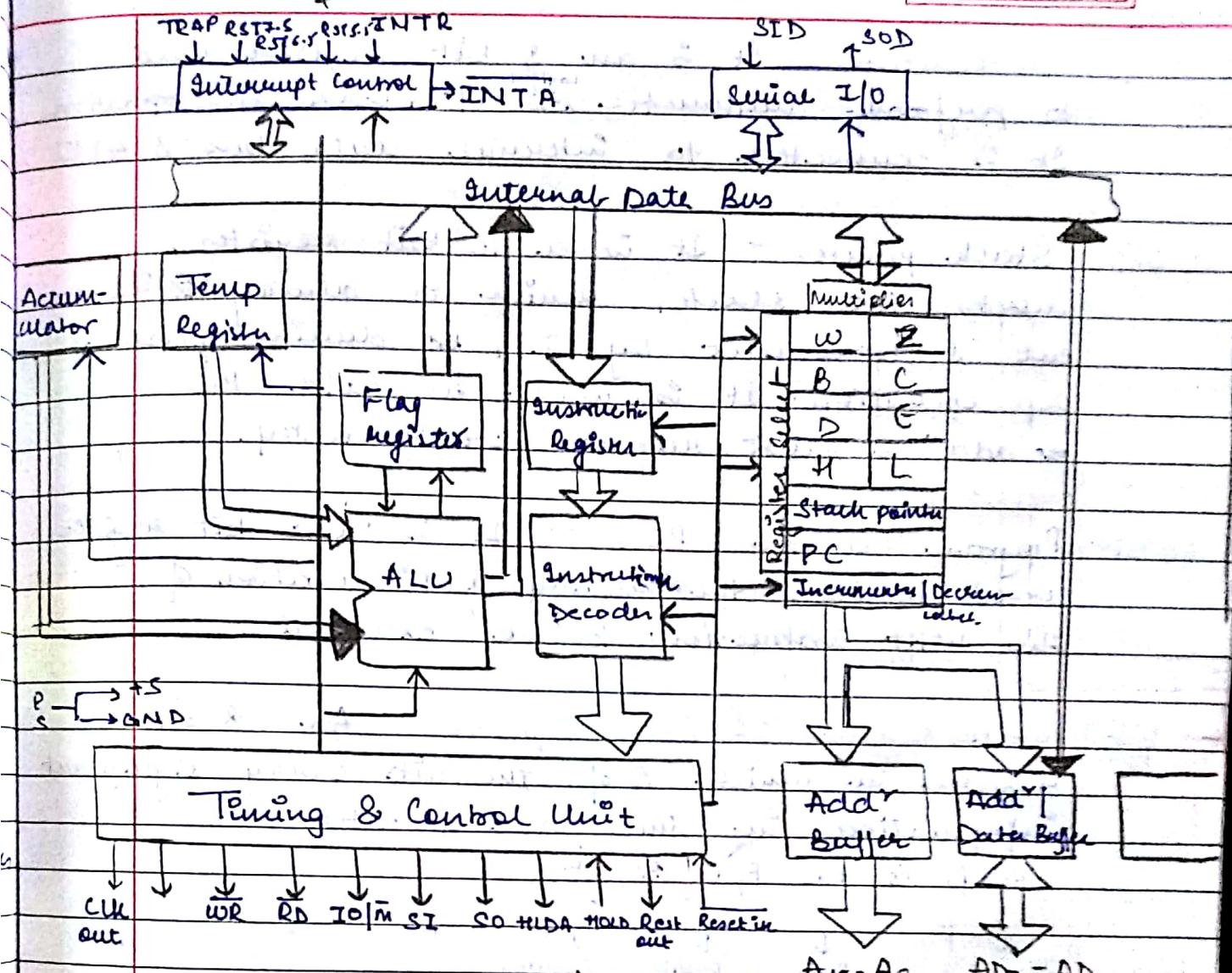
- Serial I/O port - The 8085 has 2 signals to implement serial transmission -
 - \swarrow SID
 - \searrow SOD
- SID - This input signal is used to accept serial data bit by bit from the external device.
- SOD - This is an output signal which enables the transmission of serial data bit by bit to next. device

Accumulator Temp
sign

Arch. of 8085

Very copy & paste happen
& cut paste

Op initiated - outward dir.
Ext initiated DATE forward BY -
PAGE No.

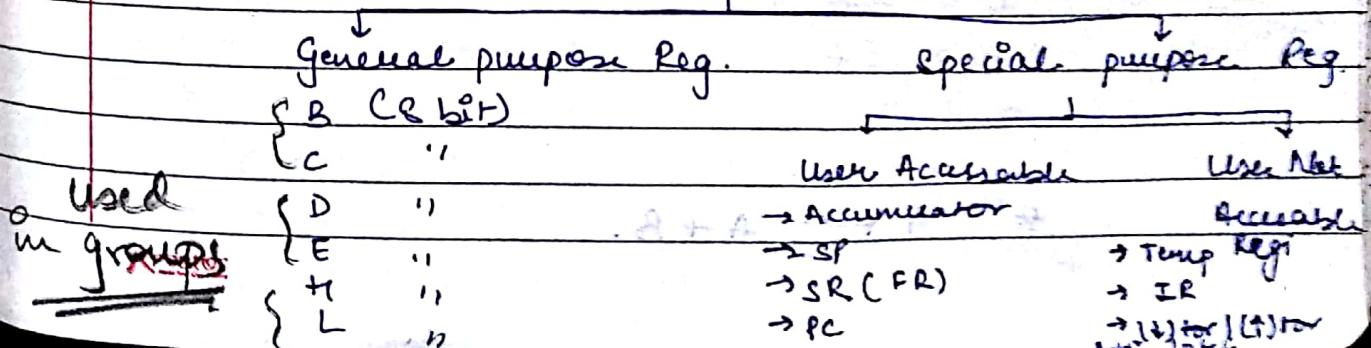


- 1) ALU - It performs arithmetic & logic operations like - addition, subtraction, and, OR, etc on 8 bit data.

ALU can perform 20 arithmetic operations by 14 logical operations.

- 2) Register Array -

Registers



User Accessable

Accumulator - It is an 8 bit register used to perform arithmetic ^{logical} I/O, loads store operation. It is connected to internal data bus & ALU.

(16 bit) Stack pointer - It is a 16 bit register, works like stack, which is always ~~increm~~ increment & decrement by 2, ~~is~~ during push & pop operation. It is used to hold the ~~add'~~ address of most recent stack entry.

(16 bit) Program Counter (PC) - It is a 16 bit register used to store the "memory add" location of the next instruction to be executed.

(8 bit) Status Register OR Flag Register - An 8 bit register in which 5 of the bits carry significant information in the form of status flag.

F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀
S	Z	X	AC	X	P	X	CY
Sign flag	Zero flag	Aux. flag	Parity Flag	Parity Flag	Carry Flag	Carry Flag	

PSW

(Prog status word)

*** Jump topic

Ans

$$A = 37$$

$$B = 57$$

→ ADD B

$$\therefore A \leftarrow A + B.$$

Kreator

$$\begin{array}{r}
 & 0 & 0 & 1 & 1 & 0 & 1 & \leftarrow A \\
 + & 0 & 1 & 0 & 1 & 1 & 1 & \leftarrow B \\
 \hline
 & 1 & 1 & 0 & 0 & 1 & 1 & \text{CY}(\text{H}) \\
 & & & & & 0 & 1 & \leftarrow C \quad (\text{Not here})
 \end{array}$$

10010100

$$\begin{array}{r}
 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & \rightarrow \text{This carry is} \\
 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & \text{known as AC.} \\
 \rightarrow & 0 & 1 & 0 & 0 & 1 & 1 & 0 \\
 \hline
 & & \overline{s} & & & & &
 \end{array}$$

even parity $\Rightarrow 4^{\text{th}}$ 1's are even

$$CY = 0$$

$$P = 1 \text{ (even)} \therefore$$

$$AC = 0$$

$$\Sigma = 0 \rightarrow C \because \text{all nos are not zero}$$

$$S = 1 \quad C \because \text{sign bit}$$

Q2.

$$A = 6eH$$

$$B = 94H$$

$$\begin{array}{r}
 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\
 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \\
 \hline
 & \overline{s} & & & & & &
 \end{array}$$

Penultimate
(~~C~~)

$$CY = 1$$

$$AC = 1$$

$$S = 0$$

$$P = 1$$

$$\Sigma = 1$$

Kreator

Sign flag - After the execution of arithmetic & logical operation, if D₇ bit of the result is 1 (set) the sign flag is set (1) otherwise it is reset (0).

Zero flag - If the result of the operation in ALU is 0, the zero flag is set. Otherwise it is reset.

Auxiliary - If there is overflow out of 3rd bit or carry is generated from D₃ to D₄ bit, the auxiliary carry bit is set (1) else Reset (0).

Ours

$$A = 52H$$

$$B = CBH$$

$$A \text{ AND } B$$

$$A = 10$$

$$B = 11$$

$$C = 12$$

$$A \leftarrow A + B$$

$$\begin{array}{r} 0101 \\ + 1100 \\ \hline 10001 \end{array}$$

$$\begin{array}{r} 0010 \\ + 1011 \\ \hline 1101 \end{array}$$

$$CY = 1$$

$$P = 1$$

$$AC = 0$$

$$Z = 0$$

$$S = 0$$

Add Bus
to 85

Higher Order Lower Order

DATE _____
PAGE No. _____

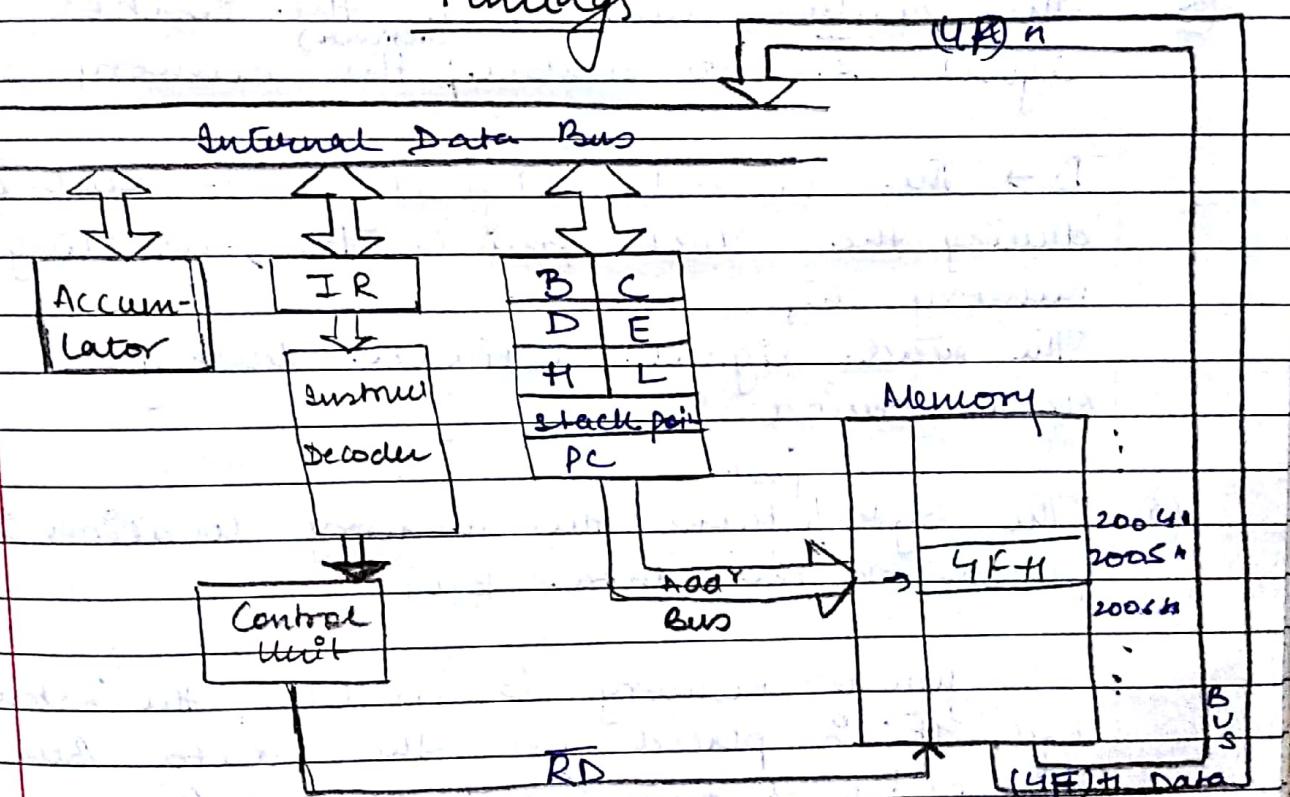
* (Cmp)

Parity flag - If the result of ALU has even no. of 1's, parity flag is set. If there is odd no. of 1's then parity flag is reset.

Carry flag - If an arithmetic operation results in a carry, the carry flag is set, else reset.

Microprocessor Comm. by Bus

Timings



The fetch the instruction in the form of byte, the MPC performs following steps :-

- (1) The microprocessor place the 16 bit word

from the program counter on the add^v bus.

In figure,

^{of mem}
 $T_1 \rightarrow$ At $\neg T_1$ state, high order add^v (20H) is placed on add^v Bus A_{15} to A_8 add^v bus & the low order memory add^v is (05) placed on AD₇ to AD₀. And the ALE signal goes high. Similarly IO/M goes low indicating that this is a memory related operation.

(2) The control unit sends the control signal RD to enable ^(activate) the memory chip.

$T_2 \rightarrow$ The Control signal is sent out during the clock period T_2 , enabling the memory chip.

The read signal activate during 2 clock period.

(3) The byte from the memory location is placed on the data bus.

When memory is enable, the instruction byte 4F is placed on the data bus D₇ to D₀ & transfer to the M.P.

When RD (Read) goes high, it causes the bus to go into high impedance state.

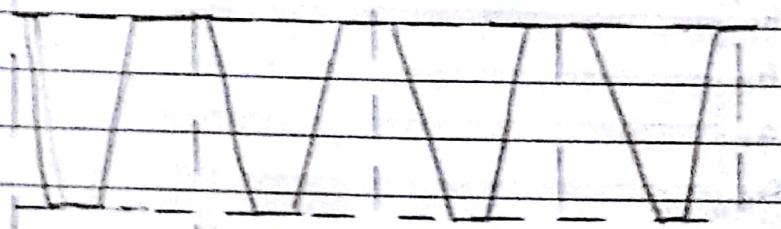
(4) The byte is placed in instruction decoder through the instruction register of the microprocessor.

and the task is carried out according to the instruction.

Timing

diag :- ← opode feed →

T₁ | T₂ | T₃ | T₄ |



AD₁₅

AD₈

AD₂

AD₀

ALE

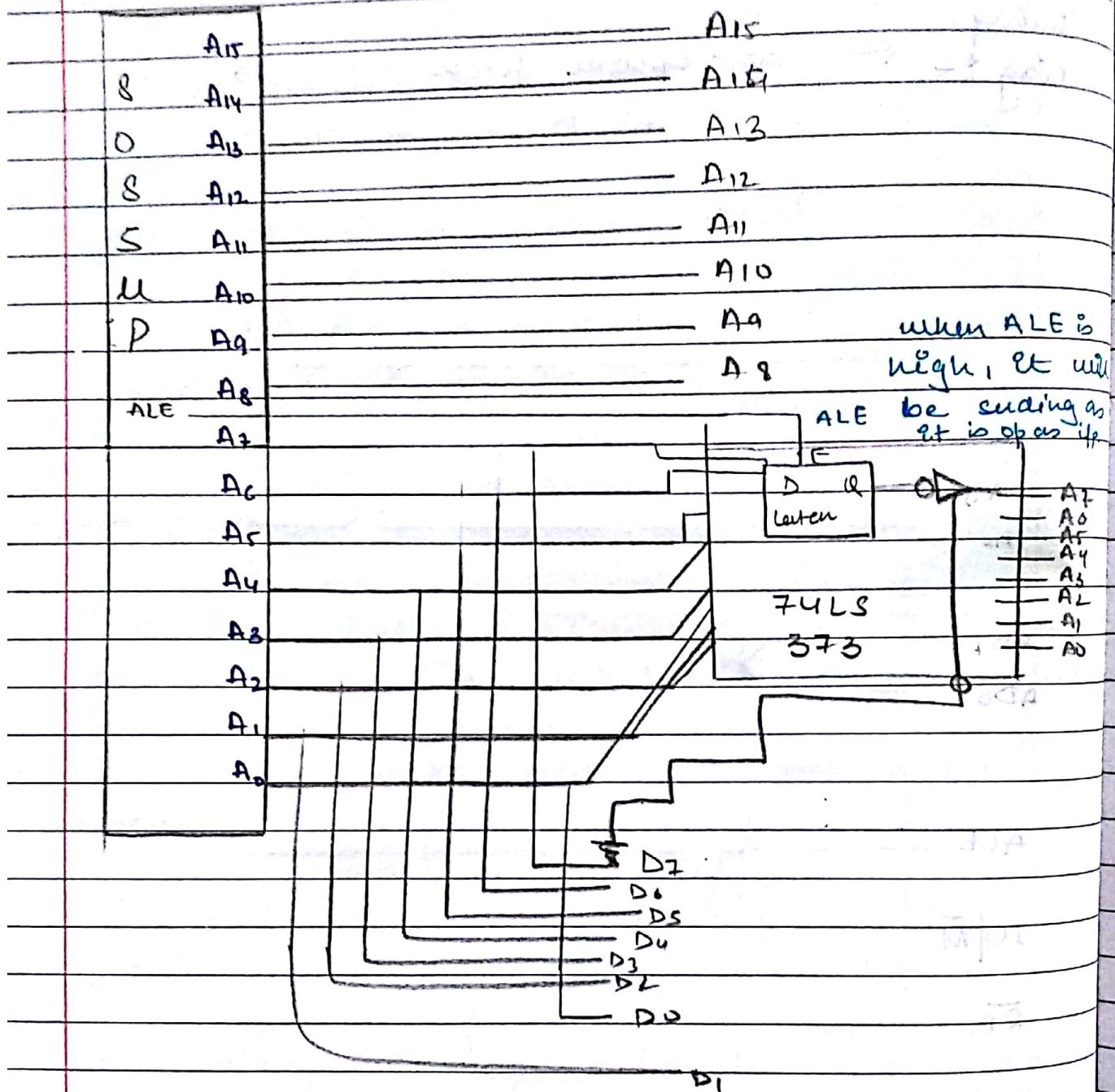
RD

RD

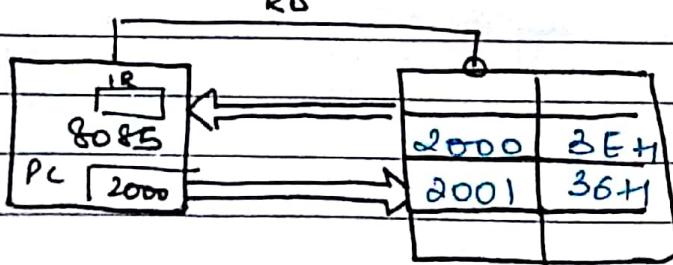
RD

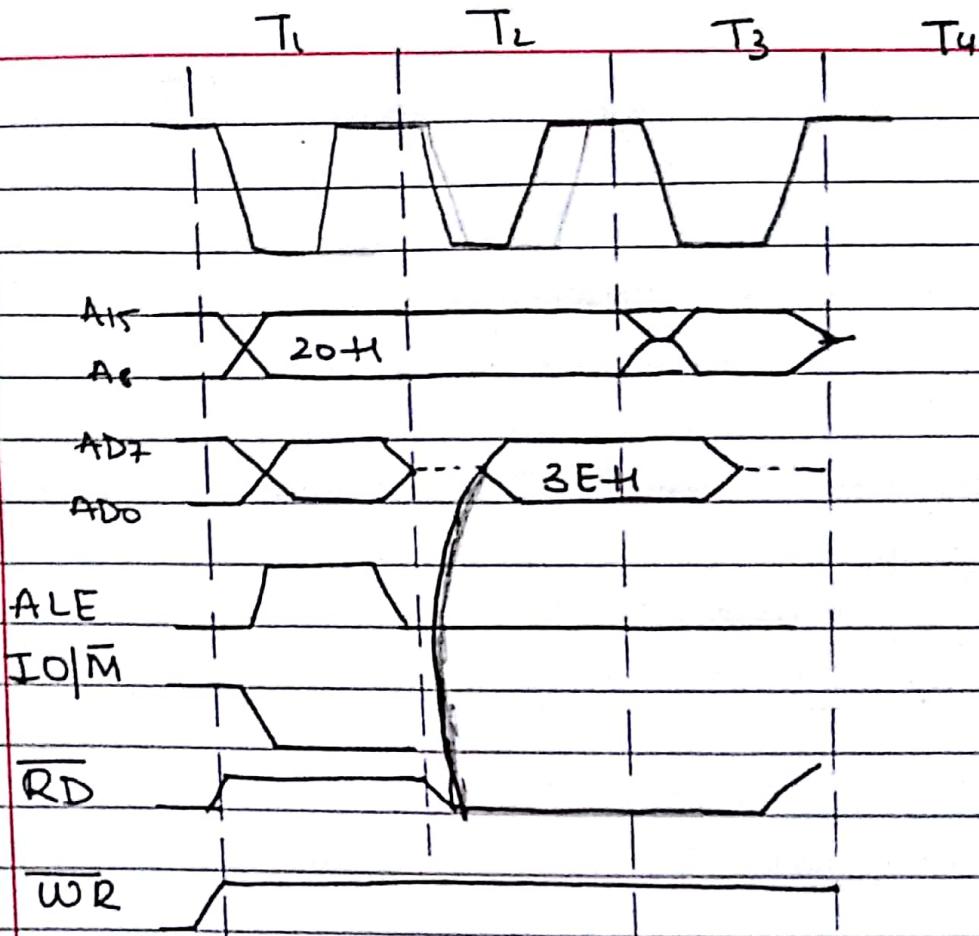
Demultiplexing of Bus

AD₇ - AD₀.



Draw timing dia of 2000H → MVI A, so tell the time it will take.





Q Draw the timing diag. of STA 2045H.

Starting location \Rightarrow 2000 H 32H

Store the content of 2001 + 45H
accumulation in the 2002 + 20 H
memory location 2045.

Diff. b/w Define (1) Instruction cycle
Clock cycle (T-state)
Machine cycle.