

VL502: Analog IC Design, 2024-2025 Final Project

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Project Title: Flipped Voltage Follower

GitHub Link: Flipped-Voltage-Follower

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1 Specifications

Design Specifications: We have used gptk90 PDK for simulations in Cadence Virtuoso

Table 1: Specifications of Flipped Voltage Follower

Parameter	Value
Input Voltage (V_{in})	1.4 V
Output Voltage (V_{out})	1 V
Power Supply Rejection Ratio (PSRR) at heavy load ($I_{load,min}$)	60 dB
Maximum Load Current ($I_{load,max}$)	2 mA
Load Capacitance (C_{load})	10 mA
Quiescent Current ($I_{quiescent}$)	1 μ F
Quiescent Current ($I_{quiescent}$)	50 μ A

2 Purpose of an FVF

The Flipped Voltage Follower (FVF) is a circuit topology widely used in analog electronics. It is a variation of the classic voltage follower (buffer) with improved performance in certain applications. The FVF is an analog voltage buffer circuit with fast local feedback, resulting in high bandwidth. The FVF consists of a transistor configured with a feedback mechanism to maintain a low output impedance.

- **Voltage Buffering:** Provides a low-impedance output to drive loads without significant voltage drop.
- **Current Boosting:** Amplifies current capability while maintaining the input voltage, making it suitable for driving heavier loads.
- **Low Voltage Operation:** Operates efficiently at low supply voltages, making it ideal for modern low-power applications.
- **High Bandwidth:** Offers excellent frequency response, suitable for high-speed signal processing.

3 Relevance of Techplots

Steps to generate Techplots:

- **Design the Circuit:** Draw the NMOS/PMOS circuit using Cadence.
- **Launch Simulation Environment:** Open the **ADE-XL (Analog Design Environment-XL)** window.
- **Load Variables:** Load all variables that need to be parameterized for the analysis.
- **Define Figures of Merit (FoMs):** Use the calculator window to create expressions for the required Figures of Merit (FoMs), such as:

$$\frac{g_m}{I_D}, \quad I_D, \quad f_t, \quad g_m r_o$$

- **Set Output Options:** Choose the **Wave vs. Wave** option to view relationships between variables as plots, such as:

$$\begin{aligned} & g_m r_o \text{ vs. } \frac{g_m}{I_D}, \\ & \frac{I_D}{W} \text{ vs. } \frac{g_m}{I_D}, \\ & f_t \text{ vs. } \frac{g_m}{I_D}. \end{aligned}$$

- **Parameterize and Run Simulation:** Parameterize the required variables, and click **Run** to generate the output plots.

3.1 NMOS Tech Plots

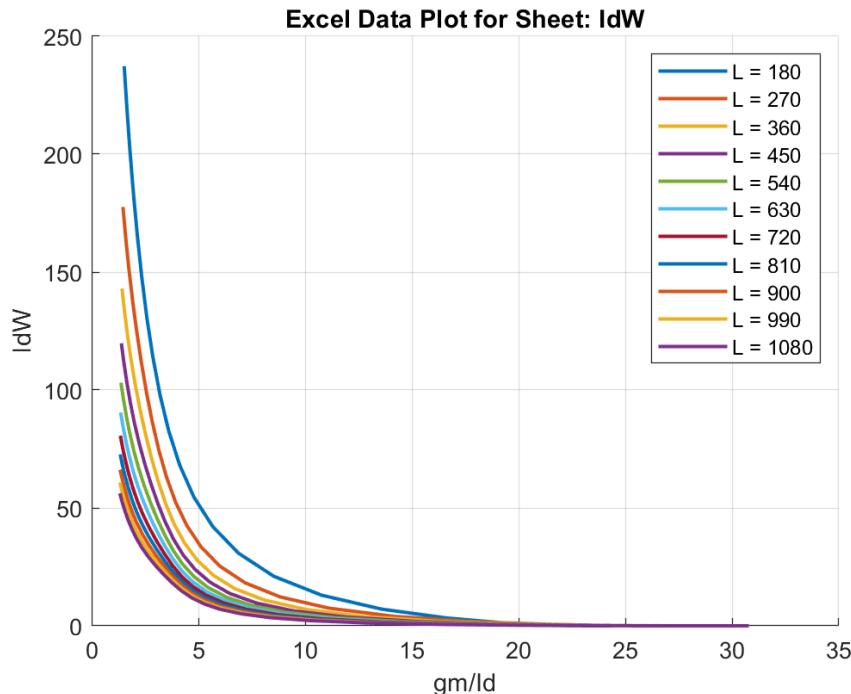


Figure 1: NMOS Techplots after Matlab postprocessing - Id/W

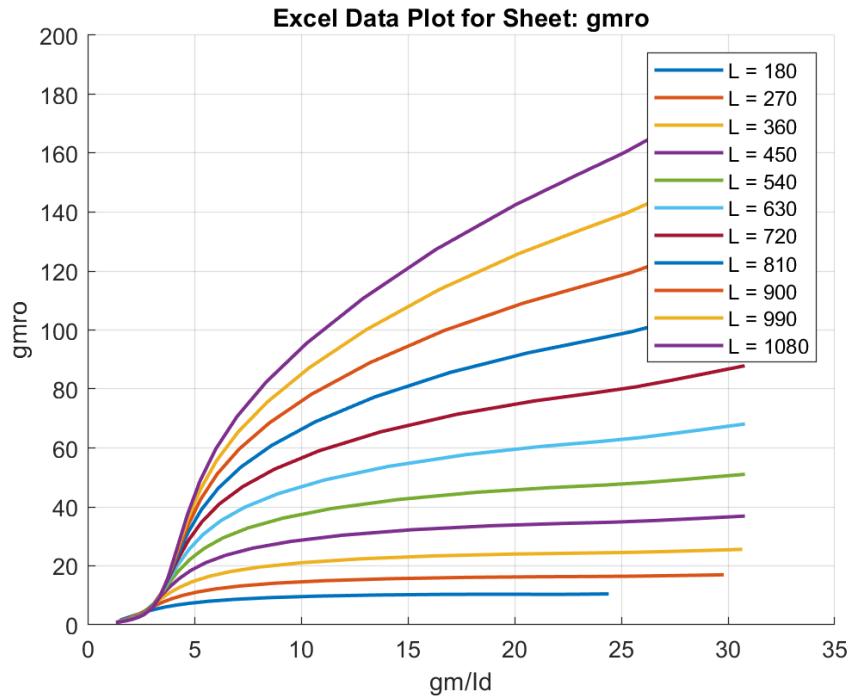


Figure 2: NMOS Techplots after Matlab postprocessing - gmro

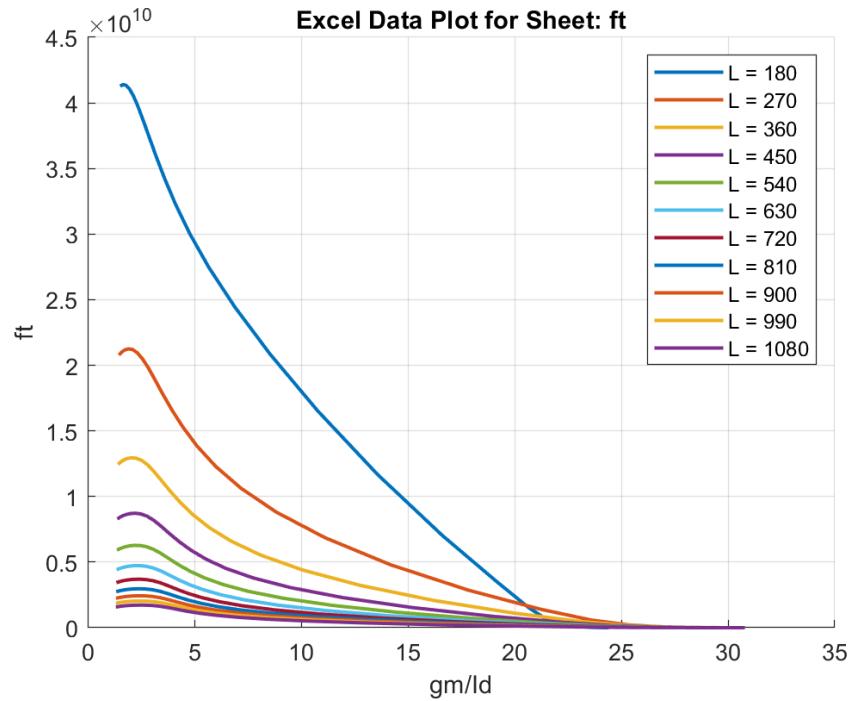
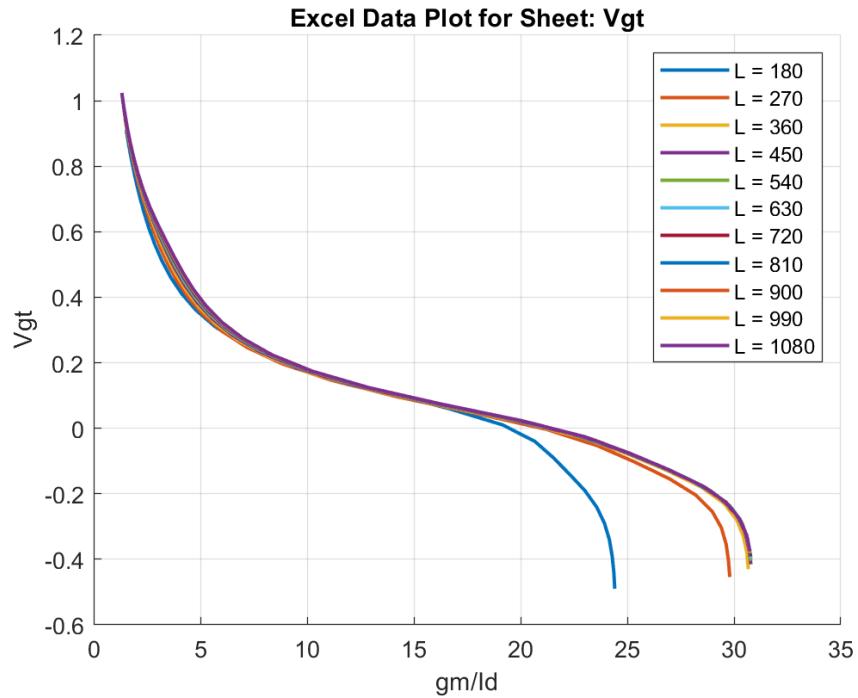
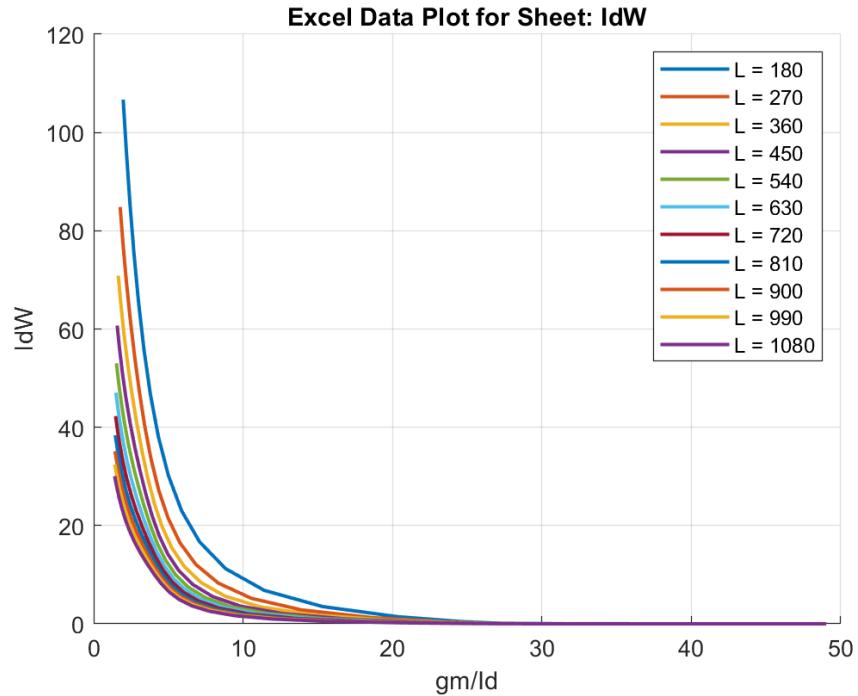


Figure 3: NMOS Techplots after Matlab postprocessing - fT

Figure 4: NMOS Techplots after Matlab postprocessing - V_{gt}

3.2 PMOS Tech Plots

Figure 5: PMOS Techplots after Matlab postprocessing - Id/W

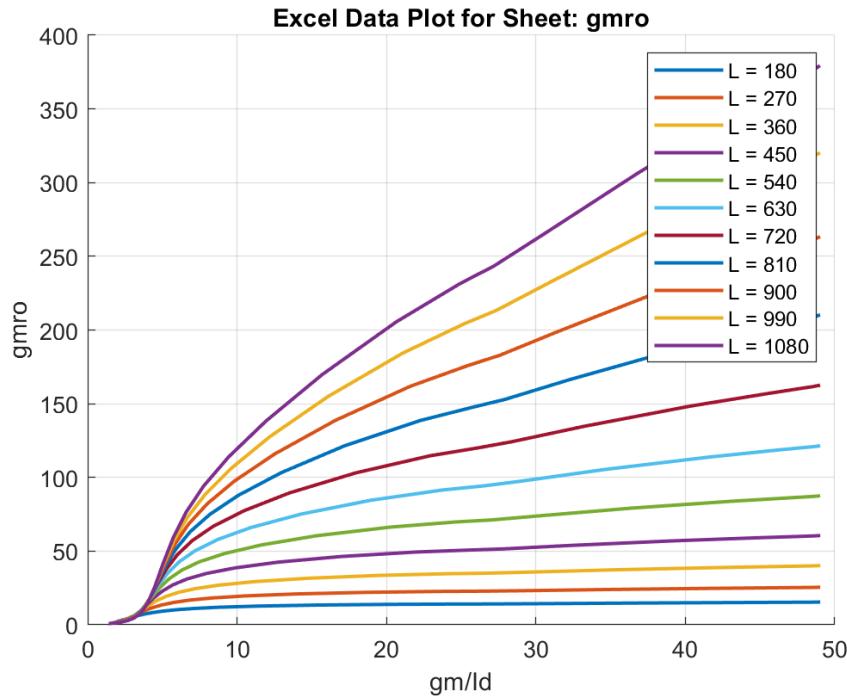


Figure 6: PMOS Techplots after Matlab postprocessing - gmro

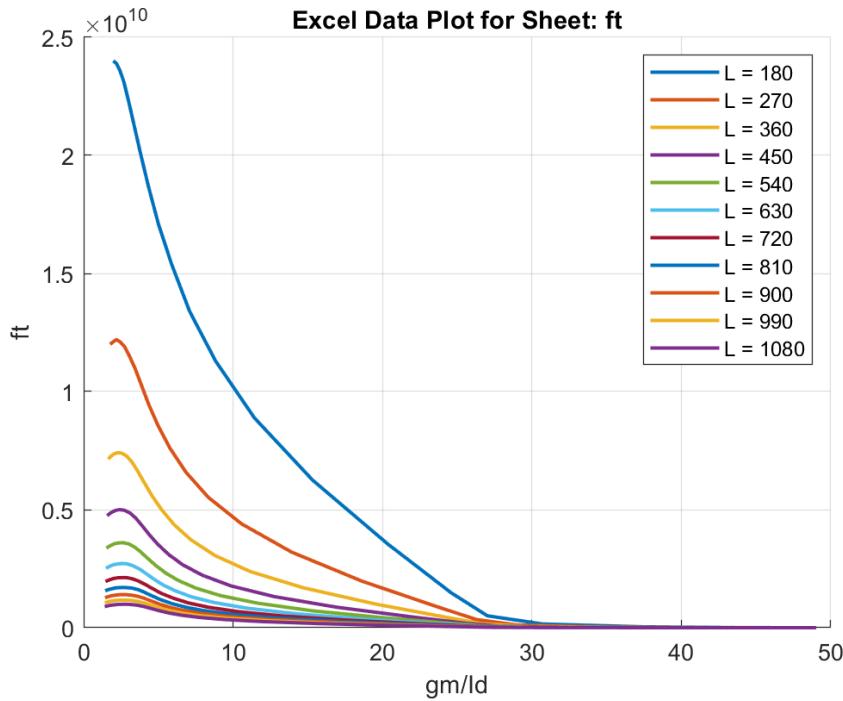


Figure 7: PMOS Techplots after Matlab postprocessing - fT

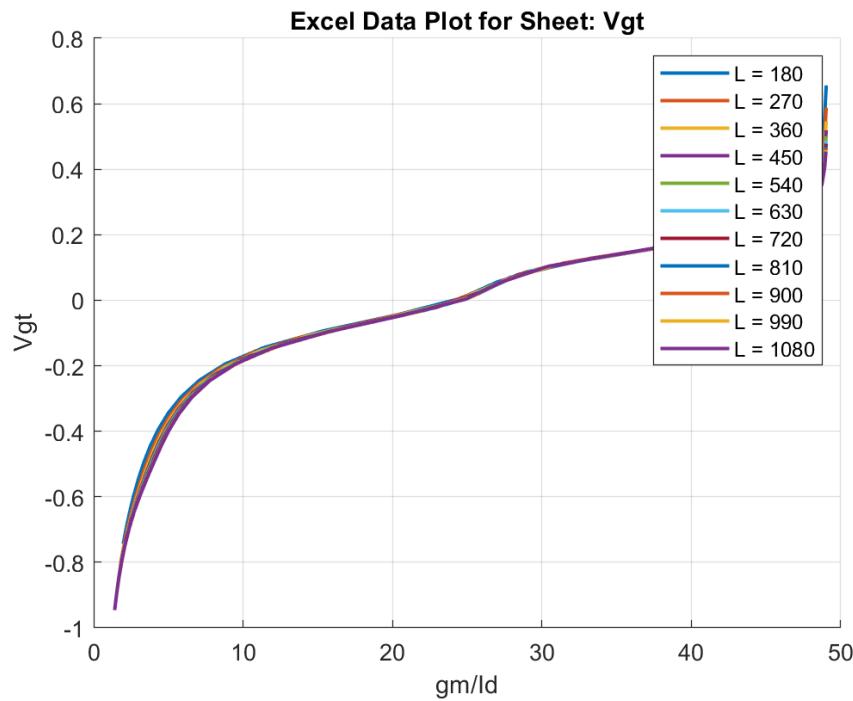


Figure 8: NMOS Techplots after Matlab postprocessing - Vgt

Table 2: Key Differences between 45 nm and our chosen node 90nm for same value of gm/Id

gmro	Value
gpdk090	23
gpdk045 Parameter	62

4 LDO

A Low Dropout Regulator (LDO) is a type of voltage regulator that provides a stable output voltage even when the input voltage is close to the desired output. The primary advantage of an LDO is its ability to operate with a small difference between the input and output voltage, known as the dropout voltage. This makes LDOs particularly useful for applications where the input voltage is only slightly higher than the required output voltage.

LDOs are widely used in battery-powered devices because they can regulate voltage effectively even when the battery voltage is near the required output level. LDOs are often used to power sensitive analog circuits, sensors, microcontrollers, and other low-voltage digital and analog components.

4.1 Characteristics of an LDO

- **Dropout Voltage:** The minimum difference between the input and output voltage required for proper regulation. It is typically in the range of millivolts.
- **Output Voltage:** The regulated voltage provided by the LDO to the load.
- **PSRR (Power Supply Rejection Ratio):** A measure of the LDO's ability to reject input noise and variations at the output.
- **Quiescent Current:** The current consumed by the LDO itself when there is no load connected to the output.

4.2 LDO Operation

An LDO operates by comparing the output voltage with a reference voltage and adjusting the pass element (usually a transistor) to maintain the output voltage at a constant level. The pass element can either be a bipolar junction transistor (BJT) or a metal-oxide-semiconductor field-effect transistor (MOSFET). The feedback loop regulates the transistor's resistance to ensure the output voltage remains stable.

The key equation governing the output voltage of an LDO is:

$$V_{\text{out}} = V_{\text{ref}} + I_{\text{load}} \cdot R_{\text{drop}}$$

Where:

- V_{out} is the output voltage.
- V_{ref} is the reference voltage.
- I_{load} is the load current.
- R_{drop} is the resistance of the pass element.

4.3 LDO Circuit

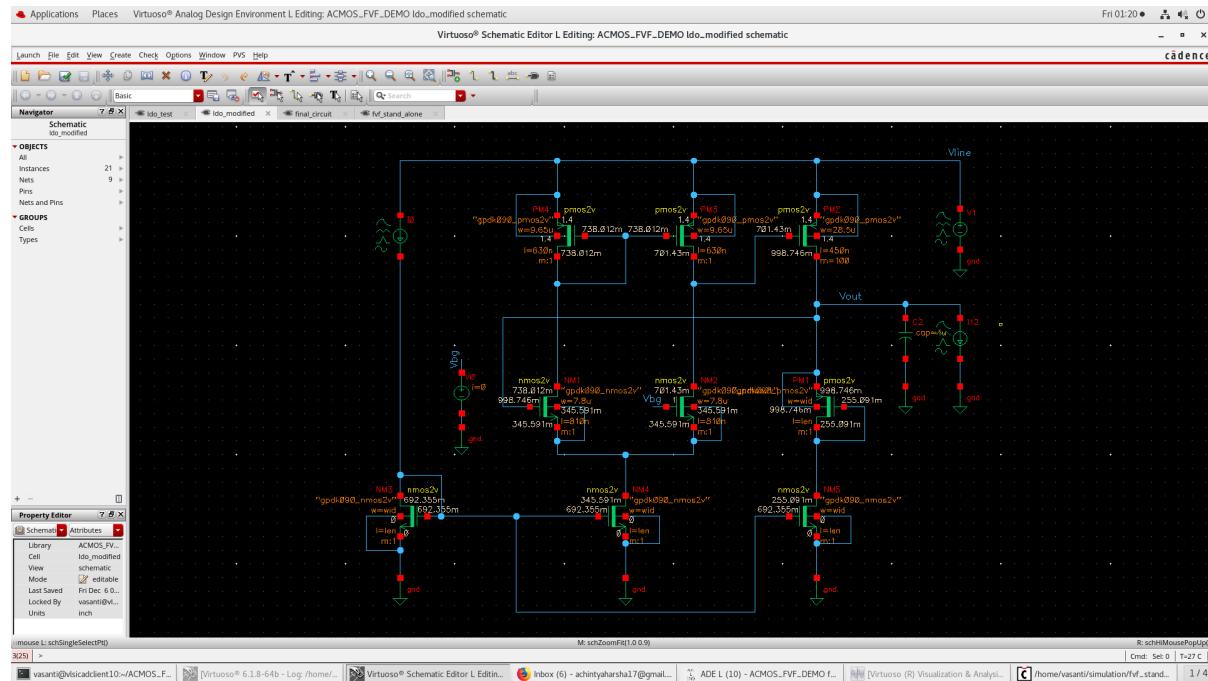


Figure 9: FET sizes and characteristics

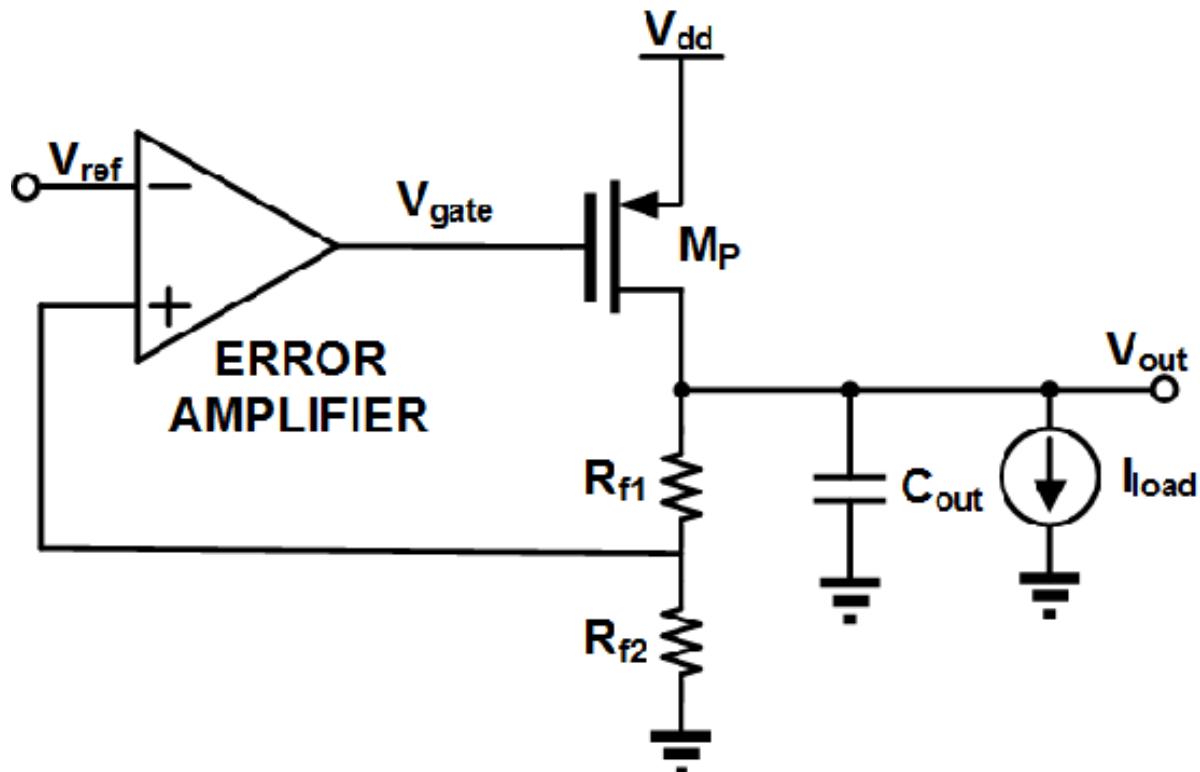


Figure 10: Block Diagram of LDO

4.4 LDO Sizing and Operation

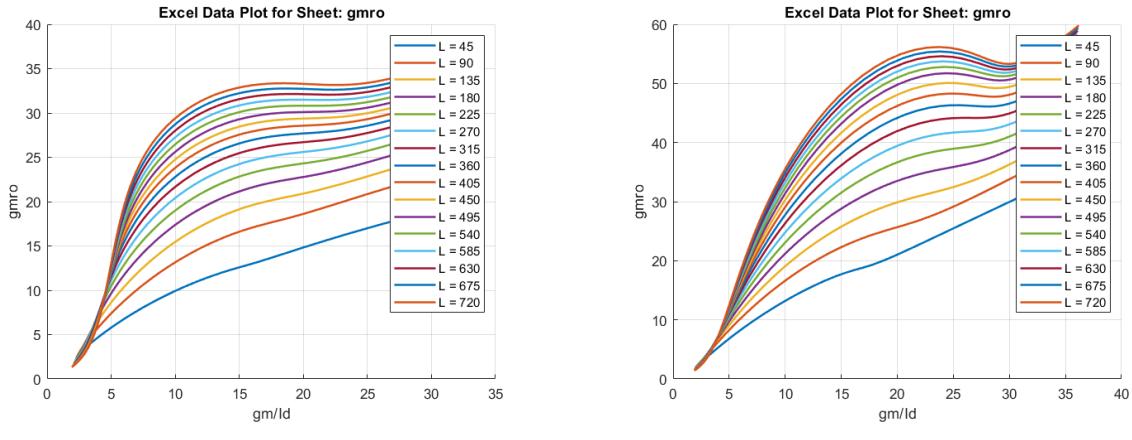
Initially, we were using GPDK045 as our PDK. However, as shown in Figure 11, the technology plots were not able to achieve sufficiently high values of $g_m r_o$ for a given $\frac{g_m}{I_D}$ unless the transistor length was made very large, on the order of microns. This is because:

$$g_m = \frac{2I_D}{V_{ov}}, \quad r_o = \frac{1}{\lambda I_D}$$

Thus:

$$g_m r_o = \frac{2}{\lambda V_{ov}}$$

Since λ is smaller for larger technology nodes, the $g_m r_o$ (intrinsic gain) is higher for larger technology nodes. Hence, we were able to more easily achieve a higher $g_m r_o$ and, consequently, a higher intrinsic gain. As a result, we chose GPDK090.



(a) $g_m r_o$ plot for NMOS.

(b) $g_m r_o$ plot for PMOS.

Figure 11: $g_m r_o$ plots of NMOS and PMOS in 45nm technology.

The table below provides the sizes of the passFET, differential amplifier, and mirror transistors.

Table 3: FET Sizes and Parameters

Transistor	Type	Size (W/L)
PM1	PMOS	10u/720n
PassFET(PM2)	PMOS	2850u/450n
DiffAmp(PM3)	PMOS	9.65u/630n
DiffAmp(PM4)	PMOS	9.65u/630n
DiffAmp(NM0)	NMOS	7.8u/810n
DiffAmp(NM1)	NMOS	7.8u/810n
CurrentMirror(NM3)	NMOS	10u/720n
CurrentMirror(NM4)	NMOS	10u/720n
CurrentMirror(NM5)	NMOS	10u/720n

Mosfet	Vgs (V)	Vgt (V)	Ids (A)	gm (S)	Vds (V)	ro (Ohm)	gmro
PM4	-661.99m	-175.75m	-23.48u	239.05u	-661.99m	289.27K	69.15
PM3	-698.57m	-179.36m	-23.61u	239.98u	-698.57m	289.33K	69.42
PM2	-743.66m	-267.13m	-10.05m	99.68m	-401.25m	388.72	38.75
PM1	-175.55m	-46.19u	-46.19u	327.71	-743.66m	218.43K	71.60
PM5	692.36m	198.83m	46.18u	414.16u	245.57u	84.46K	35.01
NM4	692.36m	199.47m	47.09u	422.39u	244.99u	110.07K	46.48
NM3	692.36m	201.92m	50.00u	441.72u	255.09m	122.27K	54.02
NM2	654.41m	166.57m	23.65u	245.57u	345.59m	248.80K	61.10
NM1	653.16m	165.50m	23.48u	244.99u	355.84m	257.59K	63.15

Table 4: Transistor parameters

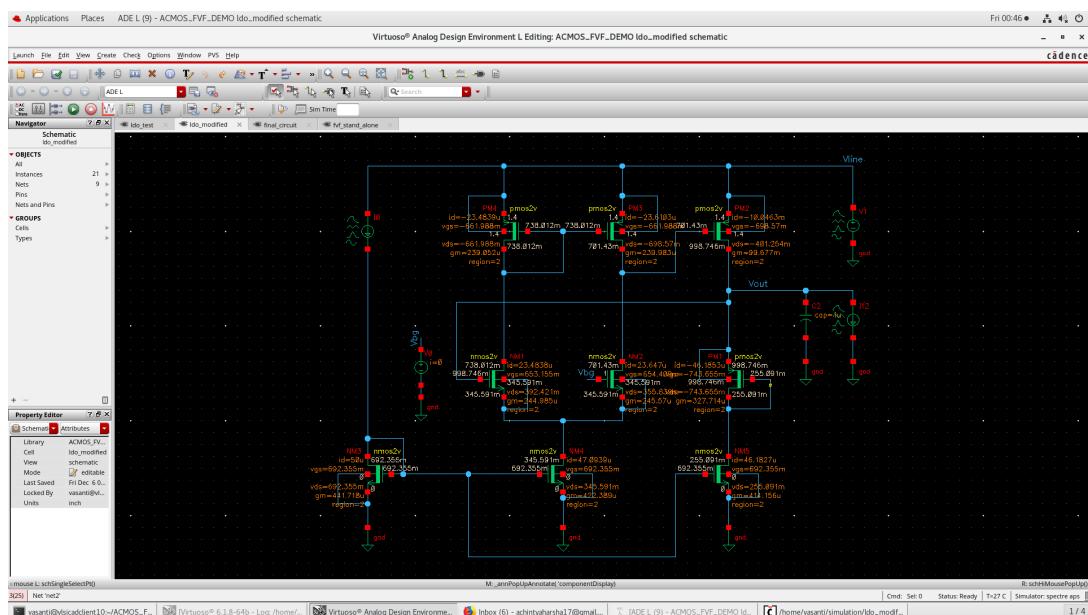


Figure 12: FET DC Operation Point

4.5 Stability Analysis

The pole locations are listed and verified through simulations. Their movement was analyzed concerning the load, and the worst-case phase margin was identified and discussed.

Phase margin is defined as the difference between the phase of the open loop transfer function and -180deg at the frequency where the open loop transfer function is 1.

$$PM = 90 - \tan^{-1}\left(\frac{w_u}{w_{p2}}\right) \quad (1)$$

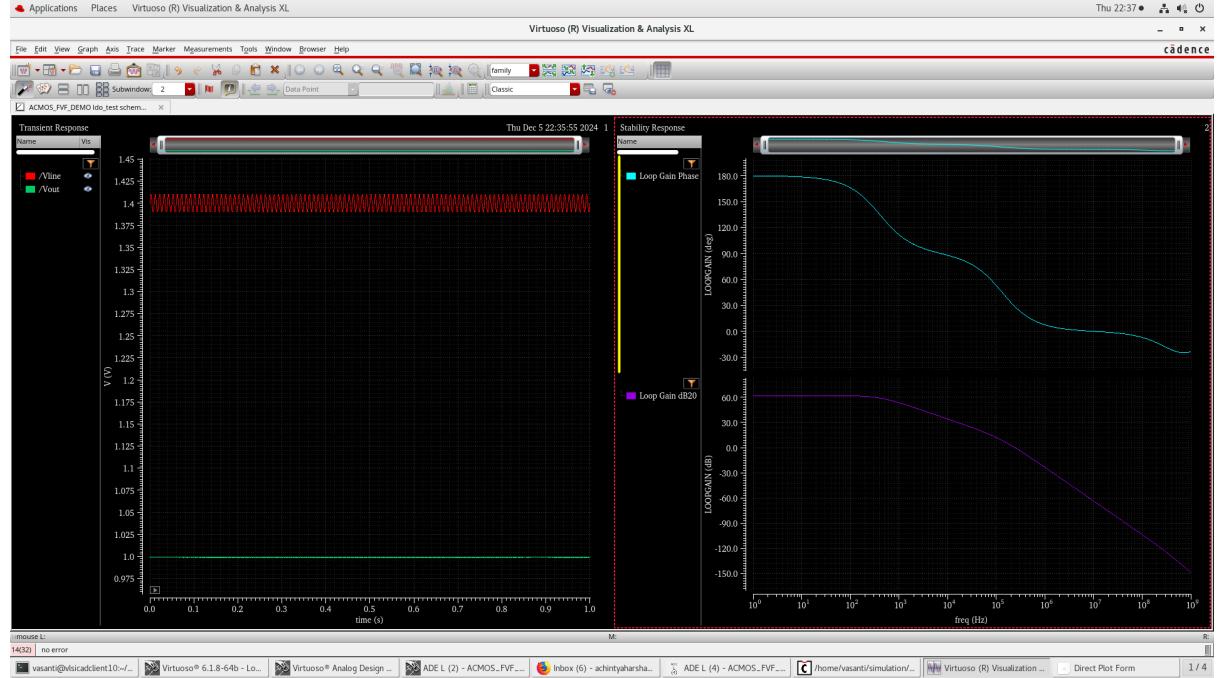


Figure 13: Stability analysis plot.

Table 5: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	62	63.9
Unity Gain Bandwidth (Hz)	981KHz	115kHz
Phase Margin (degrees)	46	59
Pole 1 (Hz)	780Hz	100Hz
Pole 2 (Hz)	1Mhz	125kHz

4.6 DC Loop Gain

4.6.1 Light Load

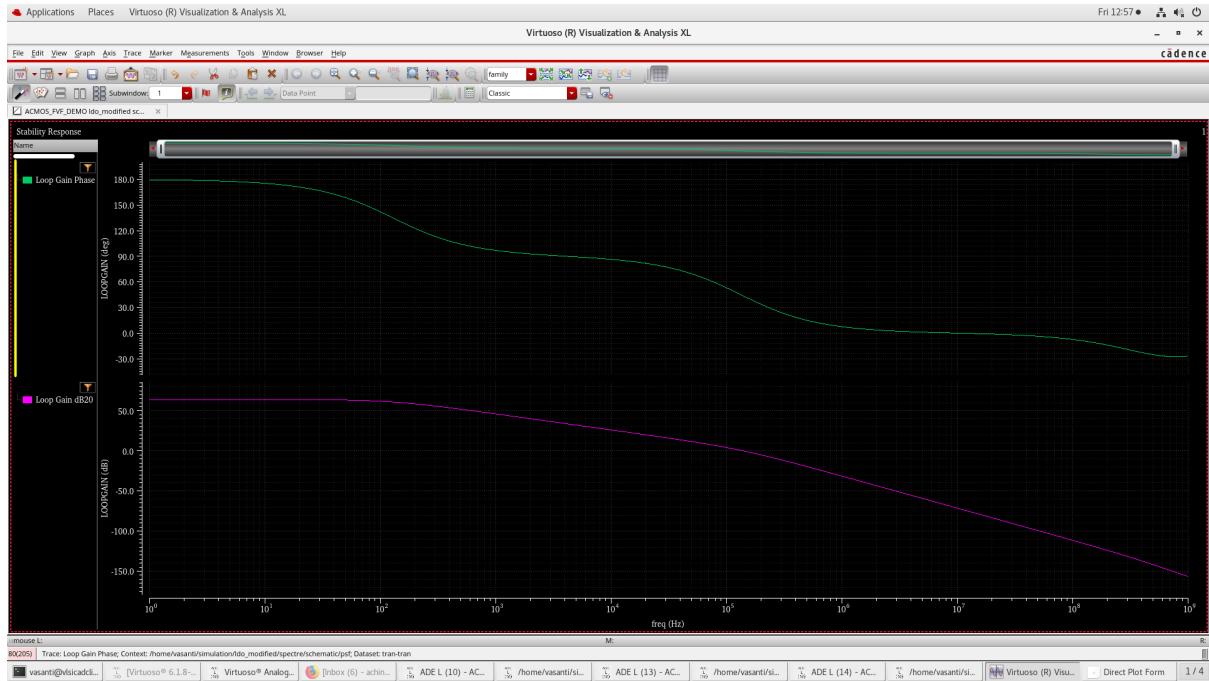


Figure 14: PSRR block diagram.

4.6.2 Heavy Load

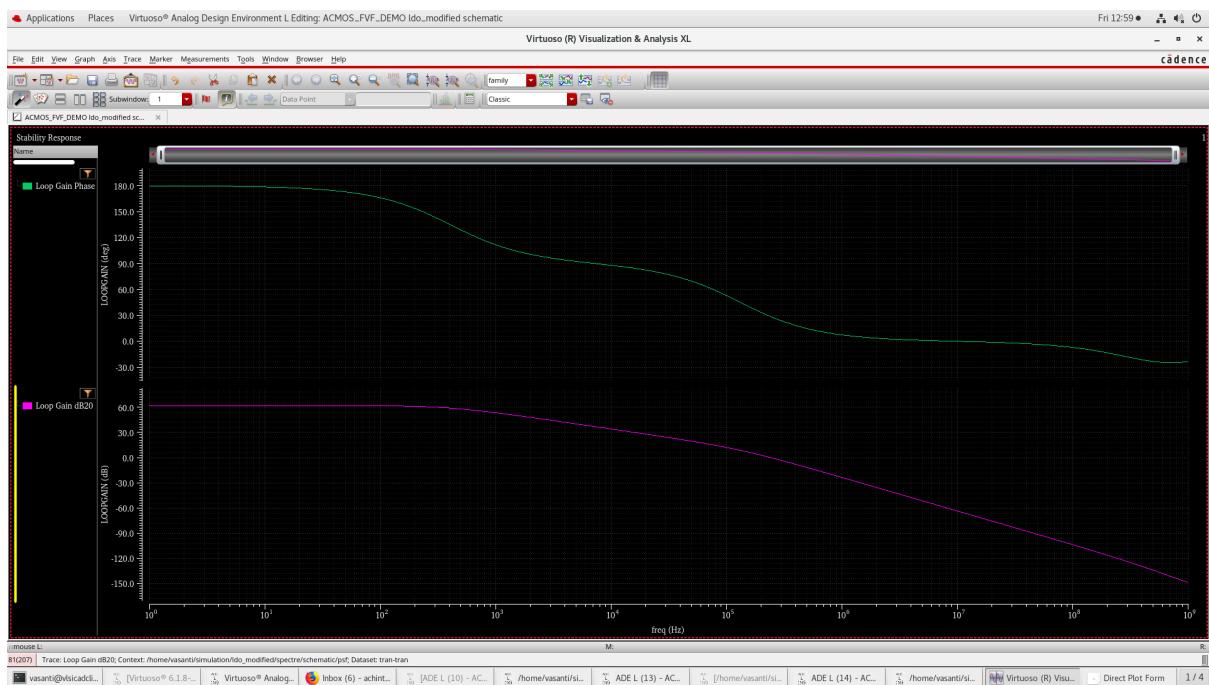


Figure 15: PSRR block diagram.

4.7 PSRR

PSRR (Power Supply Rejection Ratio) in an LDO (Low Dropout Regulator) refers to the ability of the LDO to reject noise or variations from the input power supply. It is defined as the ratio of the change in the input voltage to the corresponding change in the output voltage, typically expressed in decibels (dB). The formula for PSRR is:

$$\text{PSRR} = 20 \log \left(\frac{\Delta V_{\text{line}}}{\Delta V_{\text{out}}} \right)$$

Where:

- ΔV_{line} is the change in the input voltage (noise or variation).
- ΔV_{out} is the corresponding change in the output voltage.

4.7.1 PSRR Simulation Results

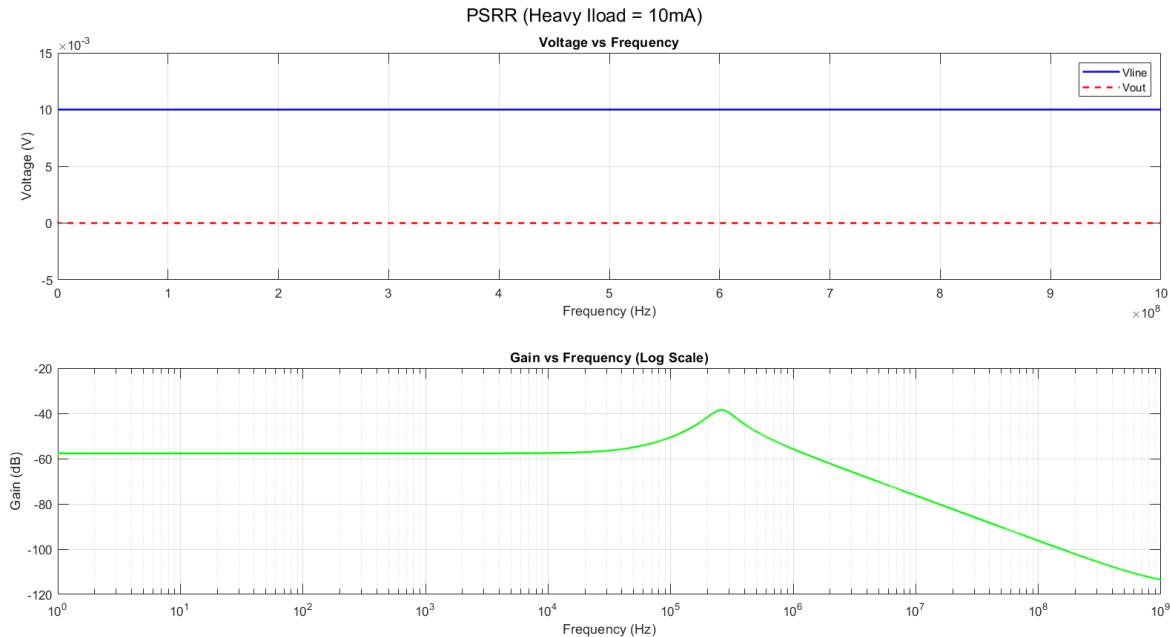


Figure 16: PSRR simulation results - heavy load.

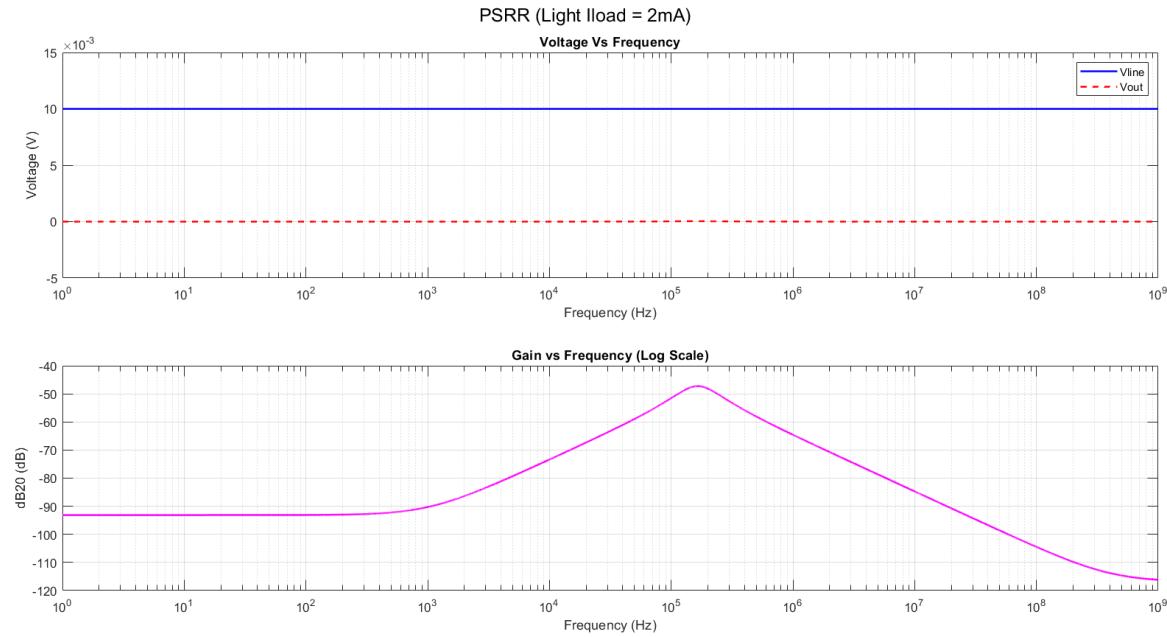


Figure 17: PSRR simulation results - light load.

4.8 Transient Simulation Results

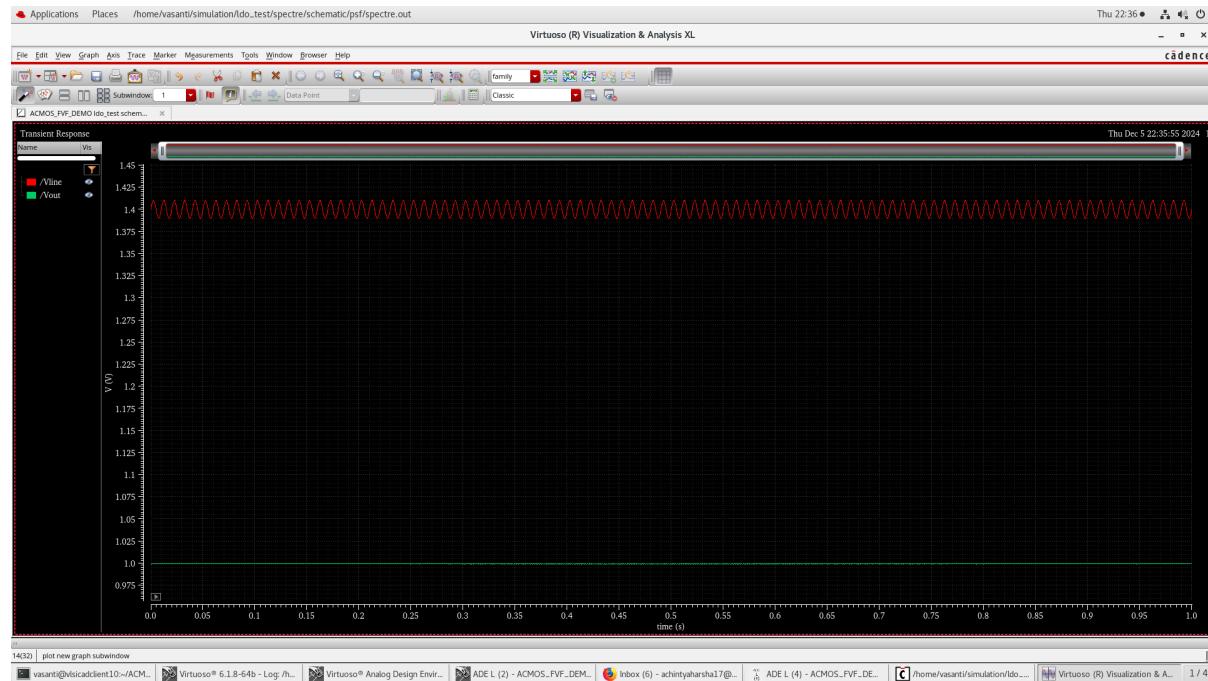


Figure 18: Transient simulation results.

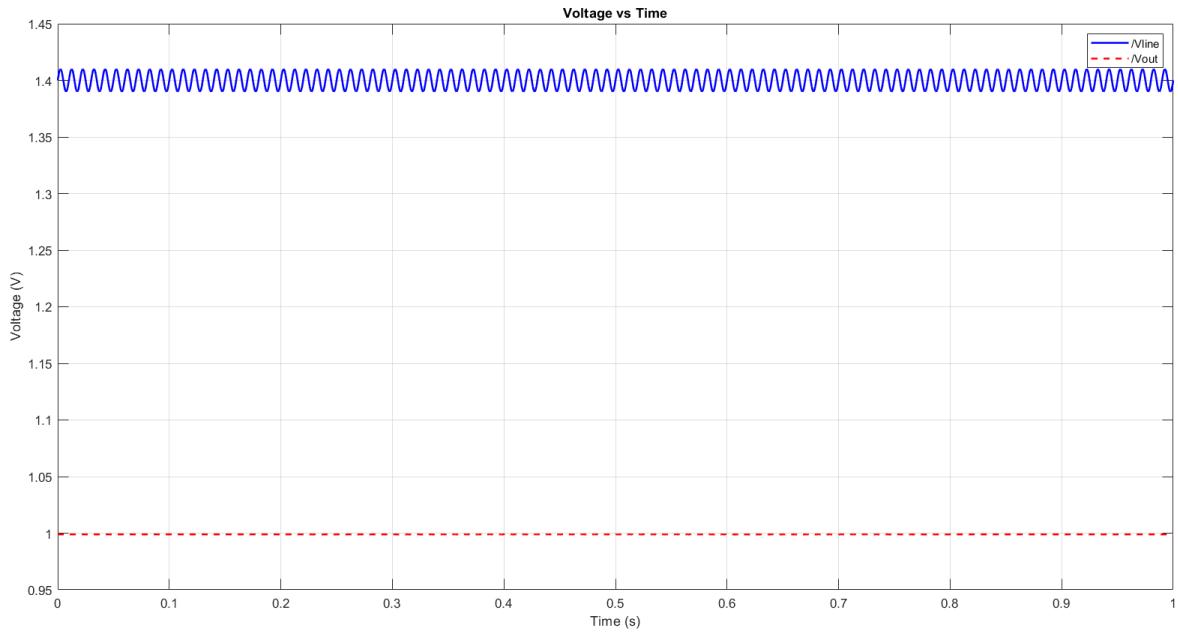


Figure 19: Transient response on Matlab.

4.9 Simulation vs. Hand Calculations

Table 6: Simulation vs. Hand Calculations

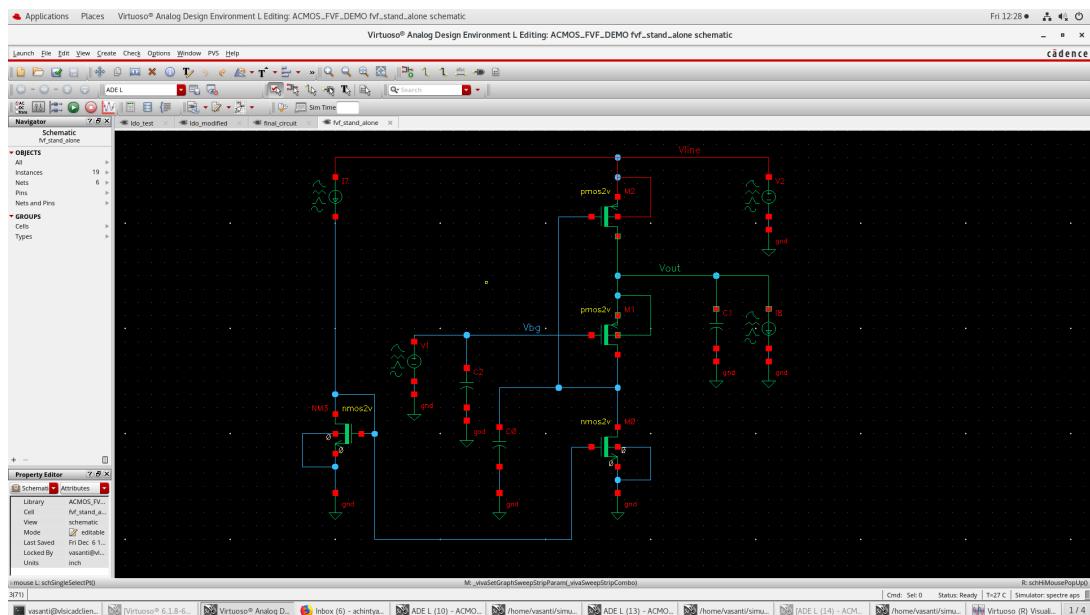
Parameter	Simulation	Hand-Calculation
Heavy Load Loop Gain (dB)	62	60
Light Load Loop Gain (dB)	63.9	60
Heavy Load PSRR (dB)	58.9	60
Light Load PSRR (dB)	92	60
Heavy Load Phase Margin (degrees)	46.1	77.21
Light Load Phase Margin (degrees)	59	59.15
Heavy Load Unity Gain Bandwidth (Hz)	981kHz	1.1Mhz
Light Load Unity Gain Bandwidth (Hz)	115kHz	200kHz

5 Flipper Voltage Follower

A flipped voltage follower (FVF) is a compact analog circuit configuration used for low output impedance and high current drive. It operates by applying the input voltage to the gate of a MOSFET, with feedback ensuring the source voltage follows the input. A current source biases the circuit, making it suitable for voltage references, operational amplifier output stages, and driving capacitive loads. It offers high slew rate, low power consumption, and efficient current buffering.

5.1 Standalone FVF Circuit

The Flipped Voltage Follower (FVF) circuit was designed and optimized separately from the Low-Dropout Regulator (LDO), with each being sized independently. To connect these two components, a PMOS-based current mirror topology is utilized.



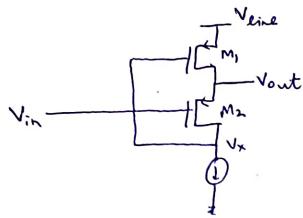
5.1.1 Fast Loop Correction

Since the FVF also relies on a MOSFET operating in the saturation region, the current mirror ensures that the source of the MOSFET matches $V_{LDO,Out}$. The FVF's fast feedback loop quickly compensates for any changes in $V_{LDO,Out}$, maintaining the stability and precision of V_{Out} .

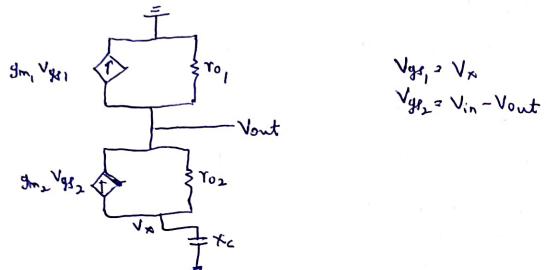
5.2 Analysis

To characterize the FVF we have to find the gain and the psrr of the fvf and to size it to wrk optimally.

5.2.1 Closed loop gain



Small signal model:



$$\text{KCL: } \frac{V_{out}}{R_{o1}} + \frac{V_{out} - V_x}{R_{o2}} + g_{m_1} V_{gs_1} - g_{m_2} V_{gs_2} = 0$$

$$\frac{V_{out}}{R_{o1}} + \frac{V_{out}}{R_{o2}} - \frac{V_x}{R_{o2}} + g_{m_1} V_x - g_{m_2} V_{in} + g_{m_2} V_{out} = 0$$

$$V_{out} \left[\frac{1}{R_{o1}} + \frac{1}{R_{o2}} + g_{m_2} \right] - V_x \left[\frac{1}{R_{o2}} - g_{m_1} \right] - V_{in} g_{m_2} = 0 \quad \text{--- (1)}$$

$$\text{KCL: } \frac{V_x - V_{out}}{R_{o2}} + \frac{V_x}{X_C} + g_{m_2} V_{gs_2} = 0$$

$$\frac{V_x - V_{out}}{R_{o2}} + \frac{V_x}{X_C} + g_{m_2} (V_{in} - V_{out}) = 0$$

$$V_x \left[\frac{1}{R_{o2}} + \frac{1}{X_C} \right] - V_{out} \left[\frac{1}{R_{o2}} + g_{m_2} \right] + g_{m_2} V_{in} = 0 \quad \text{--- (2)}$$

$$\text{--- (1) + (2) ---} \quad \frac{V_{out}}{R_{o1}} + V_x \left[\frac{1}{X_C} + g_{m_1} \right] = 0$$

$$-\frac{V_{out}}{R_{o1}} = V_x \left[\frac{1}{X_C} + g_{m_1} \right]$$

$$\therefore V_x = \frac{-V_{out}}{R_{o1} \left[\frac{1}{X_C} + g_{m_1} \right]}$$

$$(1) \Rightarrow V_{out} \left[\frac{1}{R_{o1}} + \frac{1}{R_{o2}} + g_{m_2} \right] + \frac{V_{out} \left[\frac{1}{R_{o2}} - g_{m_1} \right]}{R_{o1} \left[\frac{1}{X_C} + g_{m_1} \right]} - V_{in} g_{m_2} = 0$$

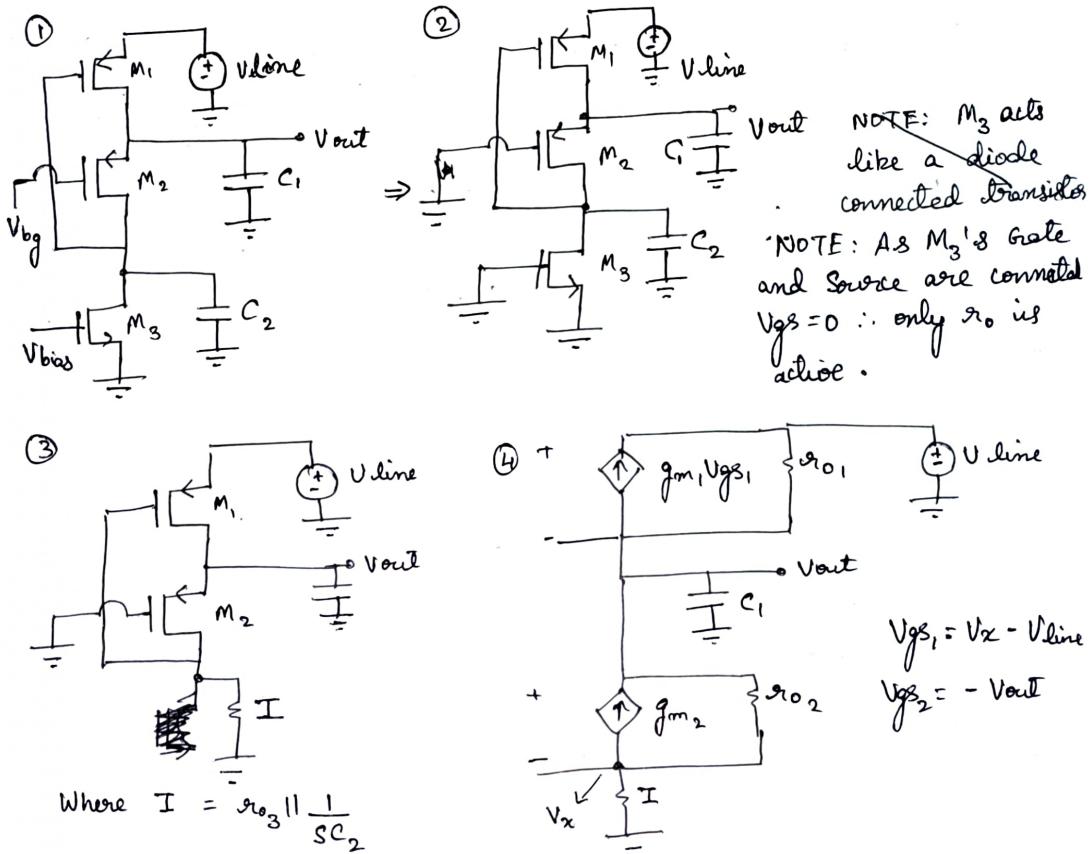
$$V_{out} \left[\frac{1}{R_{o1}} + \frac{1}{R_{o2}} + g_{m_2} + \frac{1}{R_{o1} \left[g_{m_1} + \frac{1}{X_C} \right]} \left[\frac{1}{R_{o2}} - g_{m_1} \right] \right] = V_{in} g_{m_2}$$

$$\begin{aligned}
 \frac{V_{out}}{V_{in}} &= \frac{g_{m_2}}{\left[\frac{1}{r_{o_1}} + \frac{1}{r_{o_2}} + g_{m_2} + \frac{1}{r_{o_1}(g_{m_1} + \frac{1}{X_C})} \left(\frac{1}{r_{o_2}} - g_{m_2} \right) \right]} \\
 &= \frac{g_{m_2} r_{o_1}}{1 + \frac{r_{o_1}}{r_{o_2}} + g_{m_2} r_{o_1} + \frac{1}{(g_{m_1} + \frac{1}{X_C})} \left(\frac{1}{r_{o_2}} - g_{m_2} \right)} \\
 &= \frac{+g_{m_2} r_{o_1} r_{o_2}}{r_{o_2} + r_{o_1} + g_{m_2} r_{o_1} r_{o_2} + \frac{(1-g_{m_2} r_{o_2})}{(g_{m_1} + \frac{1}{X_C})}} \\
 &= \frac{+g_{m_2} r_{o_1} r_{o_2} (g_{m_1} + \frac{1}{X_C})}{(g_{m_1} + \frac{1}{X_C}) (r_{o_1} + r_{o_2} + g_{m_2} r_{o_1} r_{o_2}) + (1-g_{m_2} r_{o_2})} \\
 &\approx \frac{+g_{m_2} r_{o_1} r_{o_2} (g_{m_1} + \frac{1}{X_C})}{(g_{m_1} + \frac{1}{X_C}) (g_{m_2} r_{o_1} r_{o_2}) + (1-g_{m_2} r_{o_2})} \\
 &\approx \frac{g_{m_2} r_{o_1} r_{o_2} (g_{m_1} + \frac{1}{X_C})}{(g_{m_1} + \frac{1}{X_C}) g_{m_2} r_{o_1} r_{o_2}}
 \end{aligned}$$

$$\frac{V_{out}}{V_{in}} \approx 1$$

5.2.2 PSRR of an FVF

PSRR calculation for FVF:



$\Rightarrow KCL$ at V_{out}

$$\frac{V_{out} - V_{line}}{r_{o1}} + g_{m1} V_{gs1} + V_{out} SC_1 + \frac{V_{out} - V_x}{r_{o2}} - g_{m2} V_{gs2} = 0$$

$$\frac{V_{out} - V_{line}}{r_{o1}} + g_{m1} V_x - g_{m1} V_{line} + \frac{V_{out} - V_x}{r_{o2}} + V_{out} g_{m2} = 0$$

$$V_{out} \left[\frac{1}{r_{o1}} + SC_1 + \frac{1}{r_{o2}} + g_{m2} \right] - V_{line} \left[\frac{1}{r_{o1}} + g_{m1} \right] + V_x \left[g_{m1} - \frac{1}{r_{o2}} \right] = 0$$

$\Rightarrow KCL$ at V_x .

$$\frac{V_x - V_{out}}{r_{o2}} + \frac{V_x}{I} - g_{m2} V_{out} = 0$$

$$\therefore V_x = \frac{V_{out} \left[g_{m2} + \frac{1}{r_{o2}} \right]}{\frac{1}{I} + \frac{1}{r_{o2}}} \rightarrow ②$$

Put ② in ①

$$\frac{V_{out}}{V_{line}} \left[\frac{1}{g_{o_1}} + SC_1 + \frac{1}{g_{o_2}} + g_{m_2} \right] = V_{line} \left[\frac{1}{g_{o_1}} + g_{m_1} \right] + \frac{V_{out} \left[g_{m_2} + \frac{1}{g_{o_2}} \right] \left[g_{m_1} - \frac{1}{g_{o_2}} \right]}{\frac{1}{I} + \frac{1}{g_{o_2}}} = 0$$

$$\therefore V_{out} \left[\frac{1}{g_{o_1}} + SC_1 + \frac{1}{g_{o_2}} + g_{m_2} + \frac{\left(g_{m_2} + \frac{1}{g_{o_2}} \right) \left(g_{m_1} - \frac{1}{g_{o_2}} \right)}{\frac{1}{I} + \frac{1}{g_{o_2}}} \right] = V_{line} \left[\frac{1}{g_{o_1}} + g_{m_1} \right]$$

$$\text{Now } g_m \gg \frac{1}{g_o}$$

$$\therefore V_{out} \left[SC_1 + g_{m_2} + \frac{g_{m_2} g_{m_1}}{\frac{1}{g_{o_3}} + SC_2 + \frac{1}{g_{o_2}}} \right] = V_{line} \left[g_{m_1} \right]$$

$$\text{Now at low freq., } s \rightarrow 0$$

$$V_{out} g_{m_2} \left[1 + \frac{g_{m_1}}{\frac{1}{g_{o_3}} + \frac{1}{g_{o_2}}} \right] = V_{line} g_{m_1}$$

$$V_{out} g_{m_2} \left[1 + g_{m_1} (g_{o_3} \parallel g_{o_2}) \right] = V_{line} g_{m_1}$$

$$\therefore V_{out} g_{m_2} g_{m_1} (g_{o_3} \parallel g_{o_2}) = V_{line} g_{m_1}$$

$$\boxed{\frac{V_{out}}{V_{line}} = \frac{1}{g_{m_2} (g_{o_3} \parallel g_{o_2})}}$$

Now if required PSRR = x dB, then

$$20 \log \left(\frac{V_{out}}{V_{line}} \right) = x$$

$$\therefore 10^{x/20} = \frac{1}{g_{m_2} (g_{o_3} \parallel g_{o_2})}$$

Ex: If $x = -60$ dB

$$\text{Then } \underline{\underline{g_{m_2} (g_{o_3} \parallel g_{o_2})}} = 10^3$$

5.3 FVF Sizing

As demonstrated in the previous derivation, achieving a $g_m r_o$ magnitude of 10^3 is not feasible for a single-stage circuit, according to the technology plot. However, a 30 dB PSRR can be achieved with ease.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{g_{m2} \cdot (r_{o2} \parallel r_{o3})}$$

$$20 \log \left(\frac{V_{\text{in}}}{V_{\text{out}}} \right) = 30 \text{ dB}$$

$$\frac{V_{\text{in}}}{V_{\text{out}}} = 10^{1.5}$$

$$g_{m2} \cdot (r_{o2} \parallel r_{o3}) = 31.62$$

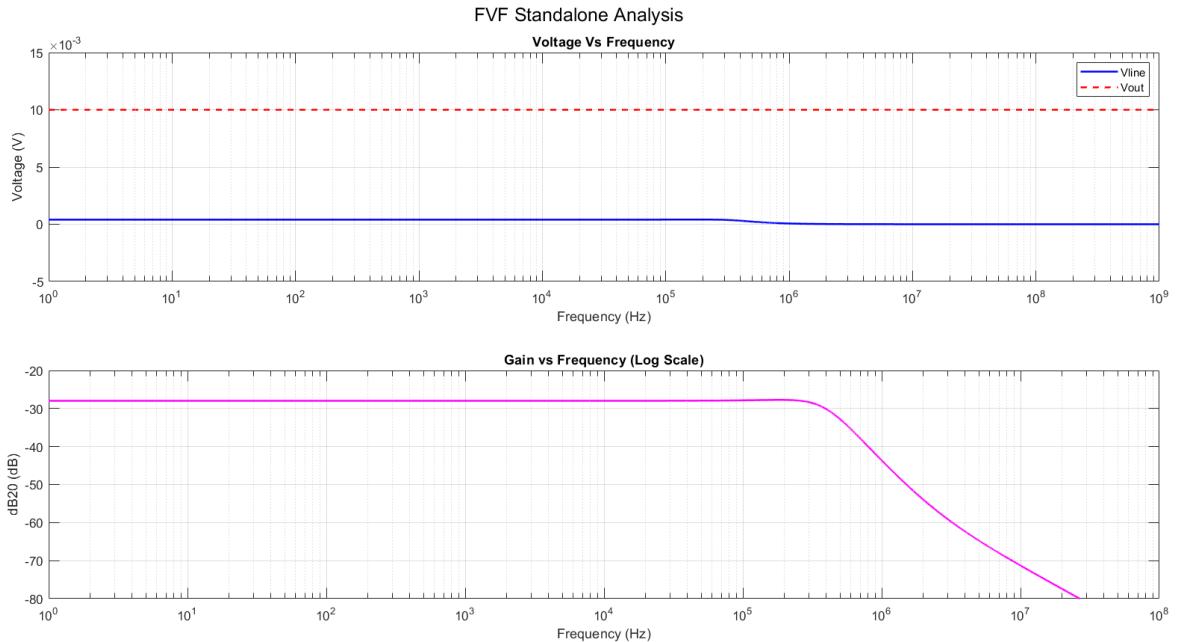
Approximately, $g_{m2} \cdot r_{o2} = 63$

This can be increased by using a Folded Cascode FVF circuit. This has been discussed in the second part of the paper.

Using these values and the tech plots, we were able to size the FVF appropriately. It is important to note that the sizing of the pass transistor does not contribute to the PSRR of the FVF. Therefore, it only needs to be sized large enough to support the load current, ensuring all transistors remain in saturation.

5.4 Simulation Outputs

5.4.1 PSRR

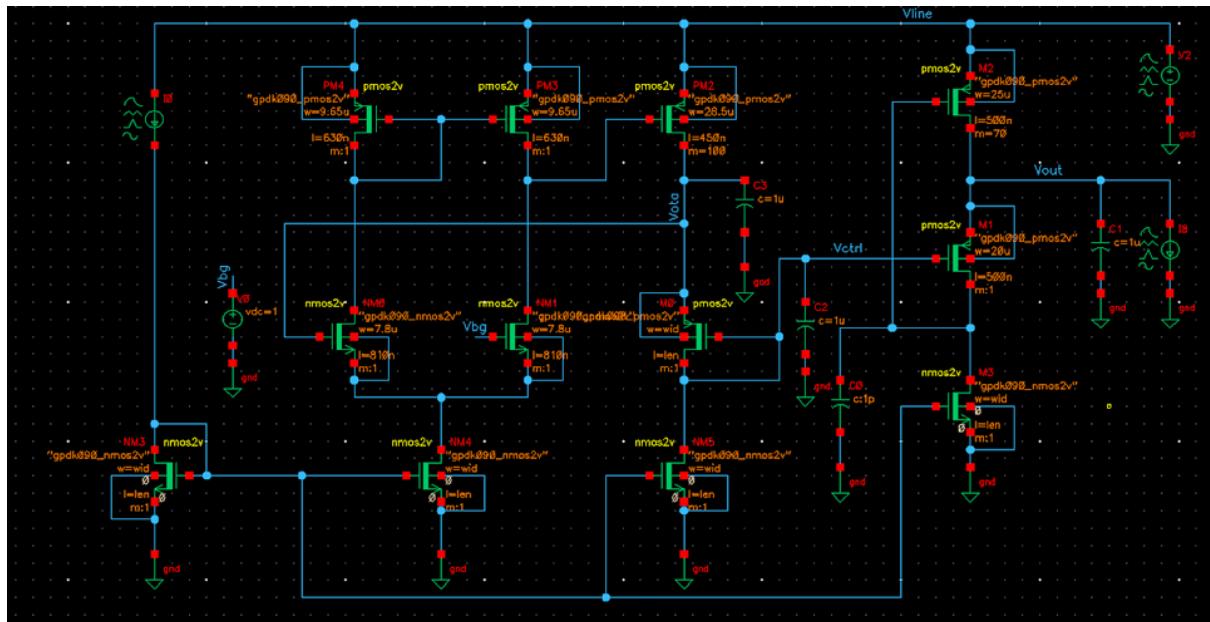


5.4.2 Transient Response



6 LDO Integration with FVF

6.1 Main Circuit



6.1.1 Current Mirror Operation

In the current mirror configuration, the output voltage of the LDO ($V_{LDO,out}$) is applied to the source of the PMOS transistor in the current mirror. Since this PMOS is operating

in the saturation region, the source-gate voltage (V_{SG}) of the PMOS transistor can be expressed as:

$$V_{SG} = V_{LDO,Out} - V_{Ctrl}$$

where:

- $V_{LDO,Out}$: Output voltage of the LDO.
- V_{Ctrl} : Control voltage of the PMOS gate.

6.1.2 Key Equations

1. Source-Gate Voltage Relation for PMOS at LDO side:

$$V_{SG} = V_{LDO,Out} - V_{Ctrl}$$

2. Source-Gate Voltage Relation for PMOS at FVF side:

$$V_{SG} = V_{Out} - V_{Ctrl}$$

3. LDO Equation:

$$V_{BG} = V_{LDO,Out}$$

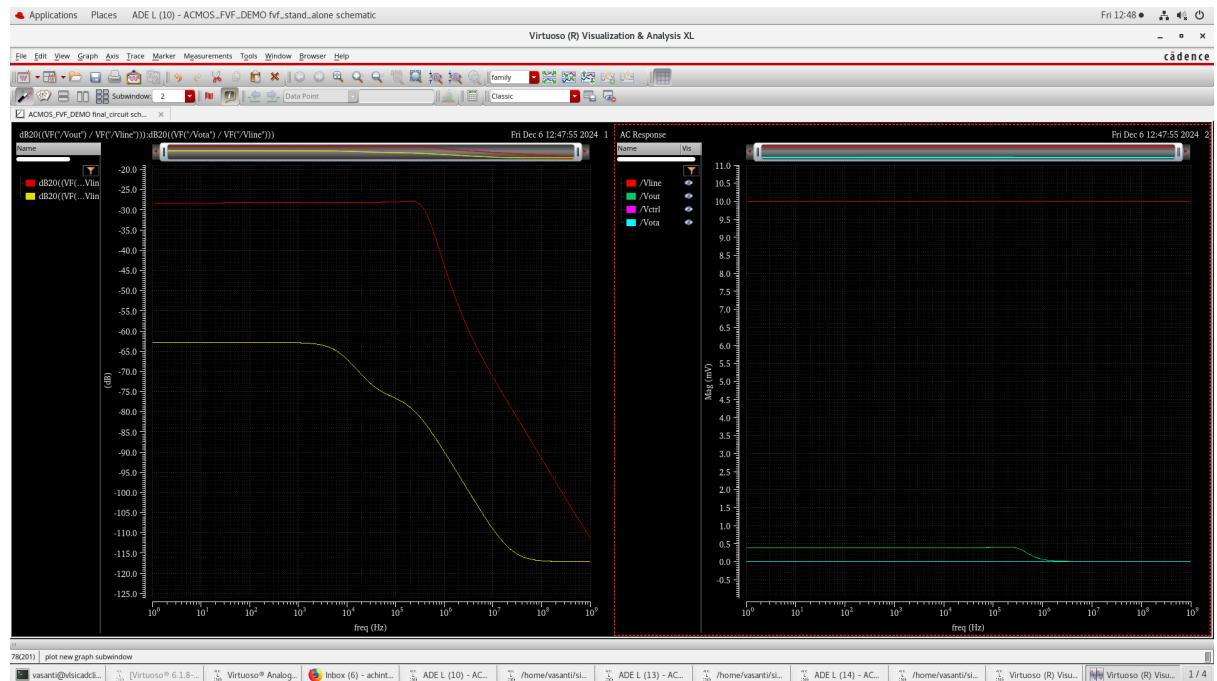
4. Feedback Correction by FVF:

Any deviation in $V_{LDO,Out}$ activates a fast feedback loop in the FVF, restoring V_{Out} to its nominal value. The FVF ensures that V_{Out} matches the reference bandgap voltage V_{BG} maintained by the LDO.

$$V_{Out} = V_{BG}$$

6.2 Simulation Results

6.2.1 PSRR



6.2.2 Transient Response

