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# Flipped Voltage Follower Low Dropout (LDO) Voltage Regulators: A Tutorial Overview

(Invited Tutorial)

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***Abstract*—This tutorial introduces flipped voltage follower (FVF) based low dropout voltage regulators (LDOs) and their recent advances in the literature. Conventional stand-alone LDO ICs often deploy an external output capacitor in the range of hundreds of nanofarads to tens of microfarads with an inherent equivalent series resistance (ESR) in order to attain stability and low overshoot and undershoot during load transients. Because of the large value of the output capacitor, the bandwidth of the LDO is often limited, thus limiting the power supply rejection ratio (PSRR). Higher SoC integration and the necessity to reduce bill of materials cost has resulted in the proliferation of low-value on-chip capacitor LDOs. One of the major requirements of on-chip capacitor LDOs is to achieve high bandwidth and, thereby, good PSRR.**

**An FVF is an analog voltage buffer circuit with fast local feedback, resulting in high bandwidth. It is capable of sourcing heavy current loads, which makes it an ideal candidate for LDOs. The architecture and design details, such as pole-zero equations, stability, and output impedance, of FVF LDOs are dealt with in detail in this tutorial.**

***Index Terms*—Low dropout voltage regulators (LDOs), Flipped voltage follower (FVF), common-drain transistor amplifier, pole-zero analysis, stability, output impedance, PSRR.**

## I. Introduction

The objective of this paper is to elucidate the basic architecture and some of the recent advances in flipped voltage follower (FVF) based low dropout voltage regulators (LDOs). FVF LDOs are also compared to conventional multi-stage LDO architectures.

### A. Conventional Output Dominant Pole LDO

Conventional stand-alone LDO ICs require a huge off-chip output capacitor $C_{OUT}$ in the range of hundreds of nanofarads to tens of microfarads in order to attain stability and low overshoot and undershoot during load transients [1]–[14]. $C_{OUT}$ creates a load tracking low-frequency dominant pole, whereas a non-dominant pole is created at the gate of the pass transistor. The equivalent series resistance (ESR) of the off-chip output capacitor $R_{ESR}$ creates a left-half-plane (LHP) zero, which helps in cancelling the non-dominant pole and improve the stability of the LDO. Because of the high output capacitor value, the bandwidth of the LDO is lower and the transient response is slow.

In a closed-loop system, power supply rejection ratio (PSRR) is proportional to the open-loop gain of the system, to a first order. In conventional LDOs, the DC open-loop gain is high; therefore, the low frequency PSRR is high. Because of the LDO's low bandwidth, the PSRR begins to drop at a low frequency [13]. Beyond the unity gain frequency (UGF), where the open-loop gain is less than unity, the PSRR depends on the output capacitor $C_{OUT}$ alone.

In modern systems the usage of high switching frequency DC-DC converters are increasing in order to reduce the size of the passive elements. These switching converters convert the main variable supply to a regulated voltage and thereafter multiple LDOs are used to generate a quieter low-ripple supply voltage to several points-of-load (POLs). Therefore, LDOs are often required to have good PSRR at high frequencies in order to attenuate the high-frequency switching noise introduced by the DC-DC converters.

Most circuits in portable applications operate with low input supply voltage $V_{LINE}$. Therefore, POL supply generators operating with low-voltage headroom are gaining importance. Due to bill of materials (BOM) cost, size and integration requirements, SoC designers are restricted to architectures which require fewer off-chip components and input-output (IO) pins. Integrated on-chip capacitor LDOs satisfy these demands [15]–[21].

### B. Integrated On-Chip Capacitor LDO with Internal Dominant Pole

The architecture of an integrated on-chip output capacitor LDO is shown in Fig. 1. It consists of a bandgap reference, an

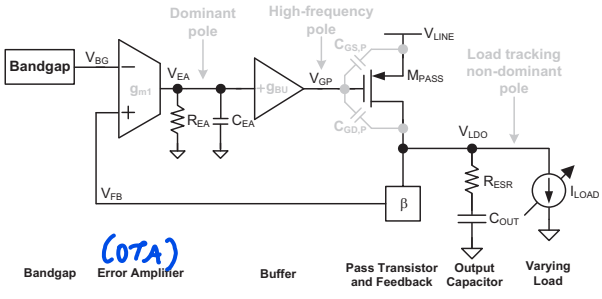


Fig. 1: On-chip capacitor LDO architecture with internal dominant pole situated at the output of error amplifier $g_{m1}$.

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operational transconductance amplifier (OTA) with transconductance $g_{m1}$, cascaded with a buffer $g_{BU}$ driving the gate of a pass transistor $M_{PASS}$. The scaled output voltage $V_{FB}$ is fed back to the OTA in a negative feedback loop that regulates the output voltage $V_{LDO}$ based on the bandgap voltage $V_{BG}$ and scale factor $\beta$. The regulation of the LDO output voltage depends on the open-loop gain. Since the LDO drives heavy output loads, the gain of the output-stage common-source amplifier created by $M_{PASS}$ is low. Therefore, the input-stage OTA needs to have high gain in order to achieve a high loop gain, even at heavy loads [5], [22]. In addition, high loop bandwidth helps reduce the load transient overshoot and undershoot and allows the LDO output to settle faster.

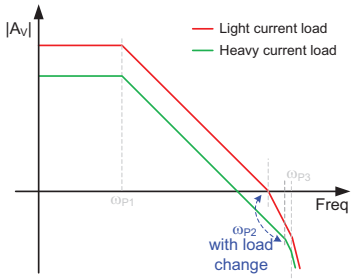


Fig. 2: Frequency magnitude response illustration of an integrated on-chip capacitor LDO of Fig. 1 with pole-zero locations for light and heavy load current conditions. Not drawn to scale.

The pole associated with the output node is non-dominant and tracks with the load. The gate capacitance associated with $M_{PASS}$ is often high. Depending on the resistance at node $V_{GP}$, the pole associated with that node could become a low frequency dominant pole, limiting the bandwidth. Inserting a buffer $g_{BU}$ with a low output impedance moves the pole associated with the gate of the $M_{PASS}$ to high frequencies [5], [9]. Due to the low input capacitance of $g_{BU}$, the dominant pole associated with the output node of the OTA, $V_{EA}$ moves to a higher frequency, resulting in an overall bandwidth increase. The location of poles and zeros for heavy and light load conditions are illustrated in Fig. 2. Since the bandwidth of the on-chip capacitor LDO is increased, the PSRR is high at low and moderate frequencies, but still low at higher frequencies, limiting this LDO's usage for wide-band applications.

## II. Flipped Voltage Follower LDO Architectures

A flipped voltage follower (FVF) is a voltage buffer, with lower output impedance compared to its common-drain transistor amplifier counterpart [1], [23], [24]. A PMOS FVF has large current sourcing capability with low-voltage dropout from $V_{LINE}$ to $V_{LDO}$ and, hence, is an ideal candidate for LDO implementation [1], [22], [25]–[32].

The schematic of an FVF LDO is shown in Fig. 3. The FVF LDO architecture comprises a bandgap circuit (not shown), which generates $V_{BG}$, control voltage $V_{CTRL}$ generation circuitry, PMOS pass transistor $M_{PASS}$, FVF control transistor $M_C$ and bias current $I_{B\_LDO}$. $V_{CTRL}$ drives the gate of $M_C$. The output of the FVF LDO $V_{LDO}$ is obtained at the source

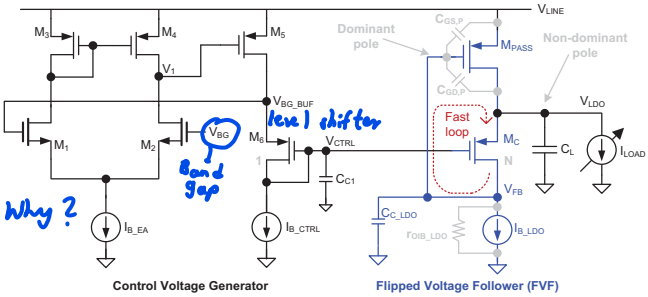


Fig. 3: Flipped voltage follower (FVF) LDO with on-chip output capacitor. The control voltage generator circuit is also shown.

of $M_C$, which is also the drain of $M_{PASS}$. Since the current through control transistor is fixed at $I_{B\_LDO}$, the $V_{SG}$ of $M_C$ is ideally constant. Thus, the output $V_{LDO}$ will be one $V_{SG}$ above $V_{CTRL}$.

The fast local analog feedback loop created by $M_C$ and $M_{PASS}$ of the FVF regulates $V_{LDO}$. $M_{PASS}$ is configured as a source follower and transistor $M_C$ is a common-gate amplifier, resulting in a moderate open-loop gain.

Because of the local feedback loop, the output range of the FVF is limited on the low side, both by the supply voltage $V_{LINE}$, $V_{CTRL}$, and $V_{SG,PASS}$. The output voltage $V_{LDO}$ satisfies

$$\begin{aligned} V_{LDO} &\leq V_{LINE} - V_{SDsat,PASS} \\ V_{LDO} &\geq V_{LINE} - V_{SG,PASS} + V_{SDsat,C} \\ V_{LDO} &\geq V_{CTRL} + |V_{THP,C}| \end{aligned} \quad (1)$$

where $|V_{THP,C}|$ is the PMOS threshold voltage. This output range is lower than the conventional LDO. This limited range impacts the pass transistor at light load currents, when $V_{SG,PASS}$ is small. Indeed, it is not possible to turn off the pass transistor completely.

The minimum bias current through $M_{PASS}$ is $I_{B\_LDO}$ and occurs when the load current is zero. During a load transient from light to heavy load current, $V_{LDO}$ will drop. When $V_{LDO}$ drops, the $V_{SG}$ of control transistor $M_C$ decreases, which pulls down the gate of $M_{PASS}$ to source higher current to the load. As such, $V_{LDO}$ is restored to one $V_{SG}$ above $V_{CTRL}$. Similarly, during a load transient from heavy to light output current, $V_{LDO}$ will increase because of the high $M_{PASS}$ current. This increases the $V_{SG}$ of $M_C$ and pulls up the gate of $M_{PASS}$ to decrease the current through it. Consequently, $V_{LDO}$ pulls back to one $V_{SG}$ above $V_{CTRL}$. The slew rate and bandwidth of the FVF loop determines the settling time of the output voltage.

The $V_{CTRL}$ generator circuit is a CMOS two-stage amplifier in buffer configuration with a level shifter in the output stage. The bandgap $V_{BG}$ reference voltage is buffered at the output of the two-stage amplifier as $V_{BG,BUF}$. A PMOS diode-connected transistor $M_6$ is used as a level shifter to move $V_{BG,BUF}$ down by one $V_{SG}$ to generate $V_{CTRL}$. $V_{CTRL}$ is applied to the gate of the FVF control transistor $M_C$, which level shifts up to $V_{LDO}$ by one $V_{SG}$. Thus, the goal is to

generate an LDO output voltage $V_{LDO}$ that is equal to $V_{BG}$. Grounded capacitor $C_{C1}$ is added at node $V_{CTRL}$ to achieve stability for the control voltage generator circuit.

The open-loop gain of the FVF LDO is given by

$$A_{DC} \approx -g_{mP}\ [r_{OIB\_LDO} || (g_{mC}\ r_{OC}\ R_{LDO})] \quad (2)$$

where $g_{mP}$, $r_{OP}$, $g_{mC}$, and $r_{OC}$ are the transconductance and output resistance of transistors $M_{PASS}$ and $M_C$, respectively. $R_{LDO}$ is the load resistor $R_L$ (not shown) in parallel with $r_{OP}$. Parameter $r_{OIB\_LDO}$ is the output resistance of current source $I_{B\_LDO}$. The open-loop gain of the FVF has a maximum value of $-g_{mP}r_{OIB\_LDO}$ at light load currents, where $g_{mC}r_{OC}R_{LDO} >> r_{OIB\_LDO}$. At heavy load currents, the open-loop gain reduces to $-g_{mP}\,(g_{mC}\ r_{OC}\ R_{LDO})$.

Since the gate capacitance of $M_{PASS}$ is large and the resistance at feedback node $V_{FB}$ is also high, the pole associated with that node will be the dominant pole. The impedance at the output node is low and thus the pole associated with that node will be non-dominant. The expression for the poles are given by

$$\begin{aligned} \omega_{P1} &\approx -\frac{1}{[r_{OIB\_LDO} || (g_{mC}\ r_{OC}\ R_{LDO})]\ C_{GS,P}} \\ \omega_{P2} &\approx -\frac{1}{\left(\frac{1}{g_{mC}} || R_{LDO}\right)\ C_{LDO}} \end{aligned} \quad (3)$$

where, $C_{GS,P}$ and $C_{GD,P}$ are the gate-to-source and gate-to-drain parasitic capacitance of pass transistor $M_{PASS}$. $C_{LDO}$ is the total equivalent grounded capacitance at node $V_{LDO}$, mainly dominated by the load capacitance $C_L$. From (3), we conclude that both poles move with load current. At light load currents, the poles are located at

$$\begin{aligned} \omega_{P1} &\approx -\frac{1}{r_{OIB\_LDO}\ C_{GS,P}} \\ \omega_{P2} &\approx -\frac{g_{mC}}{C_{LDO}} \end{aligned} \quad (4)$$

Since $r_{OIB\_LDO} >> 1/g_{mC}$, the poles are located far from each other, resulting in good stability. The bandwidth of the FVF loop is set by $\omega_{P1}$.

At heavy load currents, the poles move to

$$\begin{aligned} \omega_{P1} &\approx -\frac{1}{(g_{mC}\ r_{OC}\ R_{LDO})\ C_{GS,P}} \\ \omega_{P2} &\approx -\frac{1}{R_{LDO}\ C_{LDO}} \end{aligned} \quad (5)$$

In this case, the separation between the two poles is defined by the ratio $g_{mC}r_{OC}C_{GS,P}/C_{LDO}$. Careful design ensures these two poles are separated far enough to meet the phase margin requirements. Adding a suitable grounded compensation capacitor $C_{C\_LDO}$ at node $V_{FB}$ will make sure the two poles are far from each other to ensure stability. The magnitude response of the FVF LDO with pole-zero locations at heavy and light load currents is illustrated in Fig. 4.

One of the issues with the FVF LDO is relatively poor load regulation. The lower the output resistance, the better the output regulation. Output resistance is inversely proportional

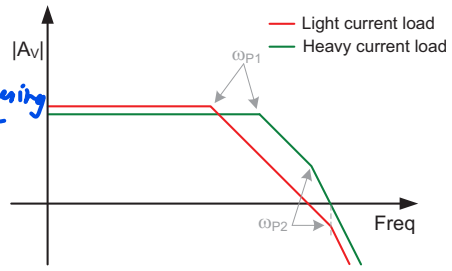


Fig. 4: Frequency response of FVF LDO with pole-zero locations for light and heavy load current conditions.

to the open-loop gain. The output resistance of the FVF LDO is expressed as [31]

$$R_{OUT} = \frac{\left(\frac{1}{g_{mC}} || r_{OP}\right)}{g_{mP}\ [r_{OIB\_LDO} || (g_{mC}\ r_{OC}\ R_{LDO})]} \quad (6)$$

The output resistance of the FVF LDO varies with load current. This variation impacts load regulation.

## III. Folded FVF LDO

To overcome FVF LDO's loop gain limitation and to improve the output regulation, the FVF can be replaced by a folded FVF, as illustrated in Fig. 5, with the addition of cascode transistor $M_{CAS}$ in the feedback loop. Bias voltage $V_{CN}$ is selected such that node $V_{FB}$ is the minimum voltage required across current source $I_{B\_LDO}$.

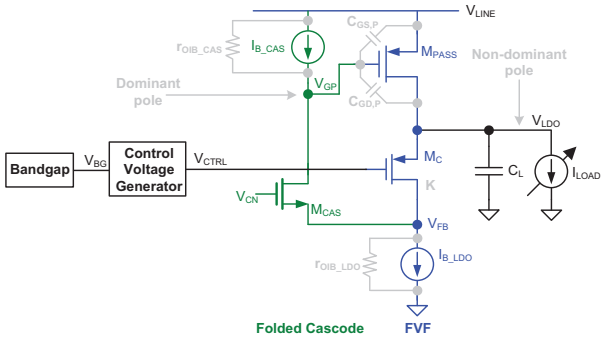


Fig. 5: Schematic of folded flipped voltage follower based LDO.

The major effect of $M_{CAS}$, high loop gain, is possible only if current source $I_{B\_CAS}$ is similarly cascoded. Nevertheless, the equivalent resistance at the gate of $M_{PASS}$ is large and thus the pole associated with node $V_{GP}$ is dominant and limits the bandwidth of the FVF loop.

The output voltage range is high in the folded FVF architecture. The inequality containing $V_{SG,PASS}$ in (1) is no longer valid. As such, it is possible to turn off transistor $M_{PASS}$ almost completely.

In [25], the authors introduce a common-drain buffer [1], [2] $M_{BUF}$ in the FVF loop, to drive the gate of the pass transistor, as shown in Fig. 6(a). Because of the low output resistance of the buffer, the pole associated with node $V_{GP}$ moves to

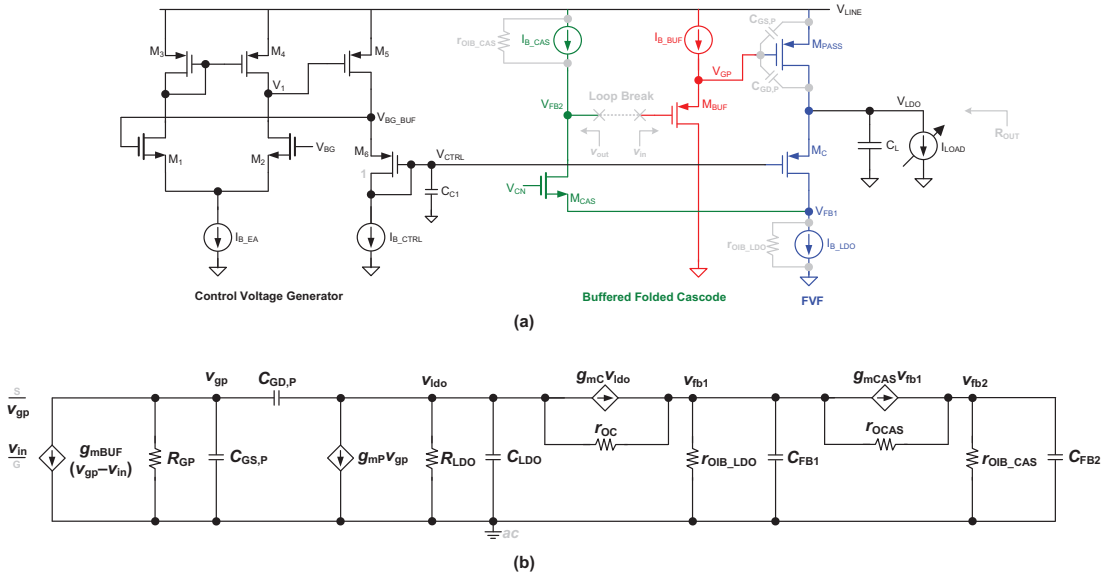


Fig. 6: (a) Transistor level schematic of buffered folded FVF based LDO from [25] and (b) its small-signal model.

higher frequencies. Now the dominant pole is determined by the high output impedance node $V_{FB2}$, which is at the drain of cascode transistor $M_{CAS}$. Since the input capacitance of buffer transistor $M_{BUF}$ is low, the dominant pole moves to higher frequencies by nearly two decades. This increase in the bandwidth of the FVF loop has no impact on the low-frequency loop gain, since the buffer has a nominal gain of one.

The small-signal model of the buffered folded FVF LDO is shown in Fig. 6(b). Assuming current $I_{B\_CAS}$ attached to node $V_{FB2}$ is a cascoded current source with high output impedance $r_{OIB\_CAS}$, whereas current source $I_{B\_LDO}$ is simple, the small-signal gain and pole locations of the LDO of Fig. 6 are approximately

$$\begin{aligned} A_{DC} &\approx -g_{mP}\,[r_{OIB\_CAS}||(g_{mCAS}r_{OCAS})r_{OIB\_LDO}] \\ \omega_{P1} &\approx -\frac{1}{[r_{OIB\_CAS}||(g_{mCAS}r_{OCAS})r_{OIB\_LDO}]C_{FB2}} \\ \omega_{P2} &\approx -\frac{1}{\left(\frac{1}{g_{mC}}||R_{LDO}\right)\,C_{LDO}} \\ \omega_{P3} &\approx -\frac{1}{\left(\frac{1}{g_{mBUF}}\right)\,C_{GS,P}} \\ \omega_{Z1} &\approx +\frac{1}{\left(\frac{1}{g_{mP}}\right)\,C_{GD,P}} \end{aligned} \tag{7}$$

where $C_{FB2}$ is the equivalent grounded capacitance at node $V_{FB2}$ and other parameters follow naming conventions.

From the DC gain expression, we note that the gain varies with $g_{mP}$. At light load currents, $g_{mP}$ is lower and the gain is reduced. As the load current increases, $g_{mP}$ increases with the square-root of load current and, thus, at higher load currents, the gain is higher. This higher loop gain reduces the output resistance of the FVF to a much lower value and improves output regulation.

The dominant pole is created by the resistance and capacitance at node $V_{FB2}$. As the capacitance $C_{FB2}$ is small, the location of the pole will be at higher frequencies but dominant by the high cascoded resistance of $I_{B\_CAS}$. The second pole is defined by $C_{LDO}$, $R_{LDO}$ and $1/g_{mC}$, Since $1/g_{mC}$ is small, this pole is also located at higher frequencies. These higher frequency poles compete for dominance as they might be closely located. Adding a compensation capacitor at node $V_{FB2}$ to ground will help in achieving stability with little compromise in bandwidth. The third pole and the RHP zero are defined by $C_{GS,P}$ & $1/g_{mBUF}$ and $C_{GD,P}$ & $1/g_{mP}$, respectively; they are located at high frequencies.

One drawback of this FVF LDO configuration is that the additional buffer $M_{BUF}$ increases the minimum voltage at node $V_{GP}$ by $V_{SG,BUF}$. It is no longer possible to turn on $M_{PASS}$ completely, which increases the dropout voltage of the LDO.

## IV. Multi-Loop Buffered FVF LDO

The bandwidth of the buffered folded FVF LDO is limited by the dominant pole of the FVF loop that is created by the high impedance node $V_{FB2}$ shown in Fig. 6. This bandwidth may be limited to tens of megahertz. In order to increase the bandwidth even higher, all the nodes in the FVF loop need to have high-frequency poles without compromising output voltage regulation. The authors in [28] introduce a multi-loop buffered FVF LDO that achieves high bandwidth; however, the regulation improvement is nominal. An advancement of the multi-loop LDO of [28] is presented in [32], in which the voltage regulation is improved significantly with no compromise in bandwidth. The schematic of the multi-loop buffered FVF LDO is shown in Fig. 7.

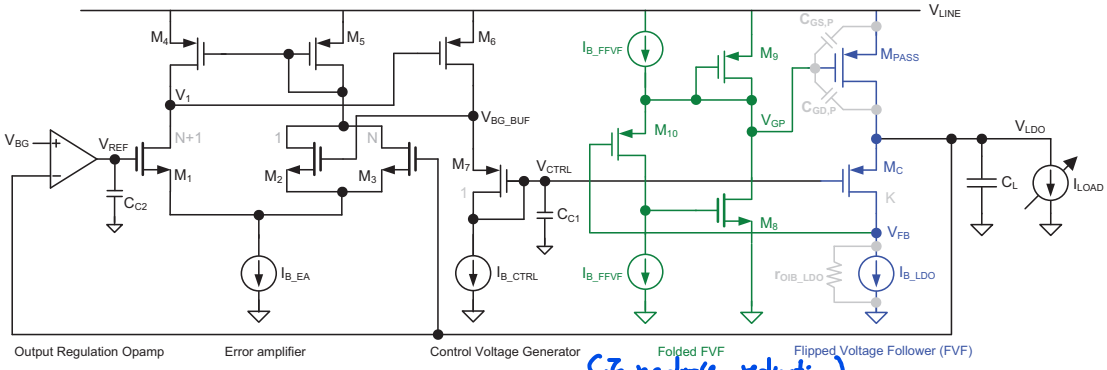


Fig. 7: Schematic of buffered cascoded FVF based LDO for accurate output regulation and high bandwidth, adapted from [6], [28] and [32].

The buffered FVF loop consists of an FVF output stage $M_{PASS} - M_C - I_{B\_LDO}$ buffered with a folded FVF formed by transistors $M_8 - M_{10}$ with two bias currents labeled $I_{B\_FFVF}$. The advantage of a folded FVF over a common-drain voltage follower is lower output resistance. Thus, the pole at the gate of $M_{PASS}$ is moved to higher frequencies. Transistor $M_9$ is added as a diode-connected transistor load of the folded FVF, which further reduces the impedance at node $V_{GP}$, particularly at high frequencies when the folded FVF output impedance begins to rise [31]. Note also that transistor $M_9$ forms the input side of a current mirror with transistor $M_{PASS}$. Thus, the ground current in the output stage increases with load current.

The loop gain of the FVF loop is designed to be relatively low, such that its bandwidth is high and, without the presence of the outer loops, would result in poor phase margin and poor load regulation. The dominant pole is moved to the output node, where a minimum load capacitance, $C_L$, is required for stability. The value of output capacitance is in the hundreds of picofarads and thus can easily be integrated on-chip.

The control voltage generation circuit is similar to the circuit shown in Fig. 6, with the exception that one side of the input differential pair is split into two transistors, $M_2$ and $M_3$, described below.

In order to improve load regulation and phase margin, one outer loop from the LDO output, $V_{LDO}$, to the control voltage generation circuit is added. The outer loop feedback is made stronger than the inner loop feedback from $V_{BG,BUF}$. This is implemented by splitting the input differential pair transistor into two transistors with ratio $N : 1$. The outer loop is connected to the higher-weighted transistor and the inner-loop to the smaller one. If the output deviates far from the reference voltage, then the control voltage $V_{CTRL}$ is adjusted in order to pull the output voltage back to the reference value.

A second outer loop is added in [32] to improve the output regulation significantly by integrating the error between the bandgap voltage $V_{BG}$ and the output voltage $V_{LDO}$ using a single-stage opamp and capacitor $C_{C2}$. Opamp output signal $V_{REF}$ is now the input to the control voltage generation block. In steady-state, $V_{REF}$ equals $V_{BG}$. However, during a transient, if the output drops below $V_{BG}$, $V_{REF}$ increases so as to restore the output voltage to $V_{BG}$.

The outer loop bandwidths are slower than the main FVF loop, such that excellent DC output regulation is achieved by the slow loops and excellent transient response is made possible by the high-frequency FVF loop.

## V. Discussion and Conclusion

This tutorial began with a discussion of the conventional stand-alone LDO IC, which used an external output capacitor in the range of hundreds of nanofarads to tens of microfarads. It then described the recent trend in SoCs toward point-of-load integrated LDOs, requiring a low-value on-chip output capacitor. These LDOs achieve high open-loop gain for excellent output voltage regulation, but their bandwidth is limited by an internal dominant pole. This limited bandwidth resulted in reduced PSRR at high frequencies.

The tutorial then introduced the basic FVF circuit as a promising candidate for implementing high bandwidth LDOs due to its fast local feedback loop. Several iterations, including folding and buffering the FVF loop led up to a multi-loop design that simultaneously achieved high open-loop gain for good load regulation and high bandwidth. A peculiar characteristic of this integrated multi-loop FVF LDO architecture is the dominance of the output pole, which is set at a high frequency by an output capacitor in the hundreds of picofarads. This high bandwidth resulted in good PSRR over a wide frequency range.

A present challenge in FVF LDOs is the maximum achievable load current. Indeed, the multi-loop folded FVF LDOs of [28], [32] are limited to a load current of 10 mA. This limit appears to be caused, at least in part, by the limited voltage range at the gate of the pass transistor. Whereas the pass transistor can be fully turned off, it cannot be fully turned on, as the minimum gate voltage is at least one $V_{SG}$ above ground.

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