Athul Robert R.B. 20 BCE1610.

Design of 4-bit Ripple Canter

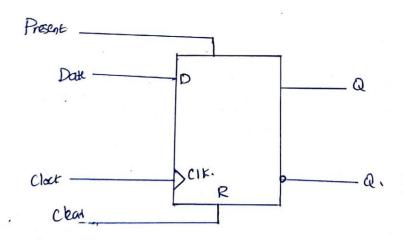
dim:

To design a 4-bit ripple Counter using D flip flop and venify its output using LT spice.

Software Registed:

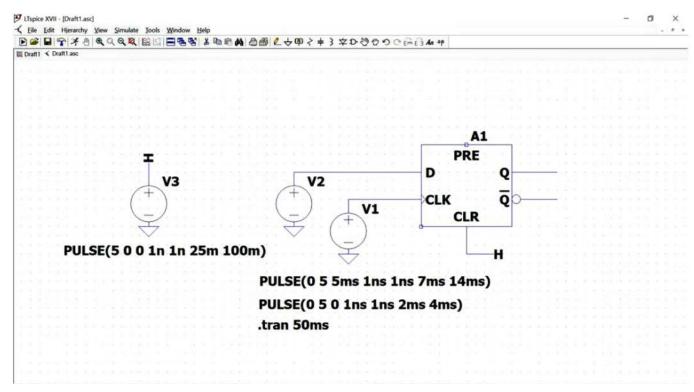
LT Spice.

Block diagram:

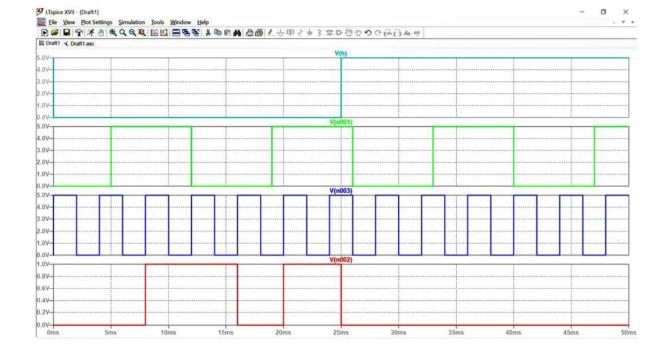


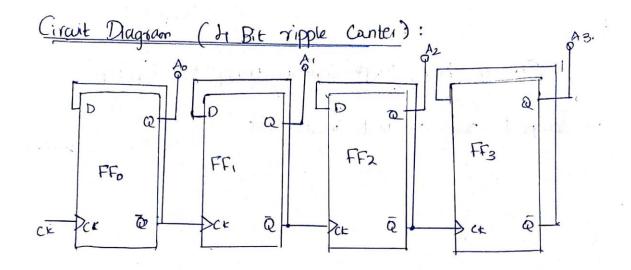
And the second s	table (D	Fip Flop):
Ds	Q (t+1)	
0	D	reset
1	1 %	Set.

D Flip-flop circuit(with clear input):



D flip- flop waveforms(with clear input):

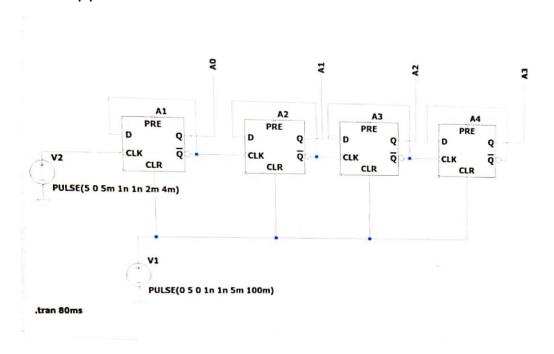




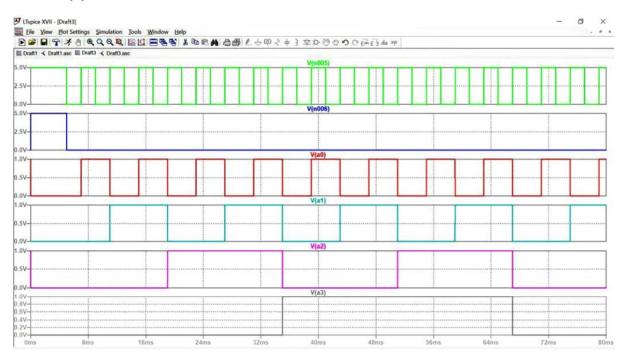
Truth table. (In Bit ripple Counter).

CK	A3	A_2	A	A
D	0	0	0	0
	0	0	D	١
2	٥	0	1	0
3	0	0	١	١
4	0	1	O	0
5	0	1	0	1
6	0	1	1	D
7	D	1	1	
8	1	0		1
9	-1	0	0	0
10	1	0	1	0
11	1	0	1	1
12	1	1	6	D
13)	1	D	1
14	1		1	0
15)	1	1	

4 Bit ripple counter circuit:



4 bit ripple counter waveforms:



Result:

The H. Lit Yipple Canter. Using D flip flop
is designed and verified in LT Spice.