CSE1003

DLD-LAB EXP 8:

MULTIPLEXER

Date: 8/06/21

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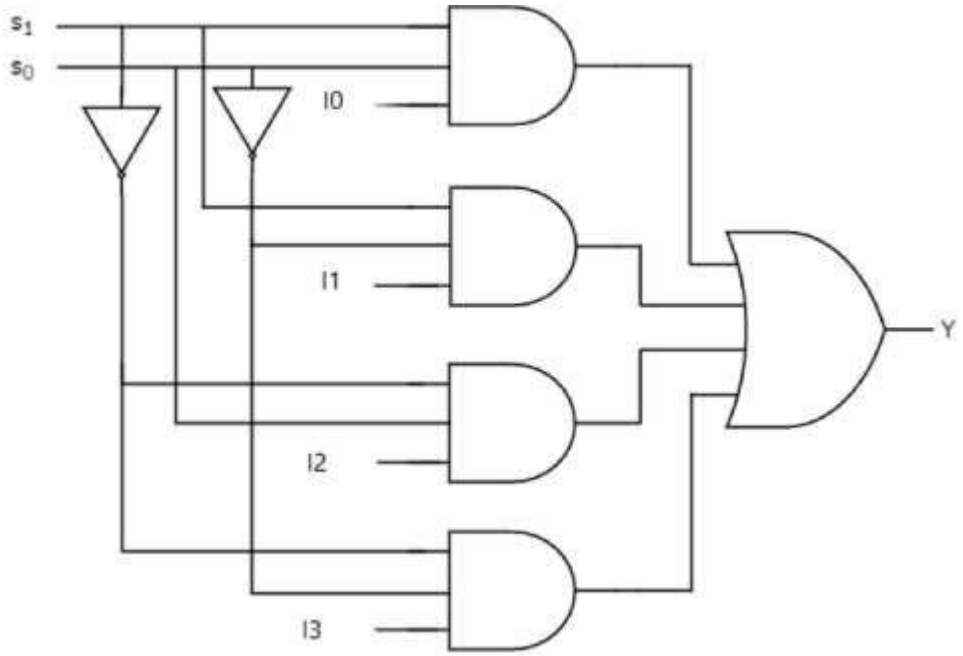
Aim: To design a half adder using 4X1 multiplexer.

Tools used: LTSpice

4x1 MULTIPLEXER

- **Logic diagram**

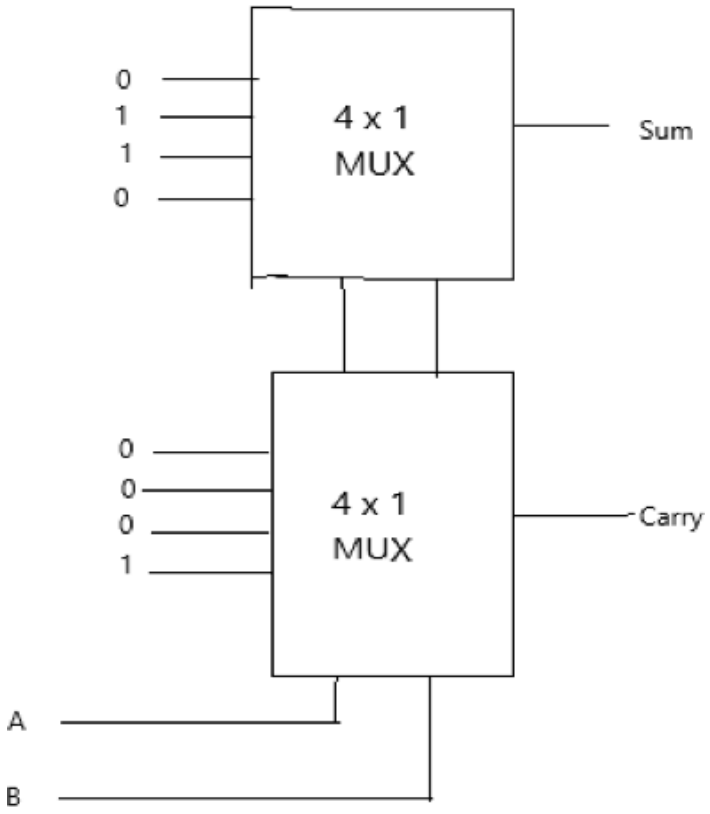


- **Truth table**

S0	S1	A	B	C	D	Y
0	0	A	0	0	0	A
0	1	0	B	0	0	B
1	0	0	0	C	0	C
1	1	0	0	0	D	D

HALF ADDER USING MUX

- **Logic diagram**



- **Truth table**

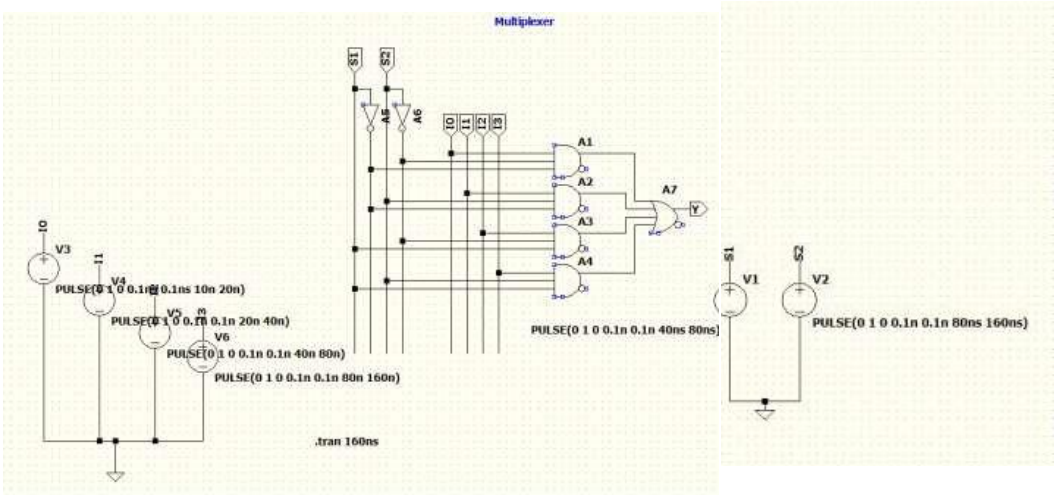
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

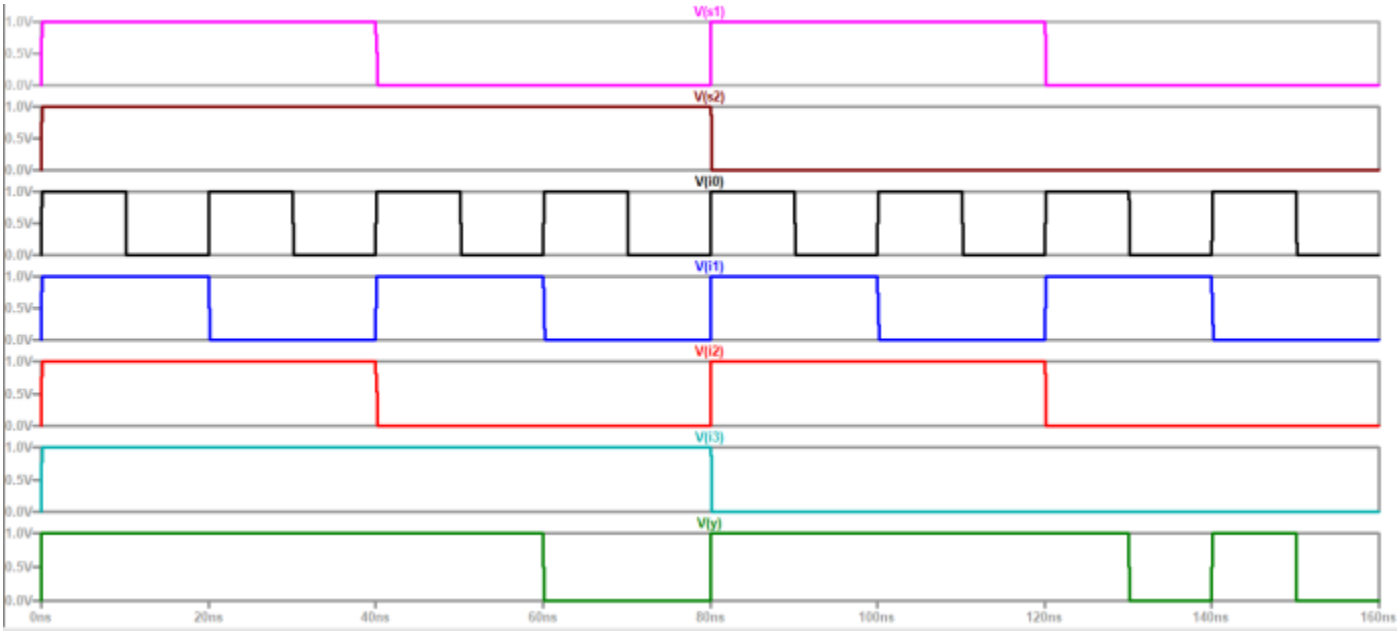
Procedure

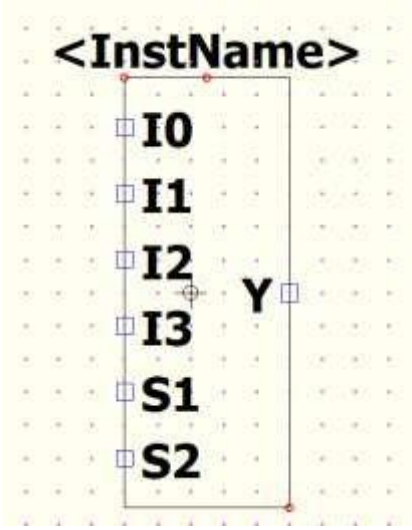
1. Open LTSpice.
2. Implement the circuit for 4x1 multiplexer and verify the output with its truth table.
3. Create a symbol for 4x1 mux.
4. Using the 4x1 mux, design a circuit for half adder.
5. Simulate and verify the output with its truth table.

LTSpice simulations and symbols

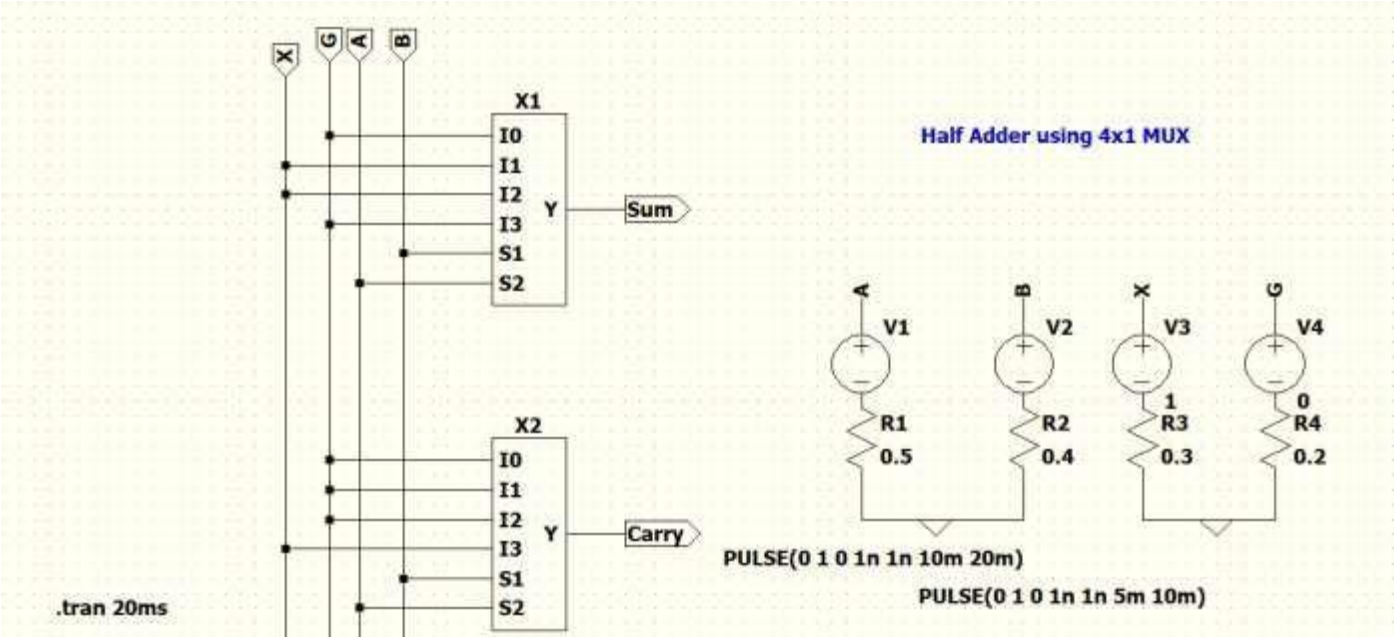
- Creating 4x1 mux symbol

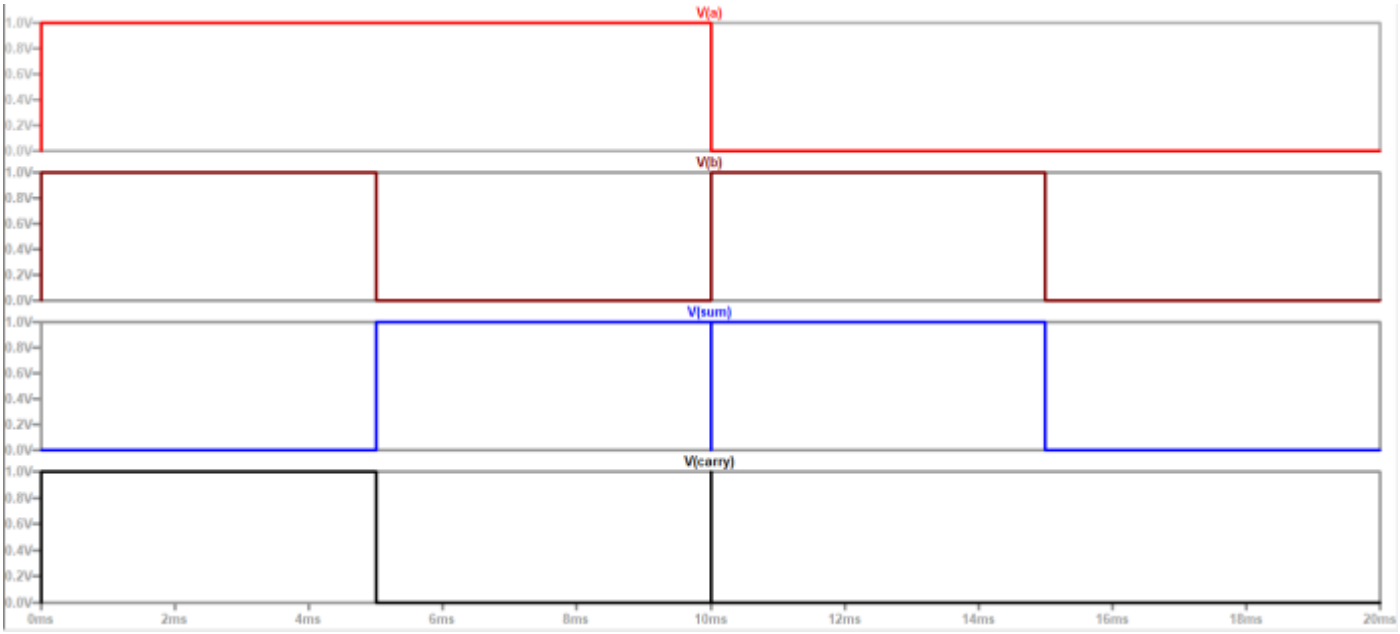






- Designing half adder





Conclusions

Thus, a 4x1 multiplexer was designed on LTSpice using which a half adder is designed and implemented.