Dept. of Computer Science and Engineering
IIT Delhi
COL216: Preparation for Minor Exam
II Semester 2020-2021

Minor Exam to begin: 20 March 2021 (Saturday), 2:00 PM
Submission deadline: 21 March 2021 (Sunday), 11:59 PM

We will have a minor exam on March 20, 2021, starting at 2 pm. It will be 27 hours assignment-based exam, where you will be asked to add more architectural features to the simulator that you have implemented in Assignment 3.

Therefore, we would like you to validate your code of assignment 3 or make desired changes if needed.

We are releasing 4 sample test cases today (compressed file uploaded on Moodle). These test cases vary based on the input format and instruction format.

Note: Even if one of the formats is supported by your program, you are good to go and just focus on the exam. Need not worry about the output format. Just simply focus on the expected values.

Important note: If you have not either implemented or are not confident about your code, you can select either of the option:

Option 1: Borrow code from your classmate and provide his/her name in the document.

Option 2: Implement a basic MIPS interpreter with add, addi, lw, and sw instructions only and use it for the minor.

Description of Test Cases:

All 4 test cases perform the same operation. Simply the way of writing the assembly program differs.

Description of the program:

1. **Initialization:** Initialize memory from 1000-1040 with natural numbers 1-10
2. **Summation**: After initialization, add two numbers and store the output back into the memory address (higher address)
3. Repeat step 2 for nine times

Values in memory (in decimal format):

Stage	1000	1004	1008	1012	1016	1020	1024	1028	1032	1036
Initialization	1	2	3	4	5	6	7	8	9	10
Summation	1	3	6	10	15	21	28	36	45	55

Each test case description:

Testcase 1: lw/sw instructions accept destination as a memory address stored in a register + branch instructions followed by a label

i.e., lw $t0, 1($s0)
j loop

Testcase 2: lw/sw instructions accept destination memory address as a constant value.

i.e., lw $t0, 1000 #1000 is the memory address

Testcase 3: lw/sw instructions accept destination memory address stored in a register + branch instructions followed by the instruction address (no label)

i.e., lw $t0, 1($s0)
j 12 #jump to the instruction at address 12

Testcase 4: lw/sw instructions accept destination memory address stored in a register + branch instructions followed by the distance relative to current instruction address (stored in PC)

i.e., lw $t0, 1($s0)
j -12 #jump to the instruction at address PC-12

Note: If your input format changes on small parameters such as the following:

a. Remove/change entry(main)/exit identifiers.
b. Spaces

In such cases, you can either make changes to your program or test cases.

You are given two files with each test case:

1. Testcase Input
2. Expected Output

The expected output format may vary from student to student but make sure that the program's behaviour in each cycle and registers or memory values are the same.