



QUESTION PAPER

Name of the Examination: CAT (FALL 2022-2023)

Course Code: ECE2002

Course Title: Computer Organization and Architecture

Slot: SB1+STB1

Date of Exam: 01-11-2022

Duration: 90 min

Total Marks: 50

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. What are the different buses used in the Microprocessor? Draw the single bus structure. **(10M)**

Q2. Draw the flow chart and demonstrate the division approach using the restoring algorithm to divide 11 by 3. **(15M)**

Q3. How to represent the signed integer numbers? Perform arithmetic operation in binary using sign-magnitude and 2's complement representation.

- (i) $(+34) + (-15)$ **(10M)**
- (ii) $(-34) - (-15)$

Q4. What are the different addressing modes used in the 8086 microprocessor? Discuss each with a suitable example. **(15M)**

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	1	1	1	1	1	10
Q2	2	1	2	2	1	15
Q3	2	2	3	2	3	10
Q4	3	2	4	2	3	15



QUESTION PAPER

Name of the Examination: FAT 2022-2023

Course Code: ECE2002

Course Title: COA

SET number: 1

Date of Exam: 20-12-2022-A
(B1)

Duration: 120 min

Total Marks: 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

Q1. How to represent the signed integer numbers? Perform arithmetic operation in binary using 1's and 2's complement representation

(i) $(+42) + (-13)$

(ii) $(-42) - (-13)$

(10M)

Q2. Demonstrate and explain how control signals are generated using Micro-Programmed control unit. **(10M)**

Q3. What are the different phases of a basic computer instruction cycle ? Explain instruction cycle with flowchart. **(10M)**

Q4. Explain a function of the memory management unit in a typical computer. Demonstrate Direct and Set associative map technique in cache memory. **(15M)**

Q5. What is instruction pipelining? Discuss the conflicts that occurred during instruction Pipelining? **(15M)**

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1	1	2	10
Q2	4	2	1	2	1	10
Q3	4	2	1	3	1	10
Q4	5	1	2	4	3	15
Q5	6	3	2	3	3	15



QUESTION PAPER

Name of the Examination: FALL 2022-2023

Course Code: ECE2002

Course Title: COA

Set number: 3

Date of Exam: 20-12-2022 - AN (B2)

Duration: 120 mins

Total Marks: 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

- Q1.** Explain the algorithm for performing the multiplication of two numbers with multiplicand, B=10111 and multiplier, A= 10011. (10M)
- Q2.** Describe the Wilkes' micro programmed control unit. Also highlight its advantages and disadvantages. (10M)
- Q3.** Explain any one type of hardwired control unit and with suitable diagram. (10M)
- Q4.** Consider a main memory of size 4MB that needs to be mapped with a cache memory of 64KB with a frame size of 8KB. For the given hardware specifications, design the memory mapping using an 8-way set associative method. (15M)
- Q5.** What are the limitations of a scalar pipelined processor? Explain pipelined superscalar processor of degree m=3 for four stages of instruction execution. (15M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1	1	2	10
Q2	4	2	1	2	1	10
Q3	4	2	1	3	1	10
Q4	5	1	2	4	3	15
Q5	6	3	2	3	3	15



QUESTION PAPER

Name of the Examination: FALL 2022-2023 - FAT

Course Code: ECE2002

Course Title: COA

Set number: 4

Date of Exam: 21-12-2022 - FN (CI)

Duration: 120 mins

Total Marks: 60

Instructions:

1. Assume data wherever necessary.
2. Any assumptions made should be clearly stated.

- Q1.** How to represent the signed integer numbers? Perform arithmetic addition and subtraction operation of 31 and 12 using two's complement. In this example, explain how to handle the overflow? (10M)
- Q2.** Compare hardware and micro programmed control units? Also compare horizontal and vertical micro-instructions. (10M)
- Q3.** Discuss how micro operations are organized to control a processor. (10M)
- Q4.** Consider a main memory associated with 22-bit physical address and a cache memory having 8KB space. For the given hardware, design the memory map using fully associative method considering frame size equal to 2KB. (15M)
- Q5** What are the pipeline hazards that can cause a slowdown in the pipeline process? Briefly explain all of them with possible remedies. (15M)

QP MAPPING

Q. No.	Module Number	CO Mapped	PO Mapped	PEO Mapped	PSO Mapped	Marks
Q1	2	1	1	1	2	10
Q2	4	2	1	2	1	10
Q3	4	2	1	3	1	10
Q4	5	1	2	4	3	15
Q5	6	3	2	3	3	15