ECEC_500

Spring 2025

Project 6b: Implementing RISC V I-Type Instruction Datapath in Verilog

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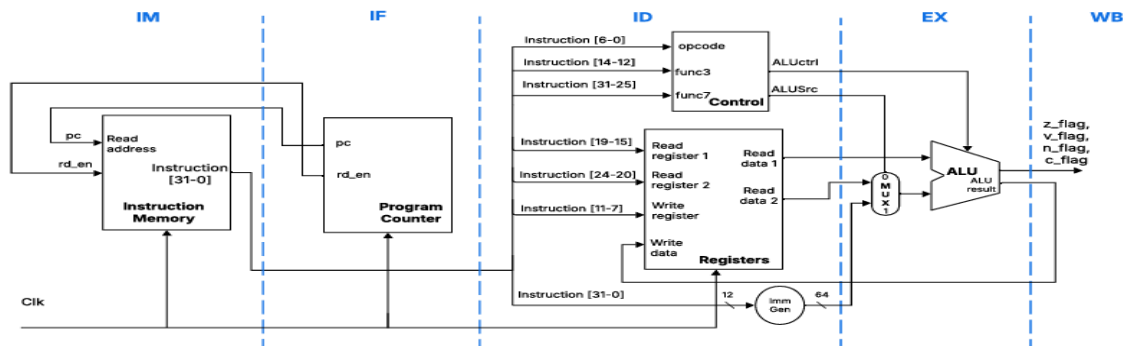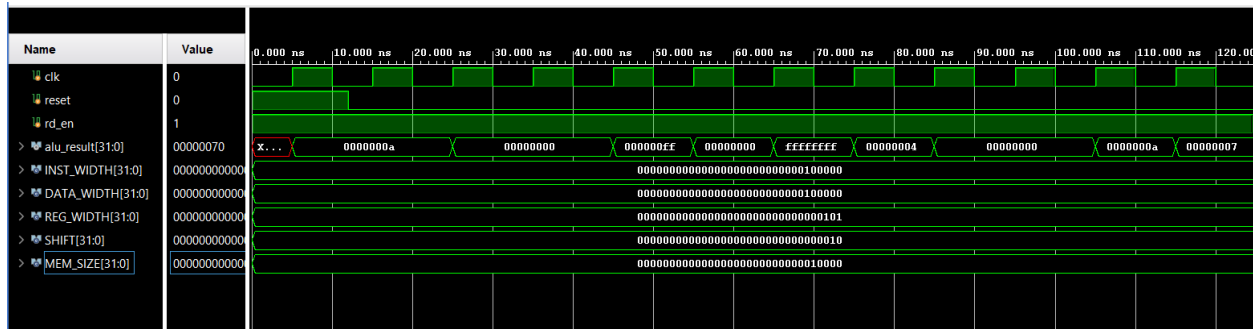
I-type RISC-V Instruction Datapath

Figure 1: Instruction Datapath

Simulation Output:

Synthesis Results:

Resource	Estimation	Available	Utilization %
LUT	733	53200	1.38
FF	1024	106400	0.96
IO	35	125	28.00
BUFG	1	32	3.13

Implementation Results:

Resource	Utilization	Available	Utilization %
LUT	733	53200	1.38
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Power:

Total On-Chip Power:	**59.474 W (Junction temp exceeded!)**
Junction Temperature:	**125.0 °C**
Thermal Margin:	-625.9 °C (-53.5 W)
Effective θJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low