Schematic to GDSII of SRAM Array

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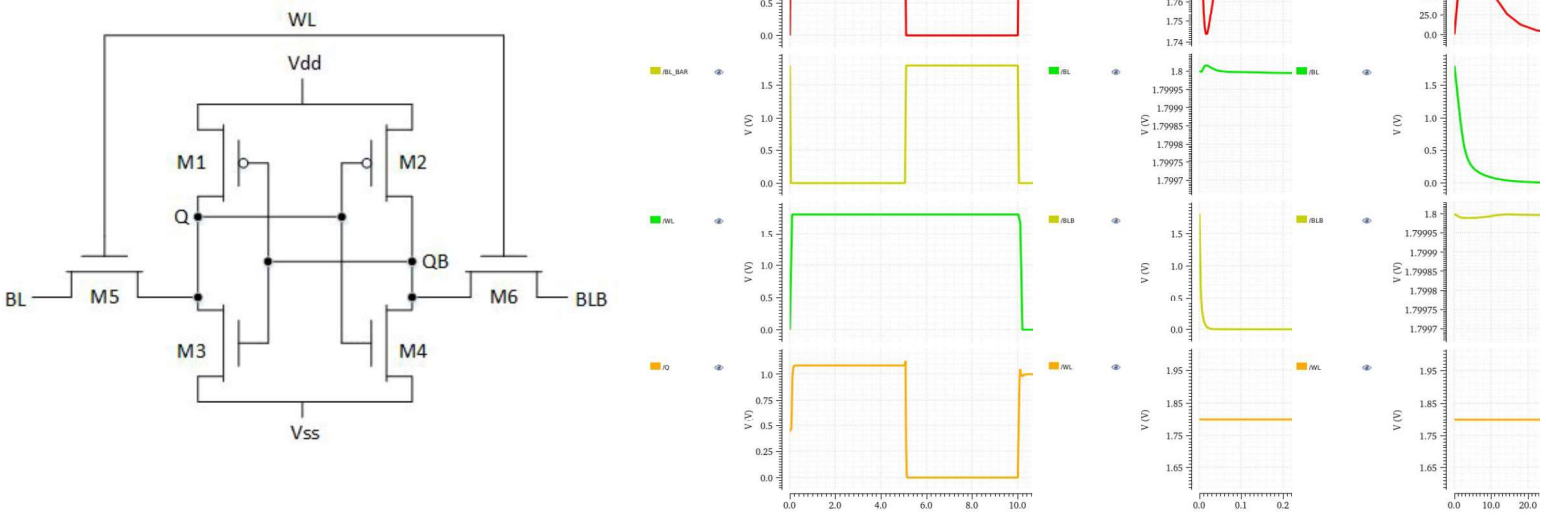
Design of 6T SRAM With Peripheral Circuitry Using Cadence Virtuoso (SCL 180nm)

- 6T SRAM bitcell:

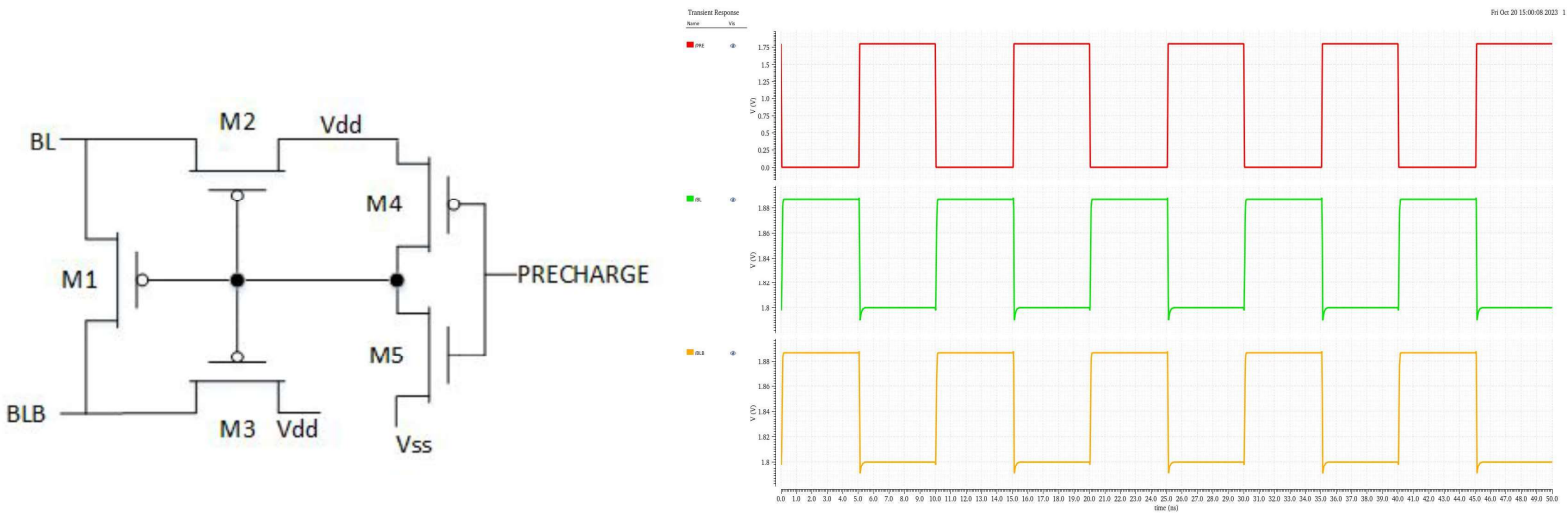


(a) (b) (c)

Fig. (a) 6T SRAM circuit (b) Simulation of Write Operation (c) Simulation of Read Operation

Contd.

- Precharge:

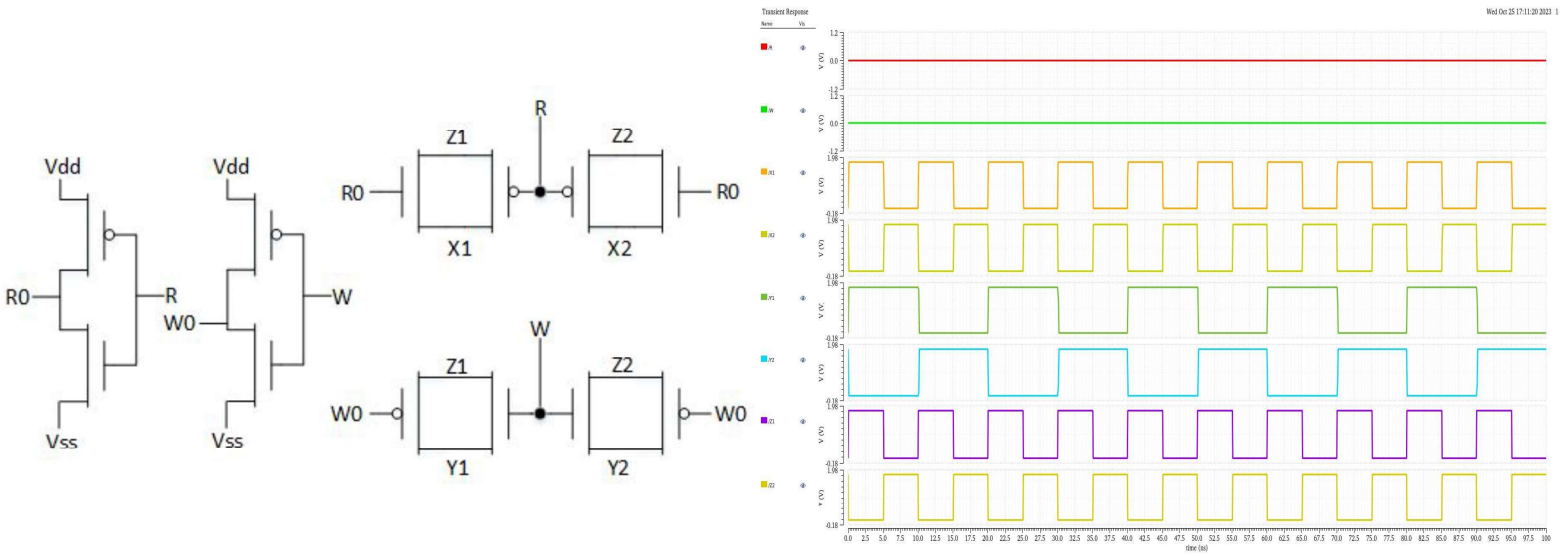


(a) (b)

Fig. (a) Precharge circuit (b) Simulation of precharge operation

Contd.

- 2:1 Multiplexer:

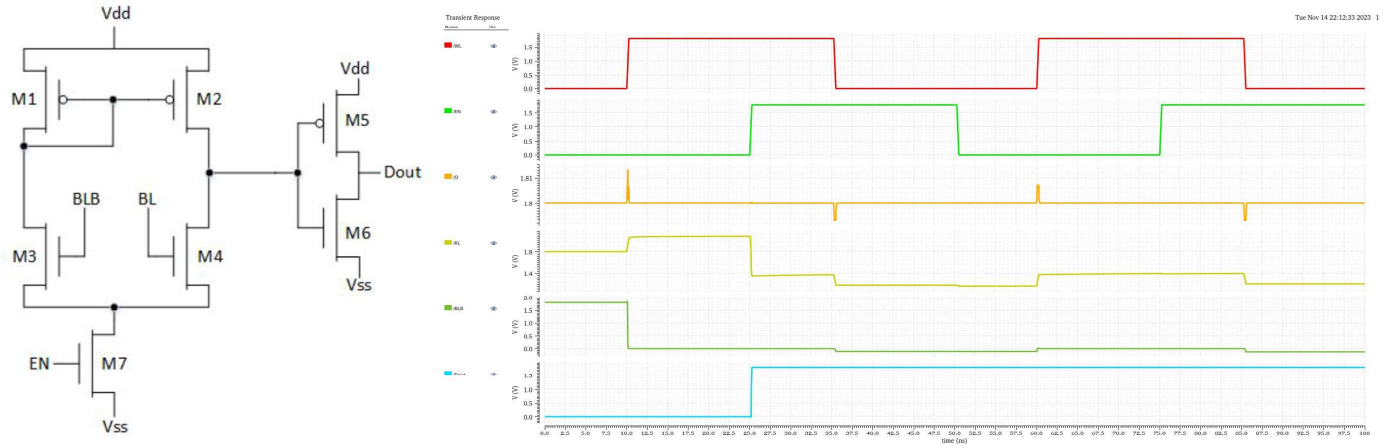


(a) (b)

Fig. (a) 2:1 Multiplexer circuit (b) Simulation of multiplexing operation

Contd.

- Voltage Mode Sense Amplifier (VMSA):

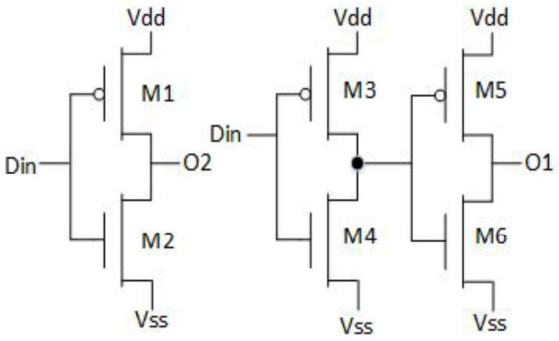


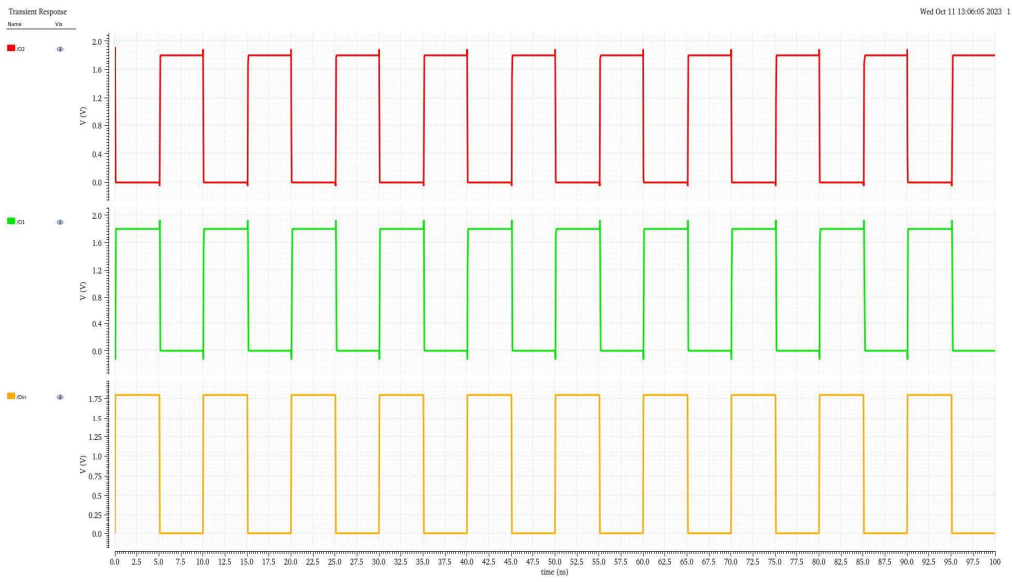
(a) (b)

Fig. (a) VMSA circuit (b) Simulation of sensing operation

Contd.

- Write Driver:



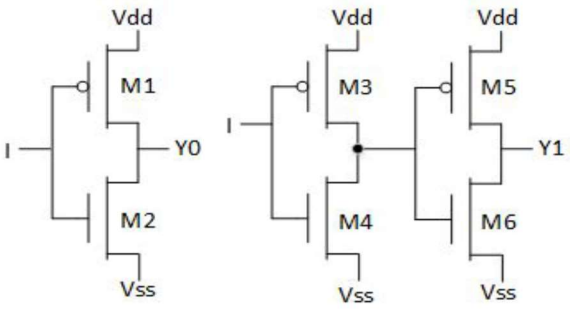


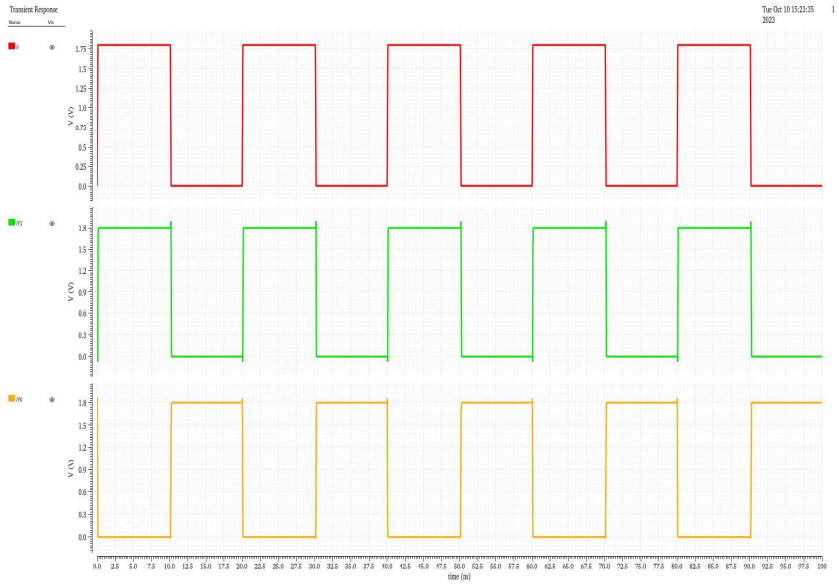
(a) (b)

Fig. (a) Write driver circuit (b) Simulation of write driver operation

Contd.

- Decoder:

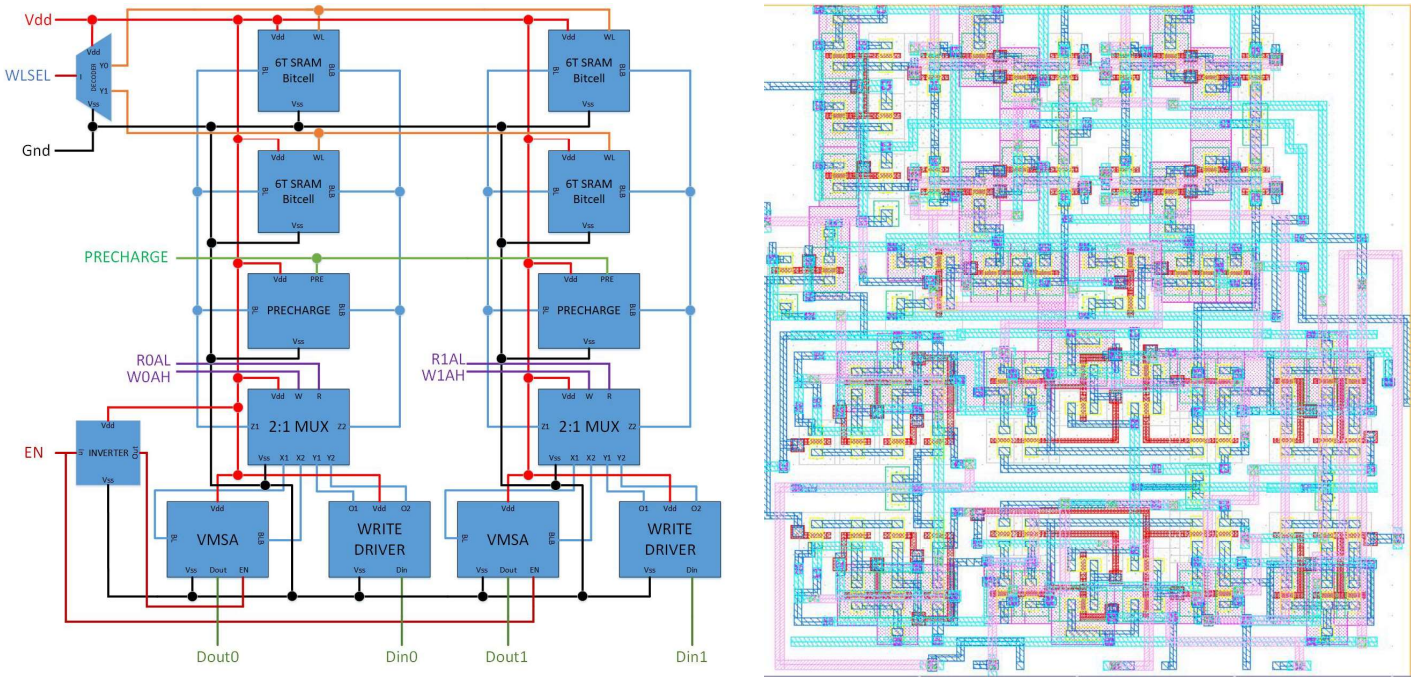




(a) (b)

Fig. (a) Decoder circuit (b) Simulation of decoding operation

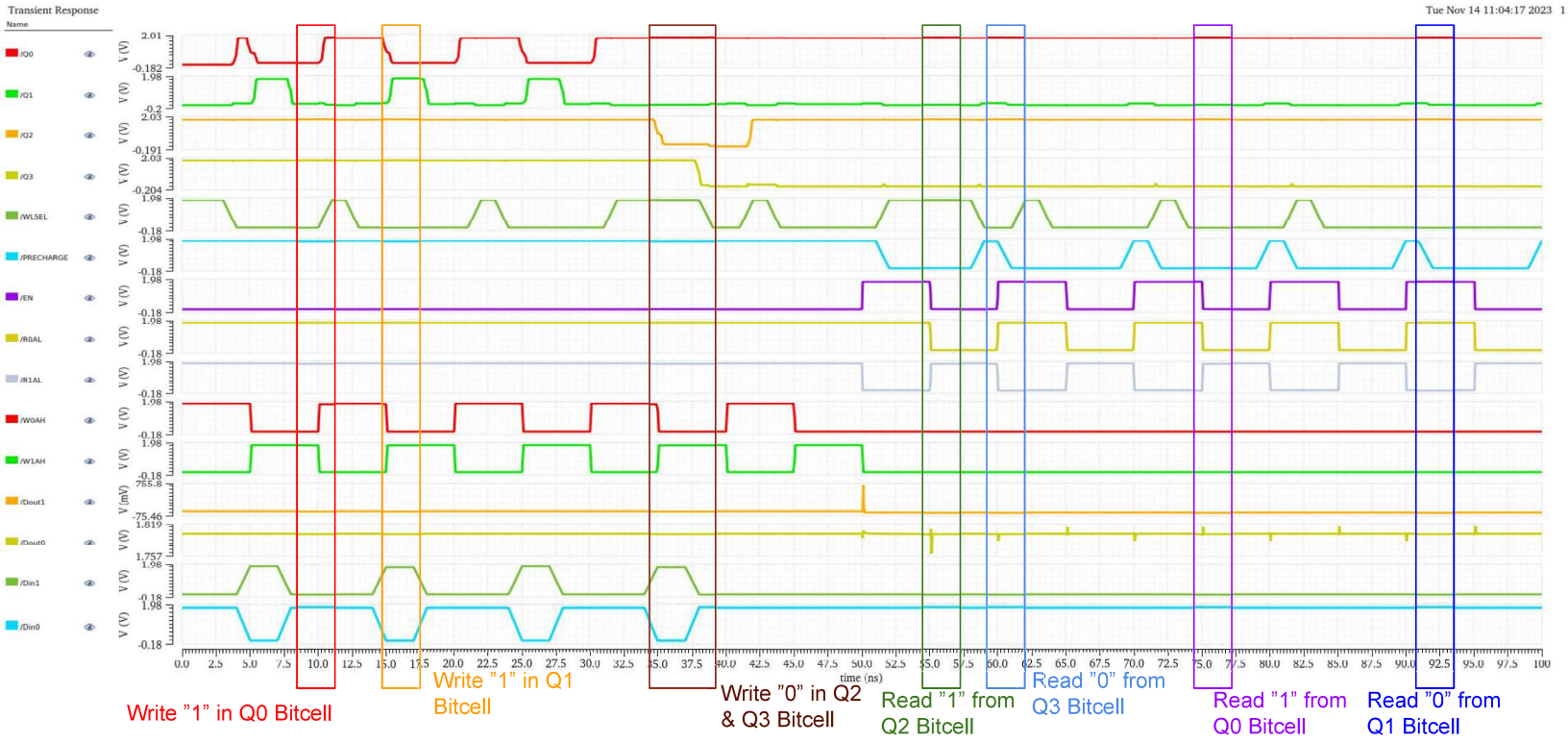
2x2 SRAM Memory Array (SCL 180nm)



(a) (b)

Fig. (a) 2x2 SRAM schematic (b) Layout

2x2 SRAM Memory Array Simulation Waveform



8x8 SRAM Memory Array

- **8x8 SRAM Memory:**

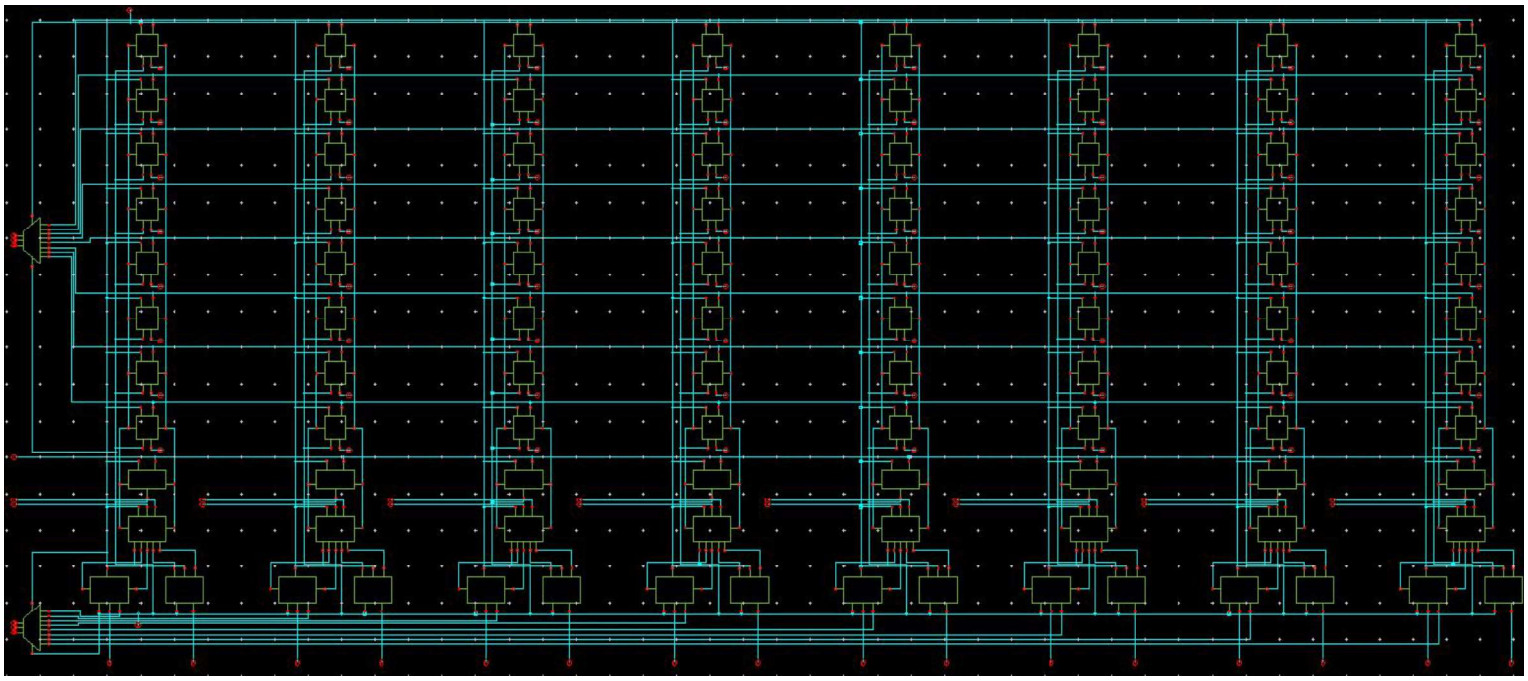
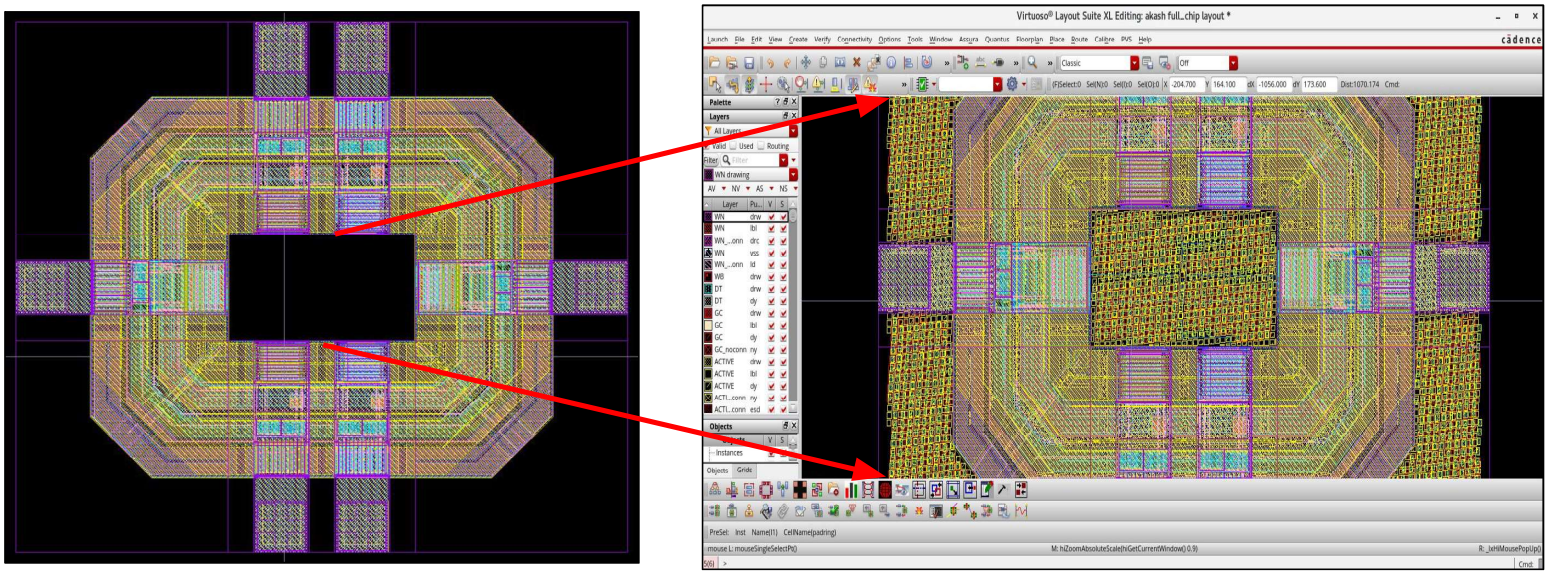


Fig. Schematic of 8x8 SRAM Memory

I/O Padding, Dummy Insertion and GDSII File Generation (SCL 180nm)



THANK YOU