

01. What is the expression for difference, borrow
of full subtractor circuit

- (a) Diff = $A \oplus B \oplus C$, Borrow = $\overline{AC} + (A \odot B)C$
- (b) Diff = $A \oplus B \oplus C$, Borrow = $\overline{AB} + (\overline{A \oplus B}) \cdot C$
- (c) Diff = $A \odot B \odot C$, Borrow = $\overline{AB} + (\overline{A \odot B}) C$
- (d) Diff = $A \odot B \odot C$, Borrow = $\overline{AC} + (A \odot B) C$

(b) $\lambda \Rightarrow$ what is the expression for difference, borrow
of full subtraction circuit.

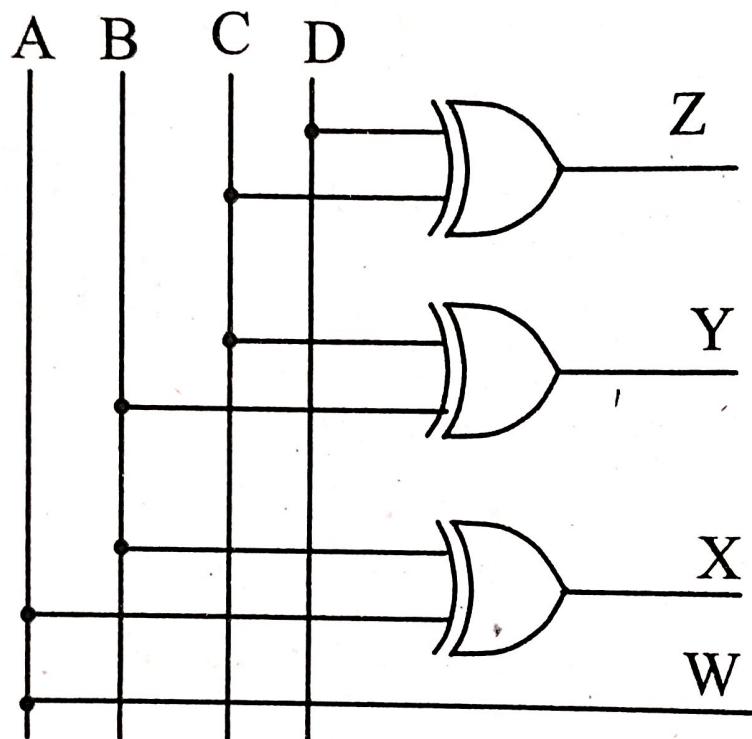
Sol

$$\text{Diff of Full sub.} = A \oplus B \oplus C$$

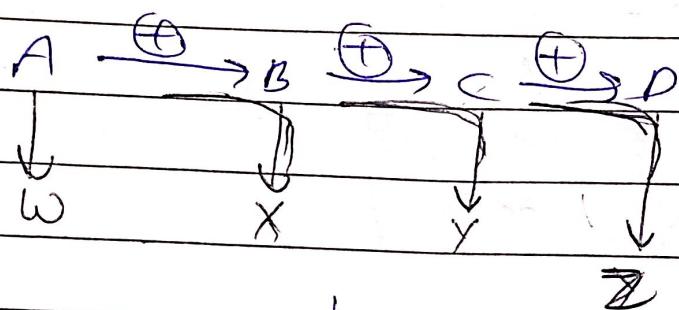
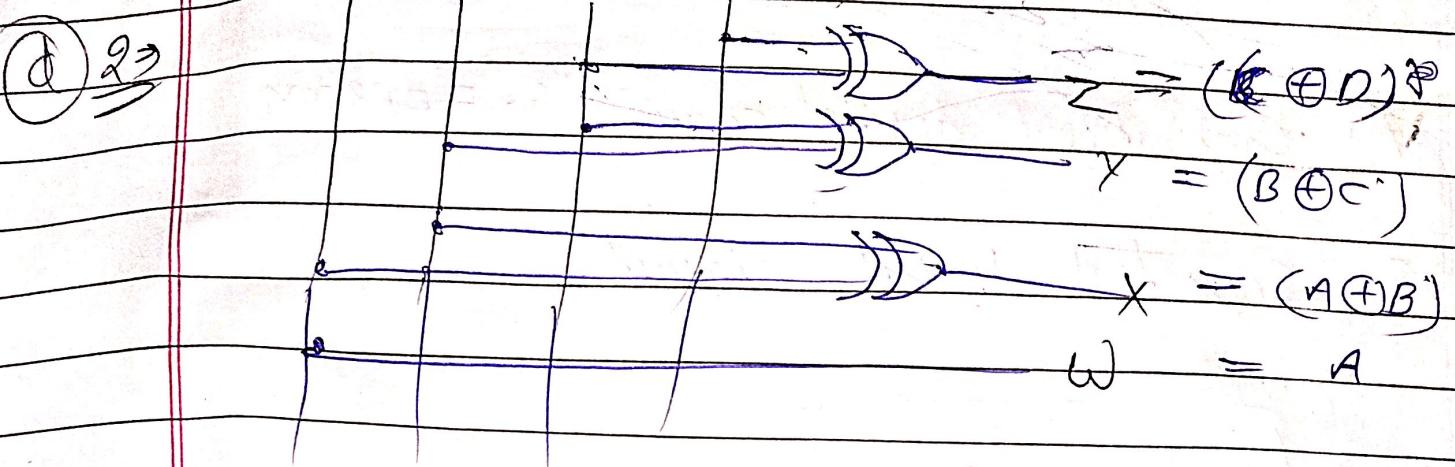
$$\text{Borrow} = \bar{A}B + (\overline{A \oplus B})C$$

(b) $\text{Diff} = A \oplus B \oplus C, \text{ Borrow} = \bar{A}B + (\overline{A \oplus B})C$

02. If ABCD is the four bit binary code, then what is the code generated at the output terminals WXYZ ?



- (a) BCD code
- (b) Excess – 3 code
- (c) 8 4 2 1 code
- (d) Gray code



It is equivalent to
gray code.

Q4

Gray code

03. Match the following

List – I

- P. Minimum number of NAND gates required to realize Ex-NOR gate.
- Q. 4 – bit Binary adder can be implemented with minimum of how many half adders and OR gates.
- R. Combinational digital circuit
- S. Sequential digital circuit

List – II

1. Seven Half – Adders and 3 OR gates
2. Five NAND gates
3. Four NAND gates
4. Eight half adders and four OR gates
5. Serial Adder
6. EEPROM

Codes:

	P	Q	R	S
(a)	2	1	6	5
(b)	1	2	5	6
(c)	3	1	2	5
(d)	2	3	4	5

(a) 3

List - 3

P. Minimum number of NAND gates required to realize Ex-NOR gate.

1. List - 21
1. Seven Half adder
→ 3-OR gates

2. Five NAND gates

Q. A 4-bit binary adder can be implemented with minimum of how many half adder and OR gates

3. Four NAND gates

4. 8 H.A &
9 OR gates

5. Serial Adder

R. Combinational digital circuit 6. EEPROM

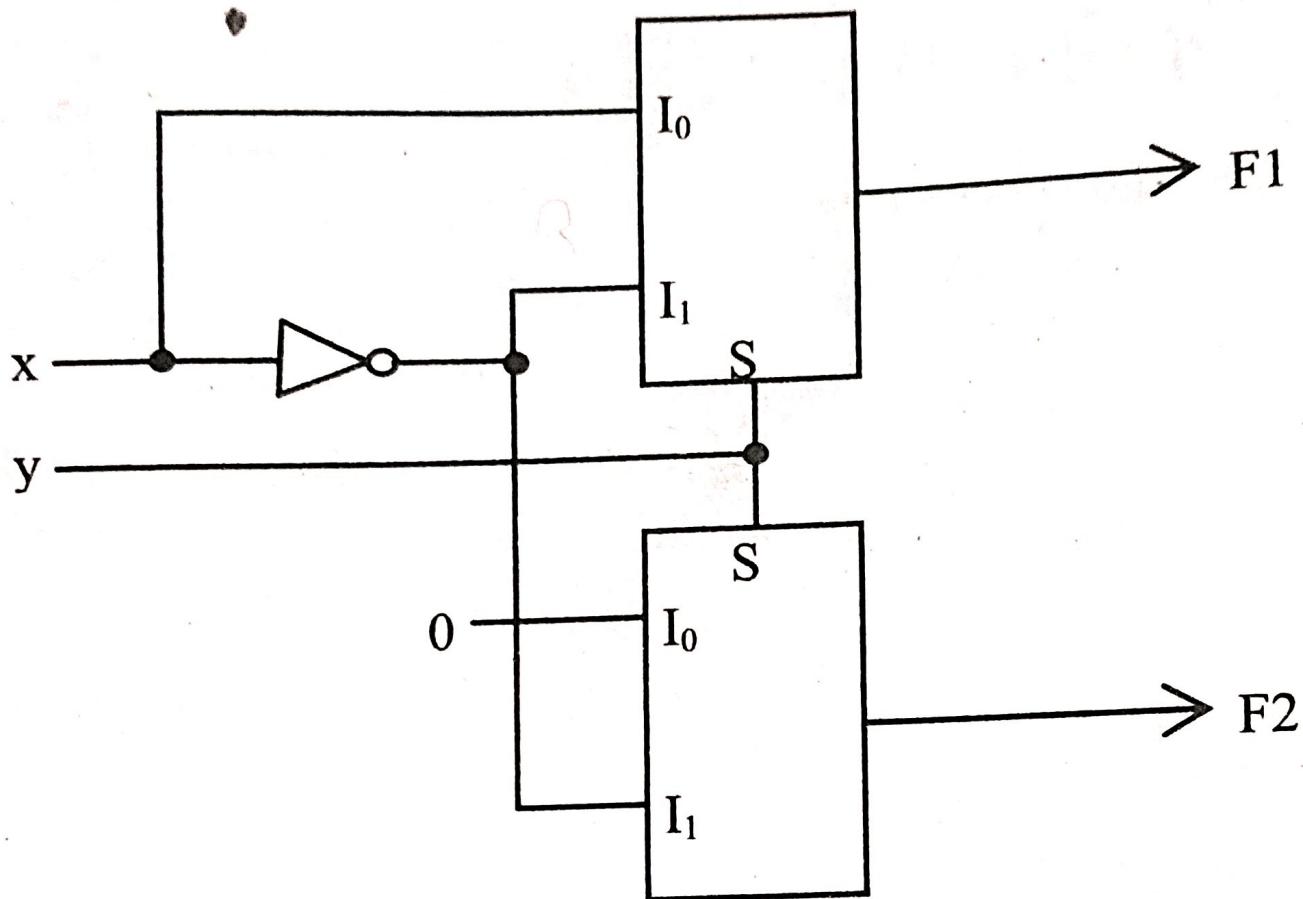
S. Sequential digital circuit

(c)

$P \rightarrow$	2
$Q \rightarrow$	2
$R \rightarrow$	6
$S \rightarrow$	M

Linked Answer Questions 04 & 05

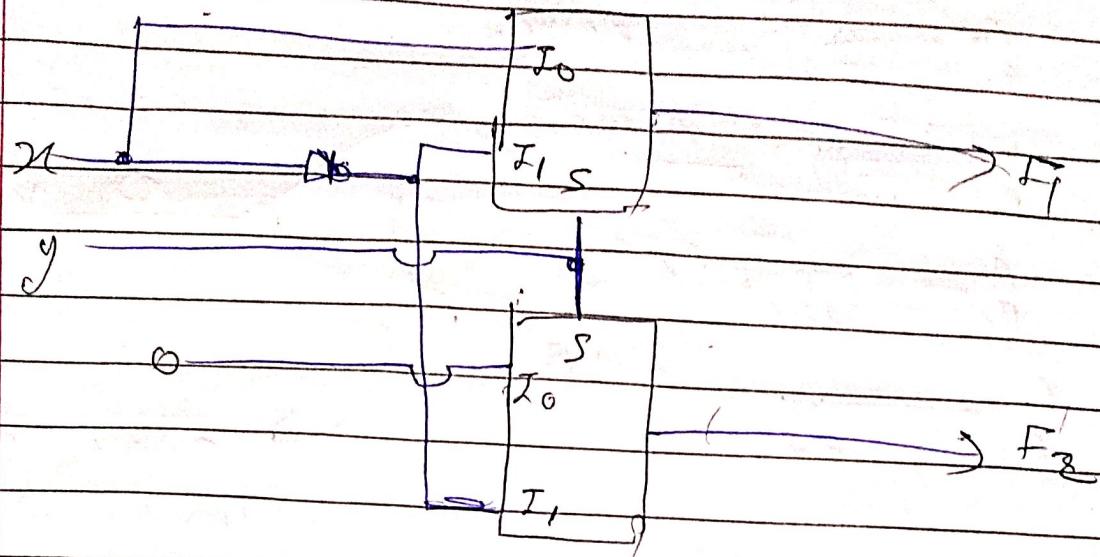
Consider the combinational circuit shown below



04. What is the circuit shown in figure?

- (a) Full Adder
- (b) Full Subtractor
- (c) Half Adder
- (d) Half Subtractor

Common $I_S \rightarrow S$



d) 9.28

Type of above circuit

$$F_1 = I_0 \bar{S} + I_1 S = x \bar{S} + \bar{x} S = x \oplus y$$

$$F_2 = I_0 \bar{S} + I_1 S = 0 + \bar{x} S = \bar{x} y$$

Diff = $x \oplus y$, Bなん = $\bar{x} y$

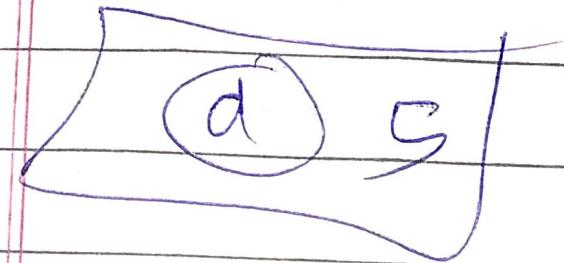
Half Adder Subtractor

(d) ns

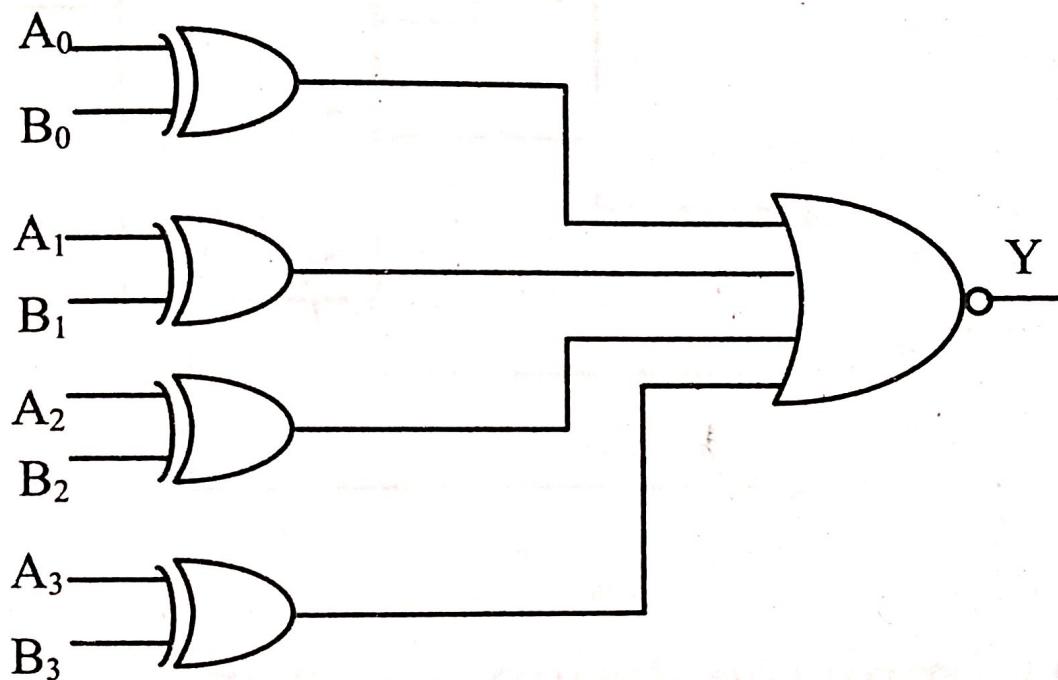
05. Minimum number of NAND gates required to implement above circuit is _____.

- (a) 5
- (b) 4
- (c) 3
- (d) 2

~~a 53~~ Minimum NAND gate -



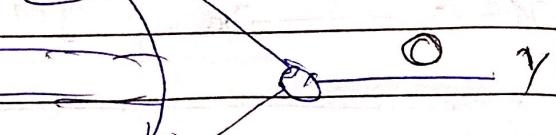
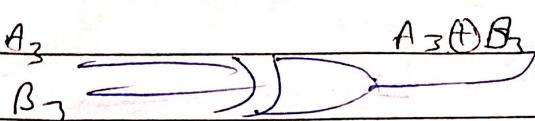
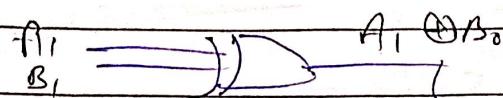
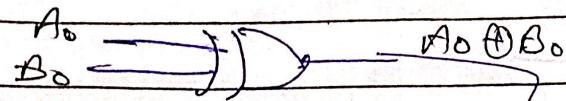
06. A digital circuit which compares two numbers $A_3 A_2 A_1 A_0$, $B_3 B_2 B_1 B_0$ is shown in figure. To get output $Y = 0$, choose one pair of *correct* input numbers



- (a) 1010, 1010
- (c) 0010, 0010

- (b) 0101, 0101
- (d) 0010, 1011

d) ~~53~~ Compan $A_3 A_2 A_1 A_0 \times B_3 B_2 B_1 B_0$
 $\rightarrow Y = 0$



$$0+0+0+0 = 1$$

$$1+0+0+0 = 0$$

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

At least
one 1

mean

01 01 10

A) $1010|1010 \rightarrow 1,00,11,00 \rightarrow 0,0,0$

B) $0101|0101 \rightarrow 00,11,00-11 \rightarrow 0,0,0$

C) $0010|0010 \rightarrow 00,00,11,00 \rightarrow 0,0,0$

D) $0010|1011 \rightarrow 01,00,11,01 \rightarrow 1,0,01$

$$\overline{1+0+0} = \overline{T} = \boxed{0}$$

07. Which one of the following statement is true?

- (a) Excess-3 code is self complementary code because of 2's complement of excess-3 code is 9's complement of given BCD number.
- (b) Excess-3 code is self complementary code because of 1's complement of excess-3 code is 9's complement of given BCD number is 1's complement form.
- (c) Excess-3 code is self complementary code because of 1's complement of excess-3 code is 9's complement of given BCD number is 2's complement form.
- (d) Excess-3 code is self complementary code because of 1's complement of given BCD number Excess-3 code is 9's complement of given BCD number in Excess-3 form.

(d) ~~7~~

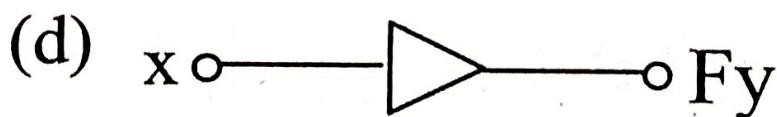
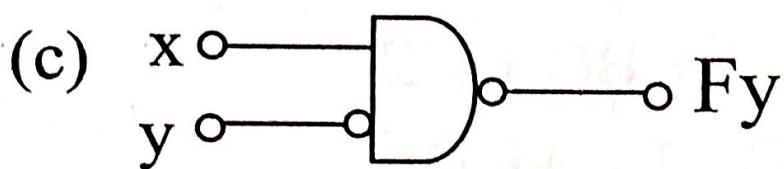
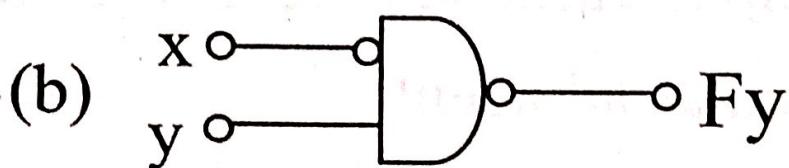
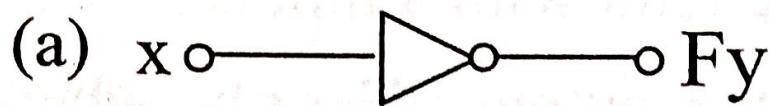
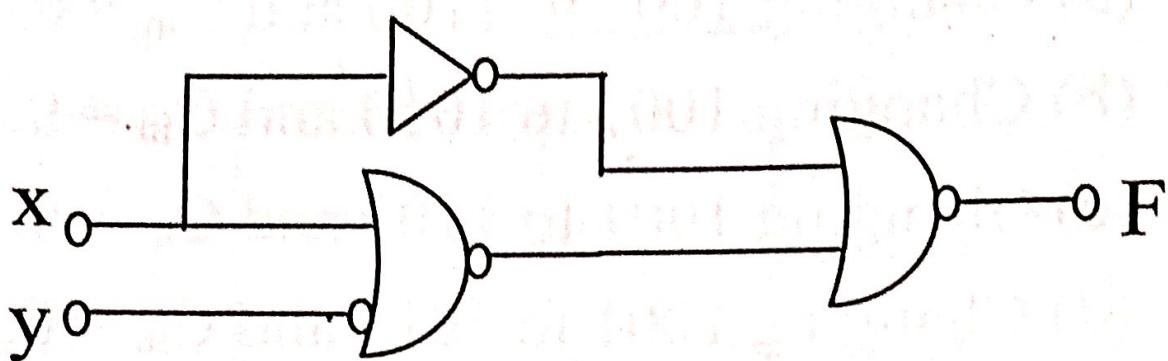
True -

(d)

~~Excess~~

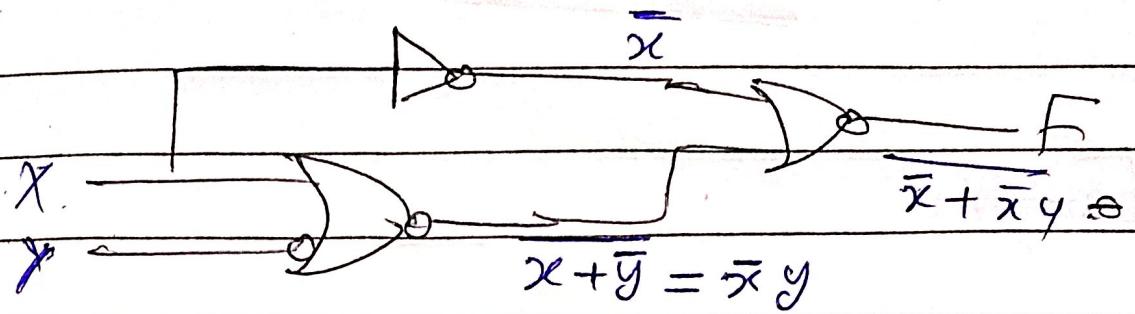
True -

08. The logic circuit shown in the given figure can be minimized to

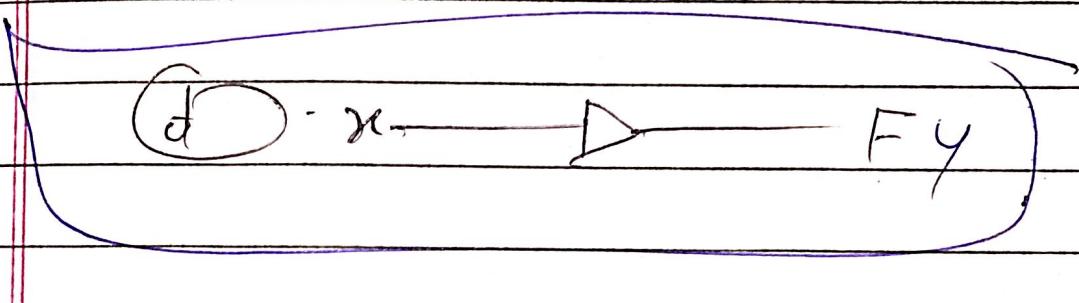


(d) 8²

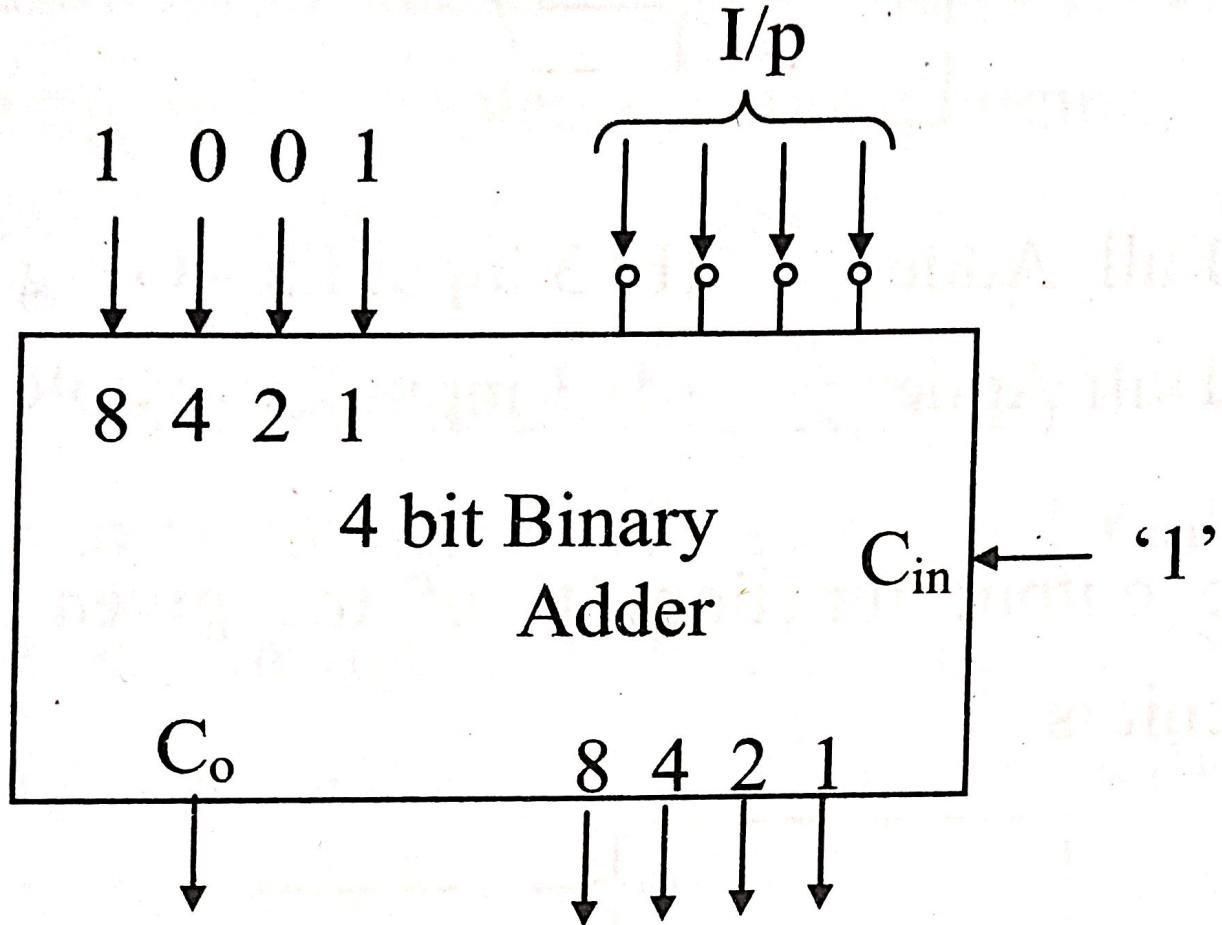
minimized \rightarrow



$$F = \frac{\bar{x} + \bar{x}y}{\bar{x}(1+y)} = \boxed{\bar{x}}$$



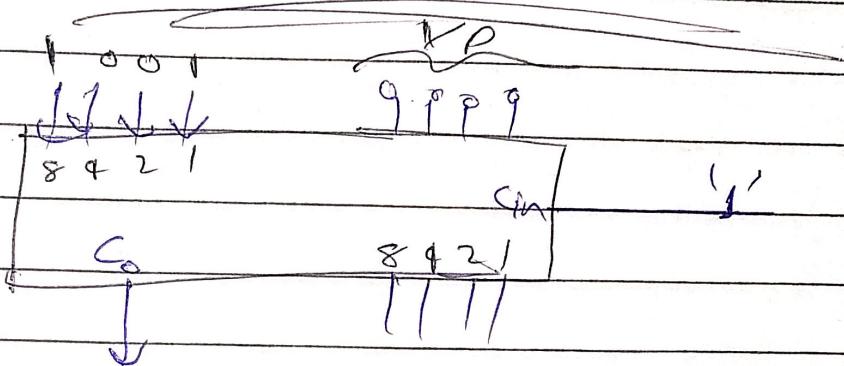
Common Data for Questions 09 & 10



09. The above circuit is converting

- (a) I/p No. to excess – 3 No.
- (b) I/p No. to 2's complement No.
- (c) I/p No. to 9's complement No.
- (d) None

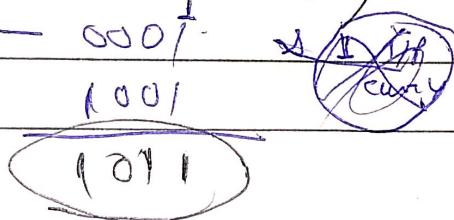
Common 9 & 10



(d) 92

Above circuit converting -

Let I.P. - 0001



(d) None

Teacher's Signature

10. Whatever the operation the circuit is performing, is possible to implement?

- (a) Changing 1001 to 1100 and $C_{in} = 0$.
- (b) Changing 1001 to 1010 and $C_{in} = 0$.
- (c) Changing 1001 to 1101 and $C_{in} = 0$.
- (d) Changing 1001 to 1011 and $C_{in} = 0$.

b) \Rightarrow whenever the operation the circuit
is performed is possible to implement.

$$\begin{array}{r} \text{Co (Carry)} \rightarrow 0 \\ \text{IP} \rightarrow 0001 \leftarrow \\ + 1000 \leftarrow \\ \hline 1011 \end{array}$$