

01. Assertion (A) : Master-slave JK flip-flop is free from race-around condition.

Reason(R) : Master-slave uses two JK flip-flops.

~~J~~ A) Master-slave JK flip-flop is free from race-around condition.

(R) Master-Slave uses two JK-Slip-flop.

~~Both True~~

02. Assertion (A): D-flip-flops are used as buffer register.

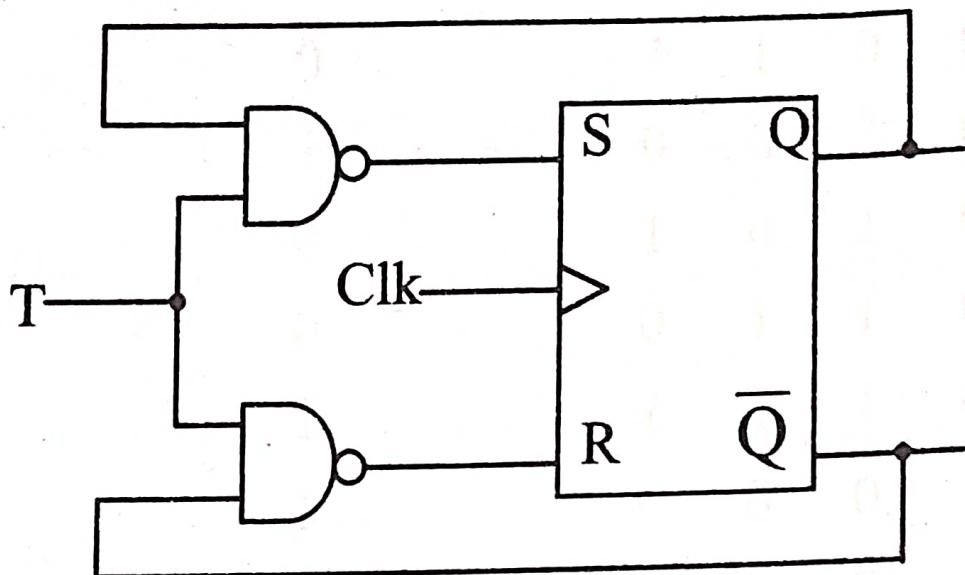
Reason (R): D-flip-flops are free from “race-around” condition.

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true

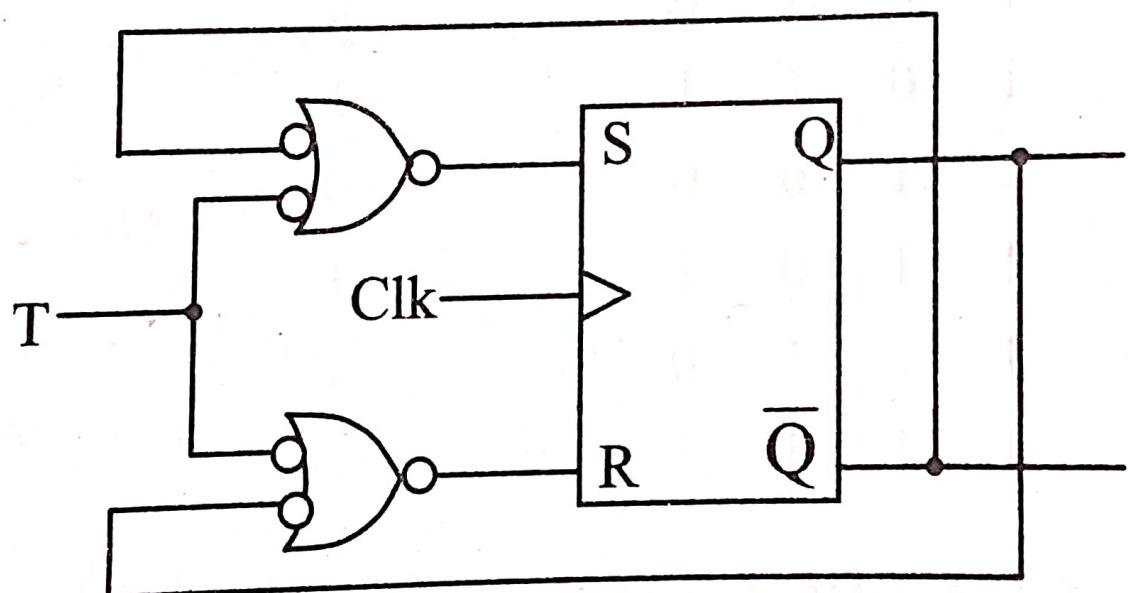
- (b) 23
- A) D-flip-flops are used as buffer register.
- B) D-flip-flops are free from "race-around" condition.
- C) Both true but R is not correct explanation of A.

03. Which one of the following circuits converts an SR flip-flop to T flip flop ?

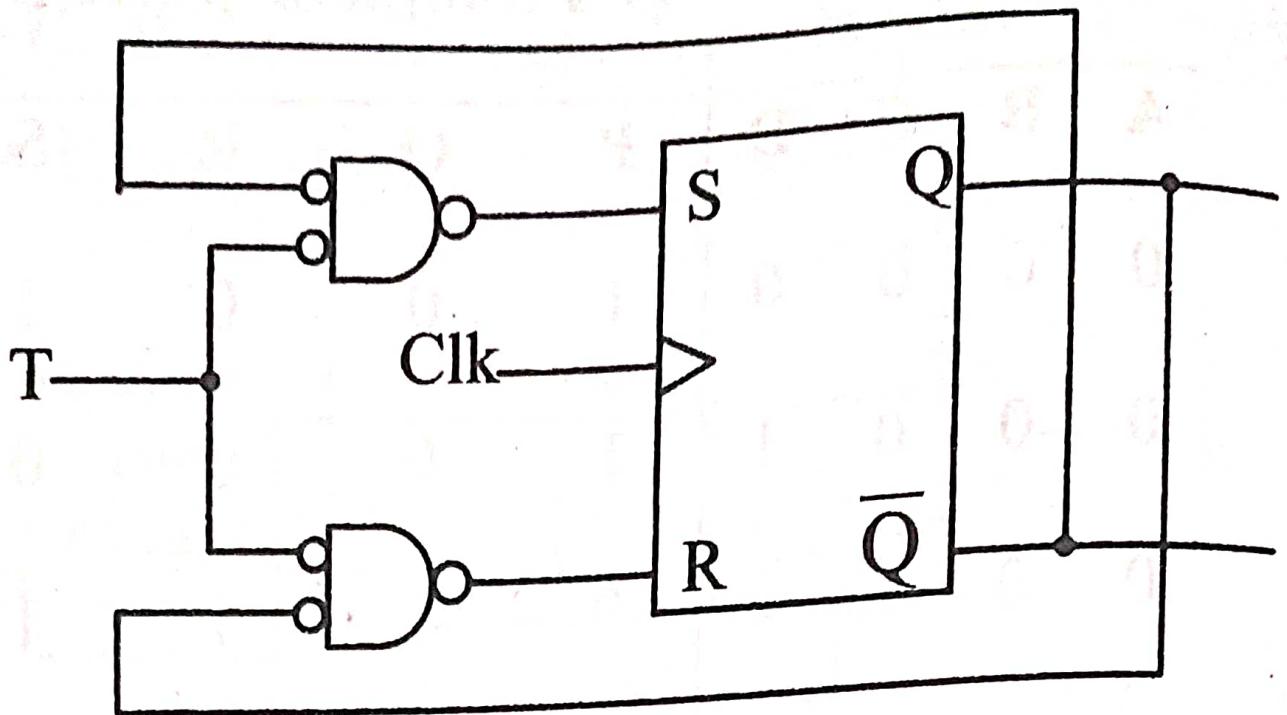
(a)



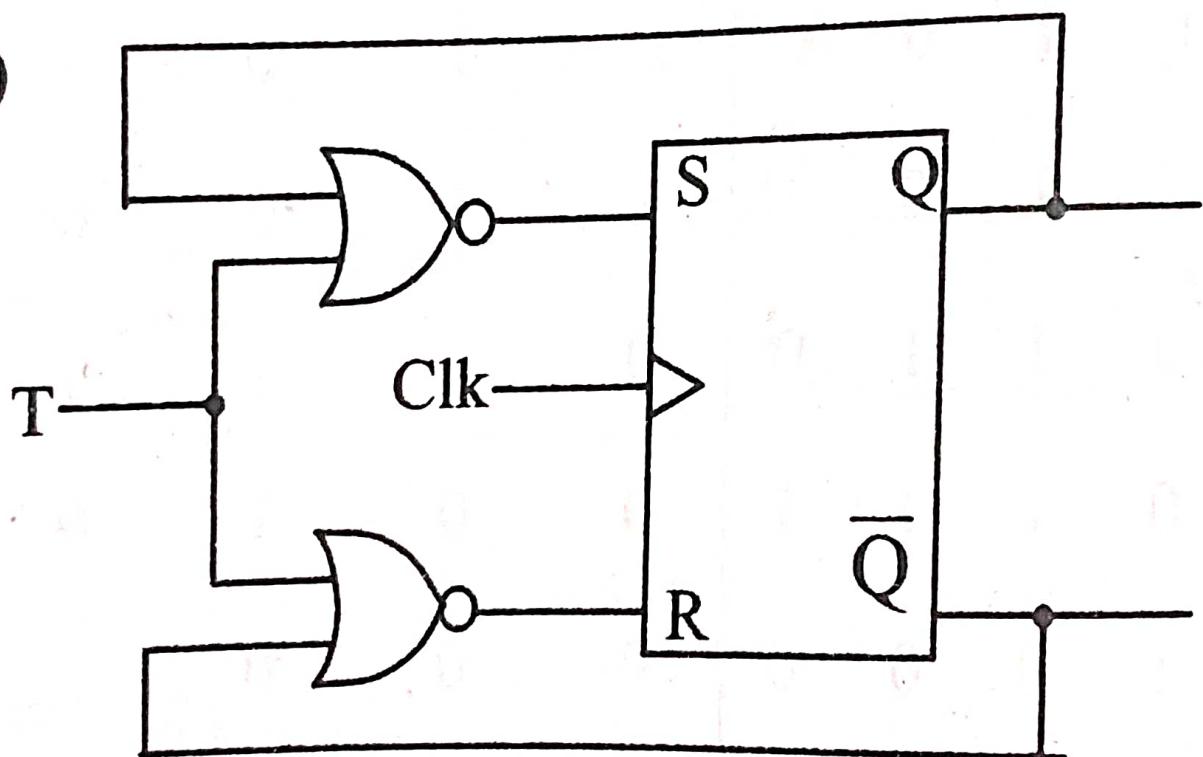
(b)



(c)



(d)

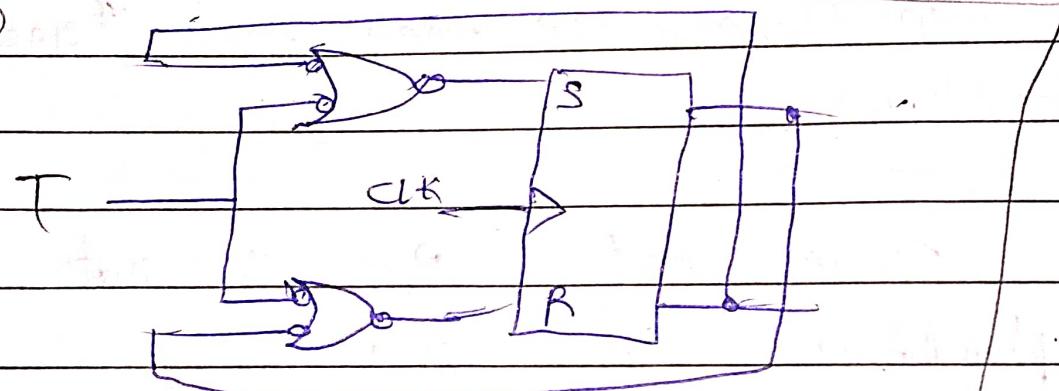


(b) 3 Convert SR to T-

T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

$$S = T \bar{Q}_n, \quad R = T Q_n$$

b)



04. What are the contents of Q_1 & Q_0 after 78th clock pulse. Initially the contents are

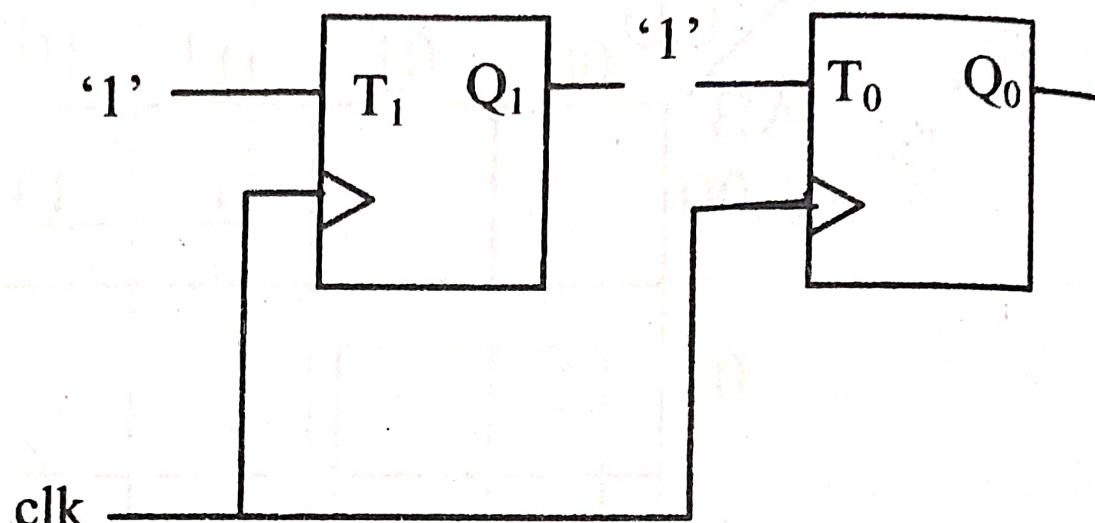
$$Q_1 = 0, Q_0 = 0$$

(a) 00

(b) 01

(c) 10

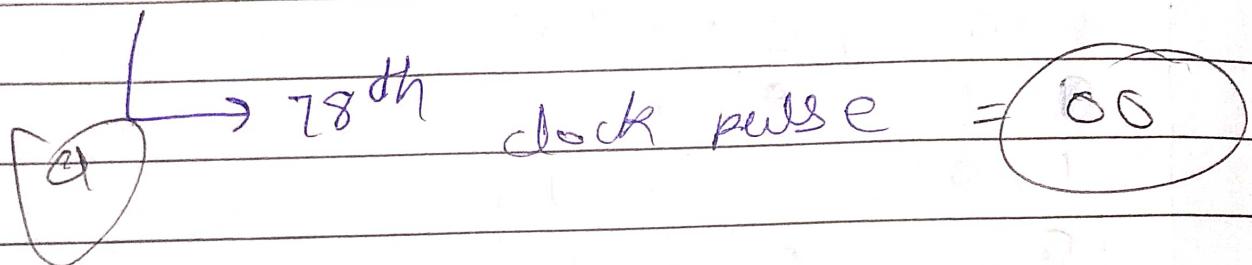
(d) 11



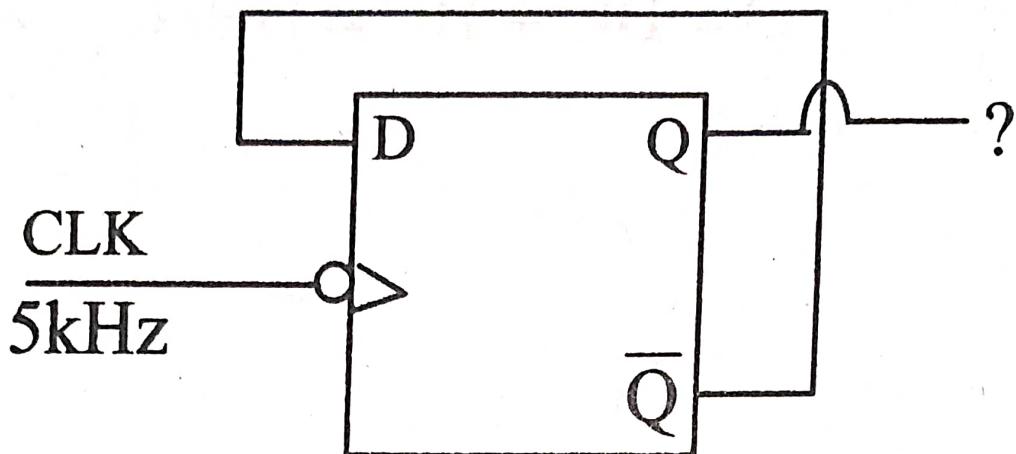
(a) $4 \Rightarrow$

odd clock pulse - $Q_1 Q_0 = 11$

even clock pulse - $Q_1 Q_0 = 00$



05. The output signal frequency of the circuit shown below is _____ if the input clock signal frequency is 5 KHz.

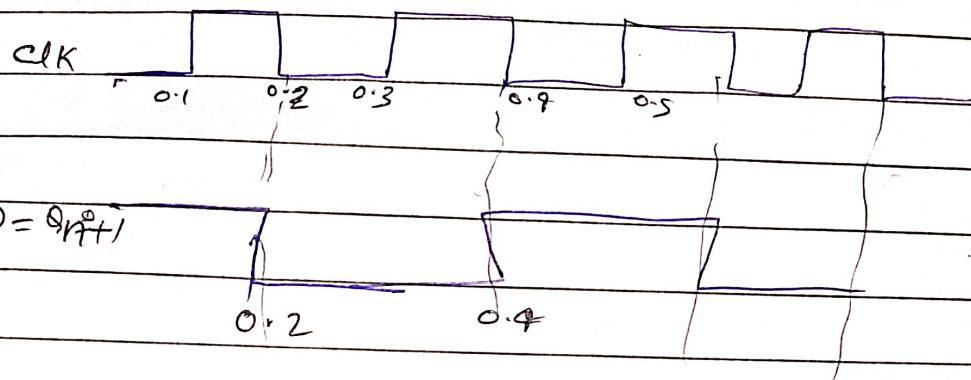


- (a) 1 KHz
- (b) 2 KHz
- (c) 2.5 KHz
- (d) 5 KHz

(C) \Rightarrow

$$\textcircled{1} = Q_{n+1}, f = 5 \text{ kHz}, T = 1/f = 0.2 \text{ msec}$$

$$\textcircled{2} = 0, Q_0 = D = 1$$

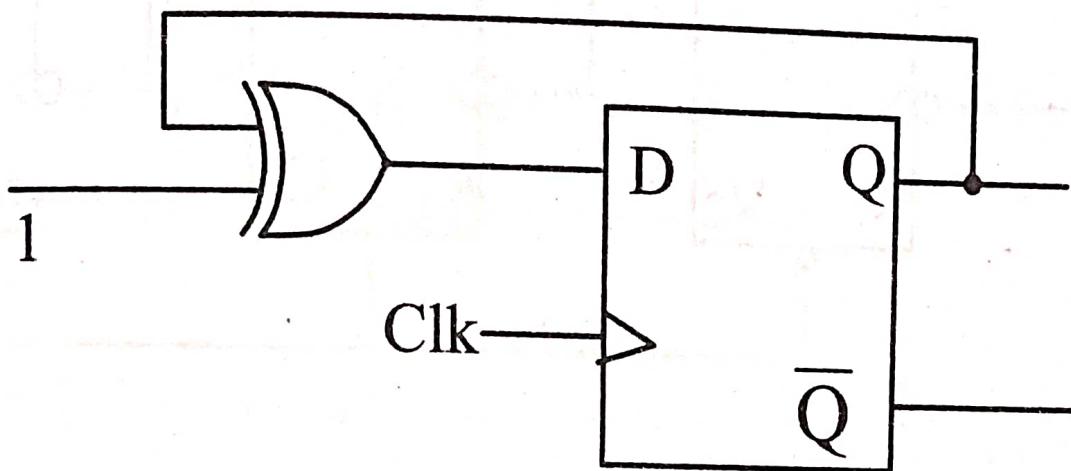


$$D = Q_{n+1}$$

$$f = \frac{1}{T} = \frac{1}{0.4} = (2.5 \text{ kHz})$$

(C) 2.5 kHz

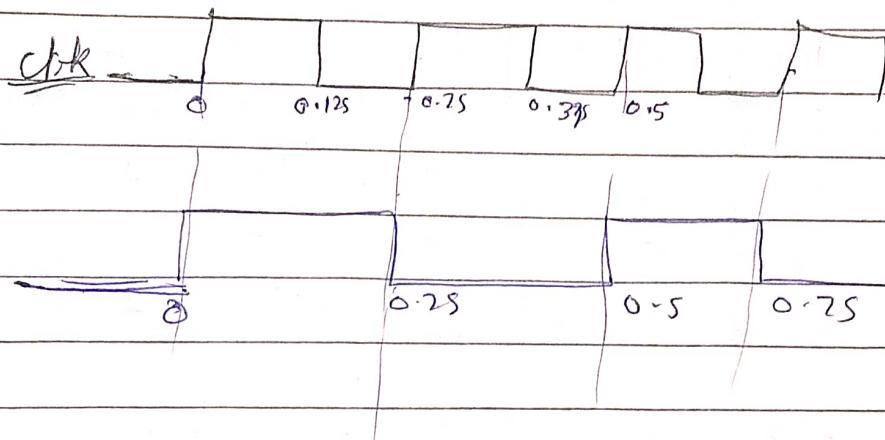
06. What is the output of the flip – flop shown in the fig., if the clock frequency is 4 KHz



- (a) output is always at 0
- (b) output is always at 1
- (c) output is always a signal with 2 KHz frequency
- (d) output is same as clock signal with 4 KHz frequency

Q) 68

$$f = 4, T = \frac{1}{f} = 0.25 \text{ m-sec.}$$

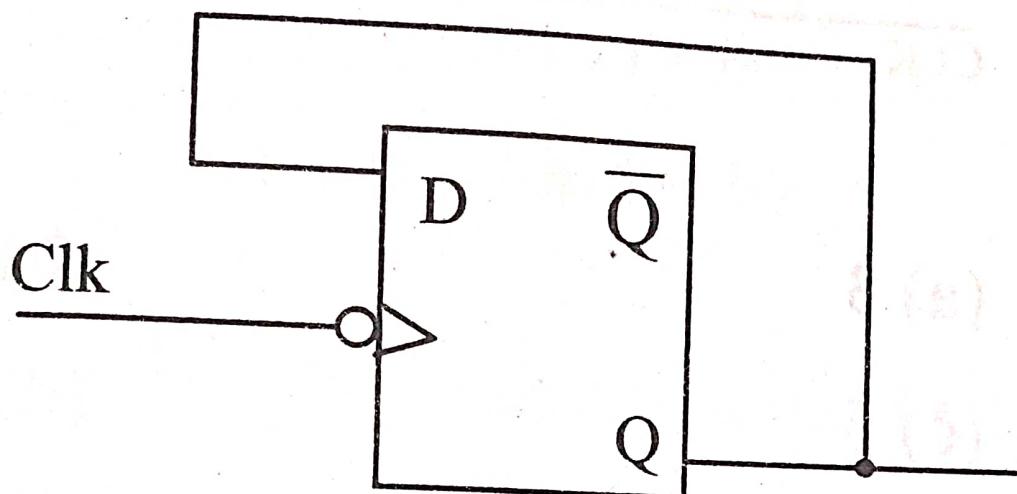


$$T = 0.5 \text{ m-sec}, f = \frac{1}{T} = \frac{1}{0.5} = 2 \text{ KHz}$$

C)

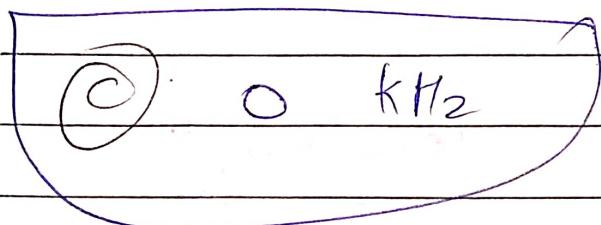
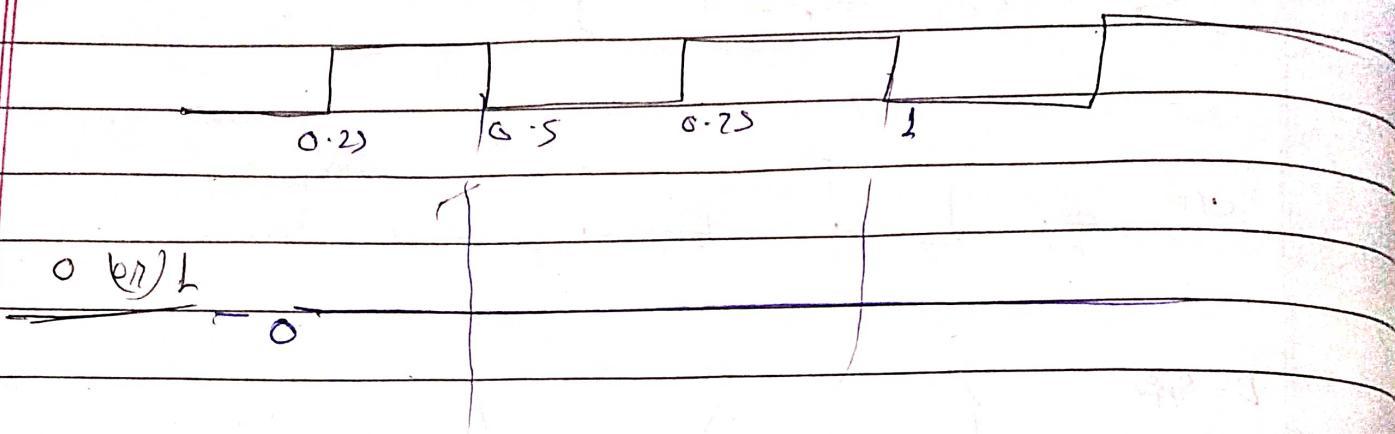
2 KHz Frequency

07. The input clock signal frequency is 2 kHz.
Then the output signal frequency of the
Circuit is ?



- (a) 1 KHz
- (b) 2 KHz
- (c) 0 KHz
- (d) Can not be determined

① $T =$ $f = 2 \text{ kHz}$, $T = 0.5 \text{ m-sec.}$



08. An A-B flip-flop whose characteristic table is given below is to be implemented using J-K flip-flop this can be done by making

A	B	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q_n}$
1	1	0

- (a) $J = \overline{B}$, $K = A$
- (b) $J = A$, $K = B$
- (c) $J = A$, $K = \overline{B}$
- (d) $J = B$, $K = \overline{A}$

④ 8-8

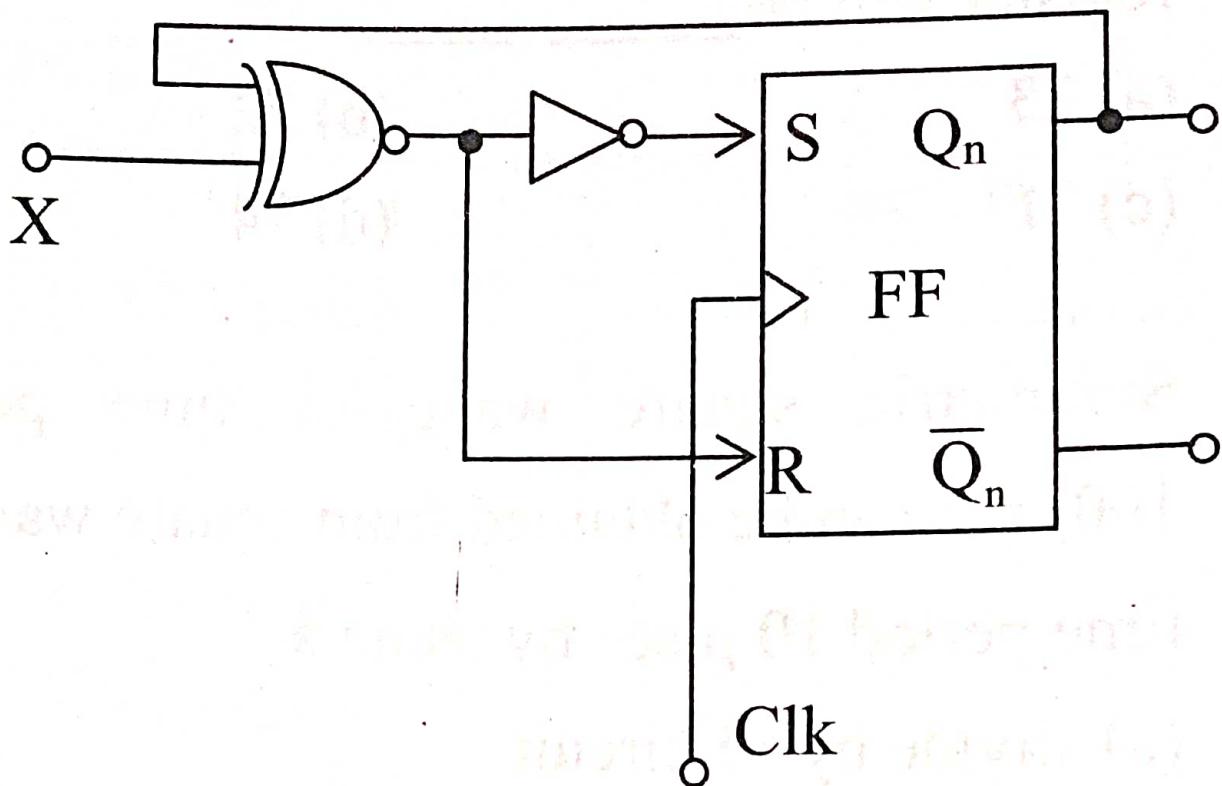
A	B	\mathcal{G}_n	\mathcal{G}_{n+1}	J	K
0	0	0	1	1	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	1	x	0
1	0	0	1	1	x
1	0	1	0	x	1
1	1	0	0	0	x
1		1	0	x	1

$$J = \bar{A} \bar{B} \mathcal{G}_n + A \bar{B} \bar{\mathcal{G}}_n = (\bar{B} \mathcal{G}_n)$$

$$K = A \bar{B} \mathcal{G}_n + A B \bar{\mathcal{G}}_n = (A \mathcal{G}_n)$$

a) $J = \bar{B}$
 $K = A$

09. A S-R Flip-Flop is converted into X-Flip-Flop as shown below.



The characteristic equation is

- (a) $\overline{X \oplus Q_n}$
- (b) $X + Q_n$
- (c) $X \oplus Q_n$
- (d) $X Q_n$

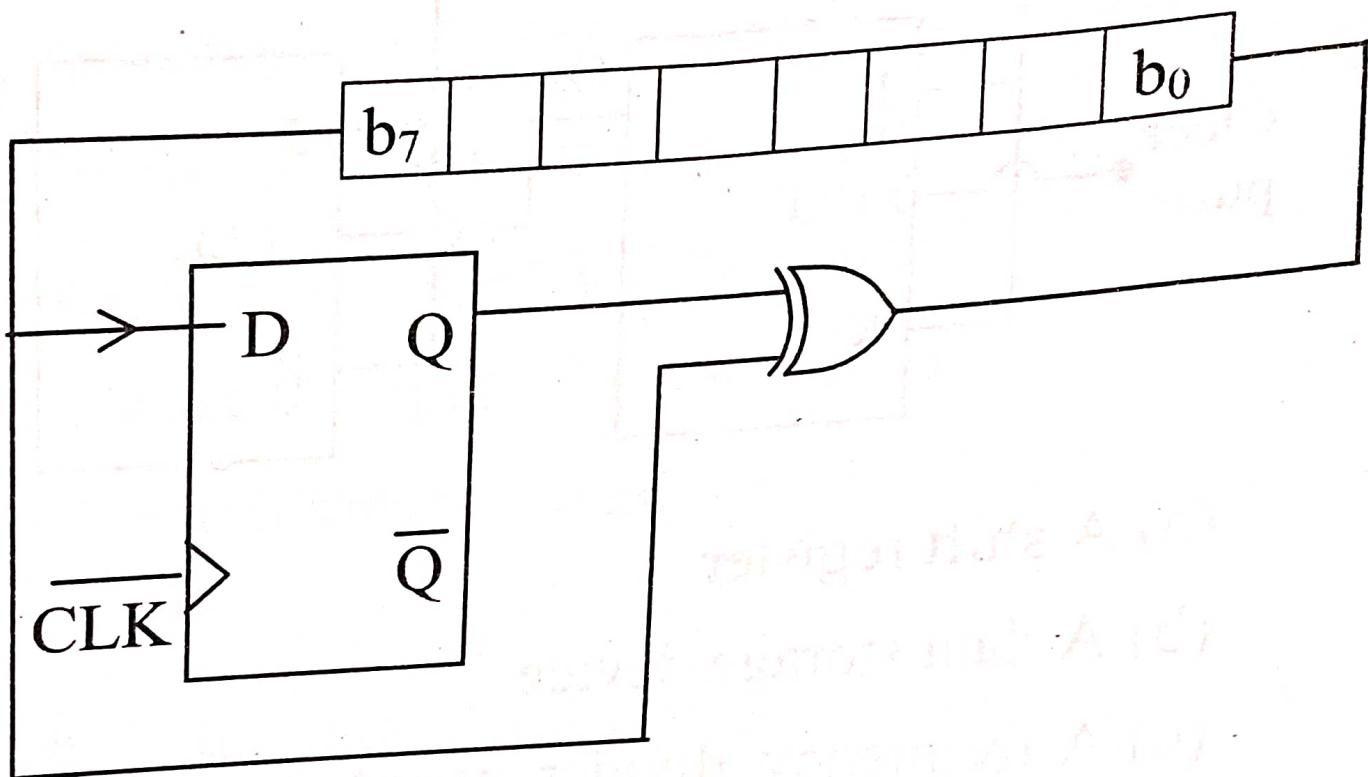
(c) 98

x_n	q_n	s	r	q_{n+1}
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	2	0	1	0

(d) $q_{n+1} = x q_n + \cancel{x} \bar{q}_n = \boxed{x q_n}$

Linked Answer Questions 10 & 11

The 8-bit left shift register and D flip-flop shown in the figure is synchronized with same clock. The D flip-flop initially cleared.



10. The circuit act as

- (a) Binary to 2's complement converter
- (b) Binary to gray code converter
- (c) Binary to 1's complement converter
- (d) Binary to Excess-3 code converter

Common 1011

(b) 1011

$b_7 \quad b_6 \quad b_5 \quad b_4 \quad b_3 \quad p_2 \quad p_1 \quad b_0$

$p_7 \quad b_7 \oplus p_6 \quad b_6 \oplus b_5 \quad b_5 \oplus b_4 \quad b_4 \oplus b_3 \quad b_3 \oplus p_2 \quad p_2 \oplus b_1 \quad b_1 \oplus b_0$

Binary group

(b)

binary gray code converter

11. If the initial content of register is 10110111
then after 4 clock pulses, the content of
register will be _____.

- | | |
|--------|--------|
| (a) 73 | (b) 72 |
| (c) 7E | (d) 74 |

		128	64	32	<u>16 8</u>	9	2	1
<u>Q</u> (11-8)		<u>clk</u>	1	0	1	1	0	1
1		0	1	1	0	1	1	1
2		1	1	0	1	1	1	1
3		1	0	1	1	1	1	1
4		0	1	1	1	1	1	1
		7	E					
								Teacher's Signature <u>7E</u>

12. Symmetric square wave of time period $100\mu\text{sec}$ can be obtained from square wave of time period $10 \mu\text{ sec}$ by using a
- (a) divide by -5 circuit
 - (b) divide by -2 circuit
 - (c) divide by -5 followed by a divide by -2 circuit
 - (d) None of these

~~(C) 12.8~~ $T_{out} = \frac{T_{in}}{MOD \cdot NO.}$

$T_{out} =$

$$MOD \cdot NO. = \frac{T_{out}}{T_{in}} \Rightarrow \frac{100}{10} = 10.$$

~~(C)~~ divide by -s followed by -z circuit