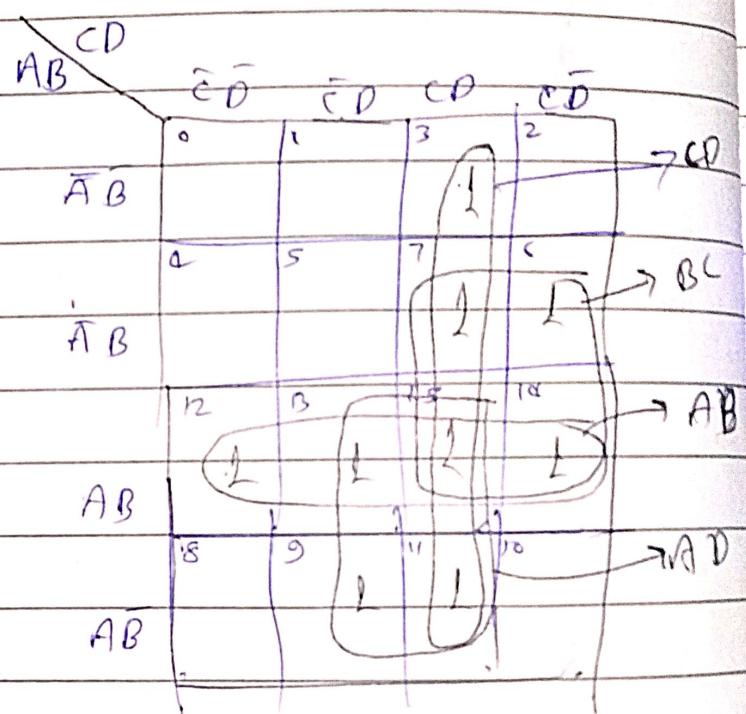


11. Design a logic circuit with 4 inputs A, B, C, D  
that will produce output '1' only whenever  
two adjacent input variables are 1's. A and D  
also to be treated as adjacent.

- (a)  $F = AC + AD + BD + AB$
- (b)  $F = \overline{AC} + \overline{AD} + AC + BD$
- (c)  $F = AB + AD + BC + CD$
- (d)  $F = \overline{AB} + \overline{AD} + BC + CD$

(c)  $\sum m = 9$  i/p  $\rightarrow ABCD$ ,  $O(P \rightarrow L)$ ,  $A, D \rightarrow \text{Adje.}$

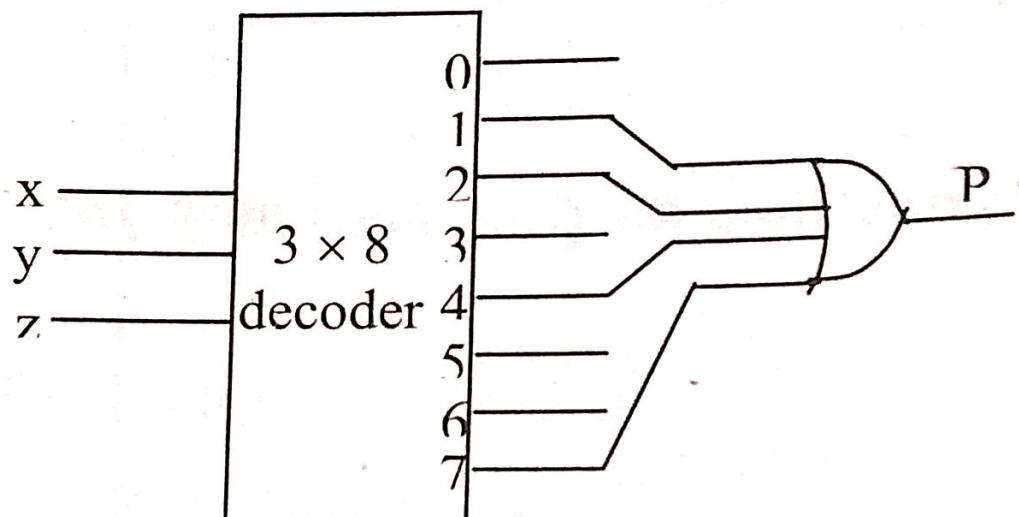
Des	A	B	C	D	F
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1



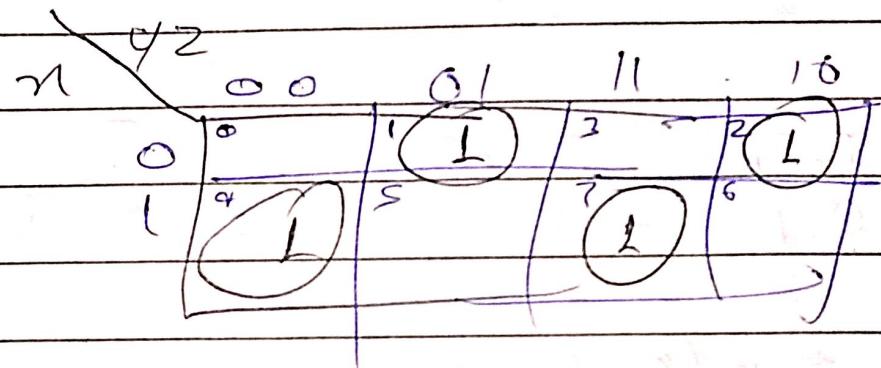
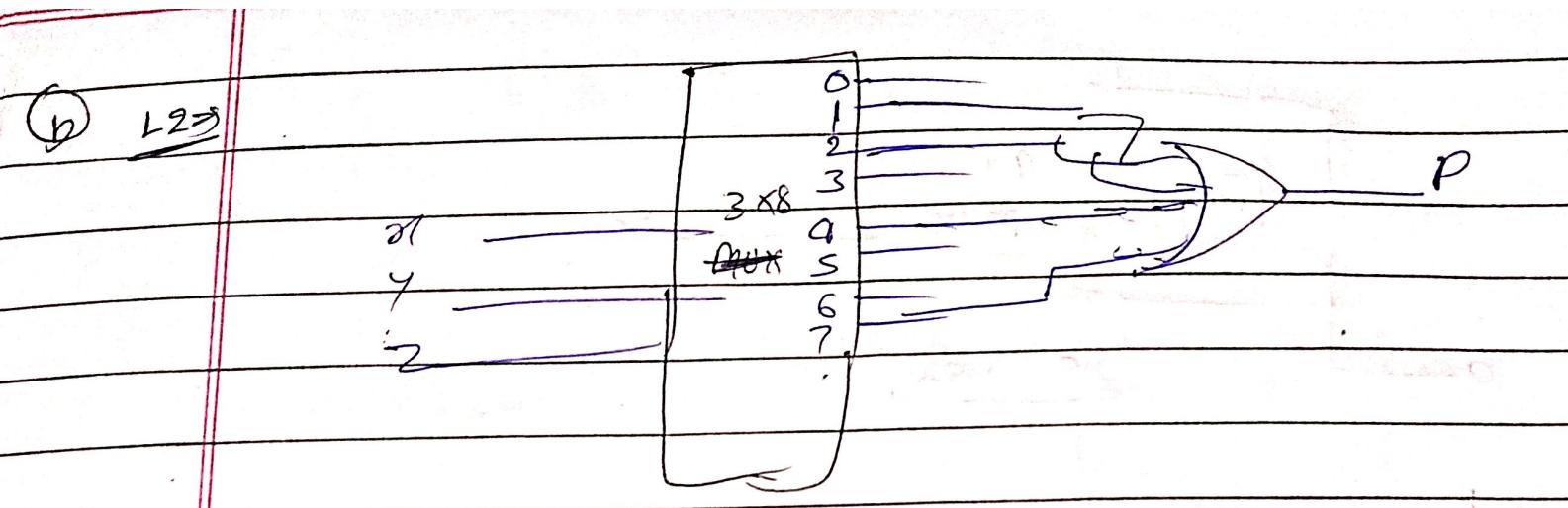
$$F = AB + BC + CD + AD$$

Teacher's Signature .....

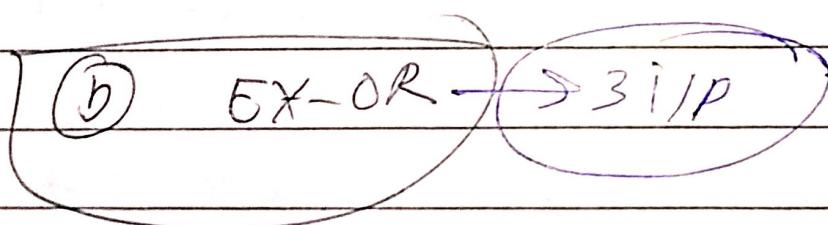
12. The circuit shown below is



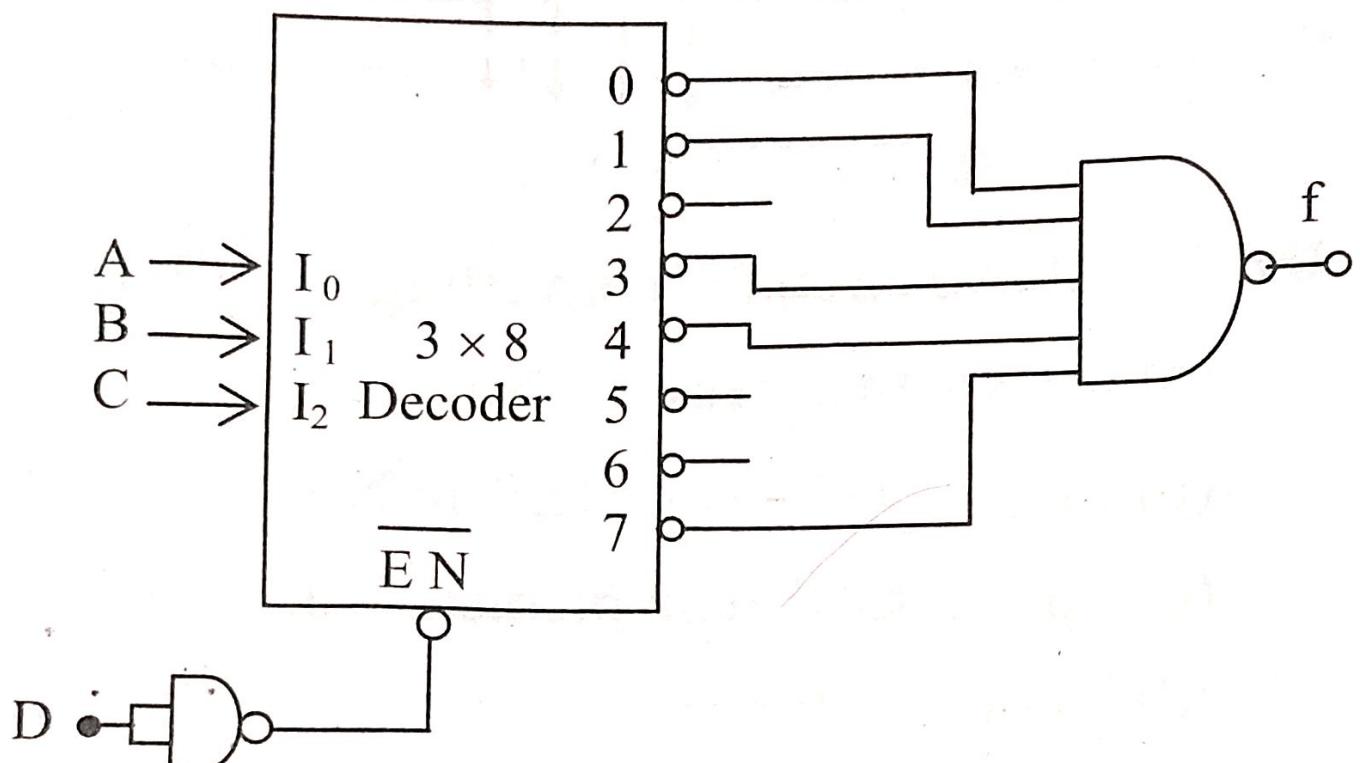
- (a) Full Adder
- (b) 3 input Ex - OR gate
- (c) Half Adder
- (d) 3 input Ex - NOR gate



$$F = x \oplus y \oplus z$$



13. The output function 'f' of the given logic circuit is



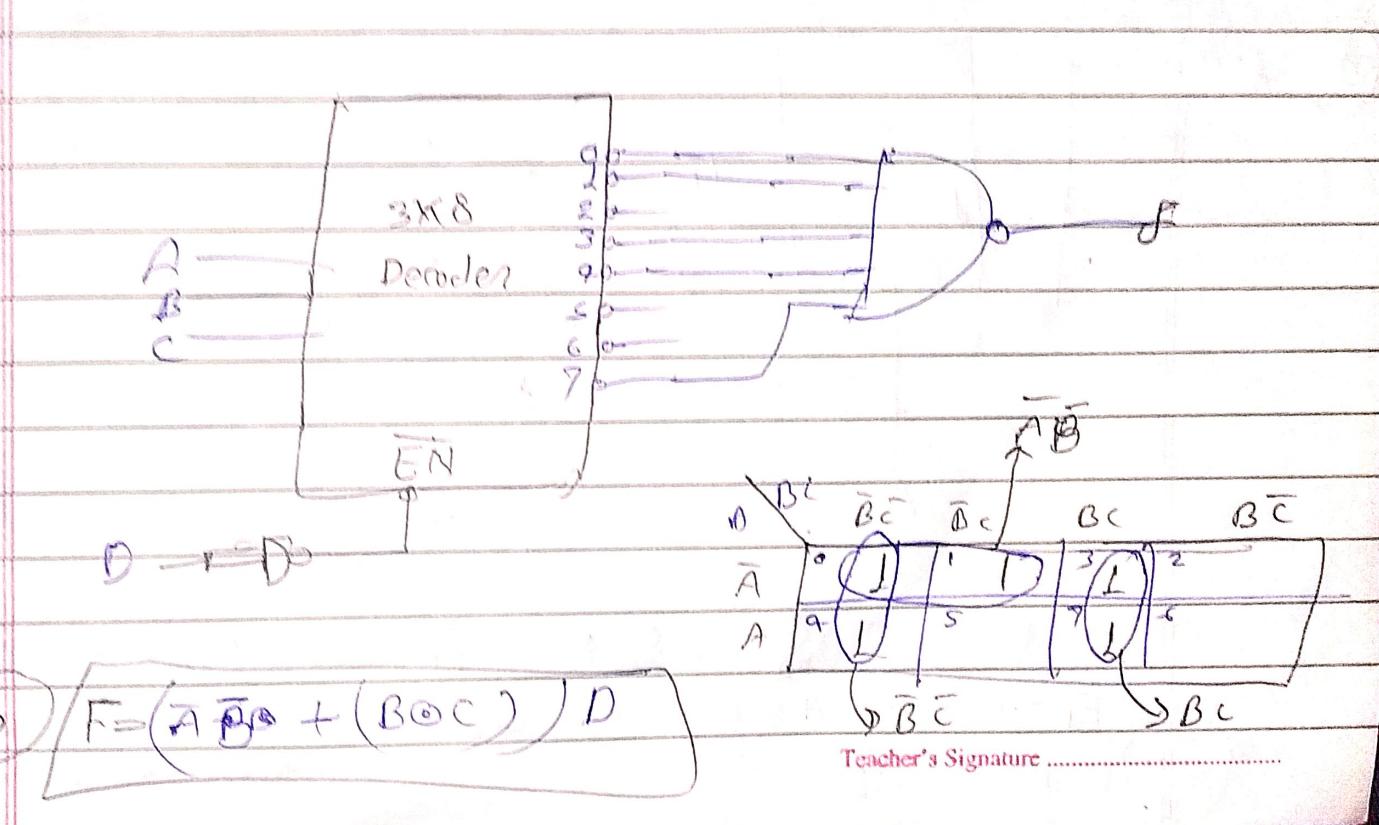
$$(a) (A \odot C + \overline{A} \overline{C})D$$

$$(b) (B \odot C + \overline{A} \overline{B})D$$

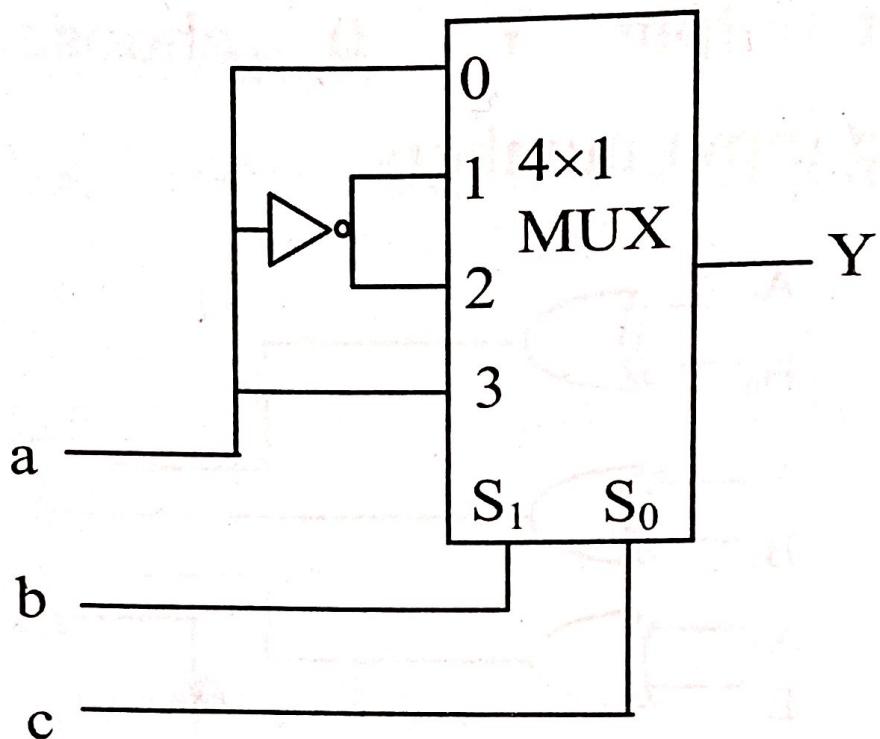
$$(c) (B \oplus C + \overline{A} \overline{C})D$$

$$(d) (A \oplus B + \overline{A} \overline{B})D$$

(a) 138

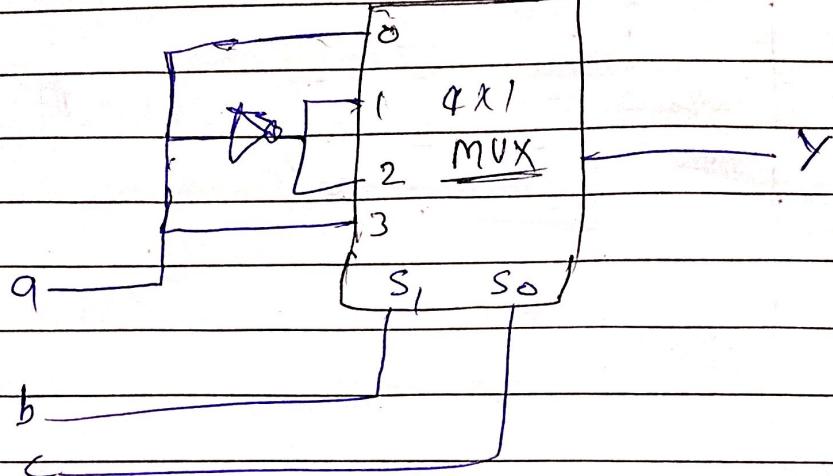


14. The following multiplexer circuit is equivalent to \_\_\_\_\_.



- (a) Implementation of sum equation of full adder
- (b) Implementation of carry equation of full adder
- (c) Implementation of Borrow equation of full subtractor
- (d) All the above

@ 19



$$F = I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 + I_3 S_1 S_0$$

$$F = \bar{a} \bar{b} \bar{c} + \bar{a} \bar{b} c + \bar{a} b \bar{c} + a b \bar{c}$$

$$F = \sum m(4, 1, 2, 7)$$

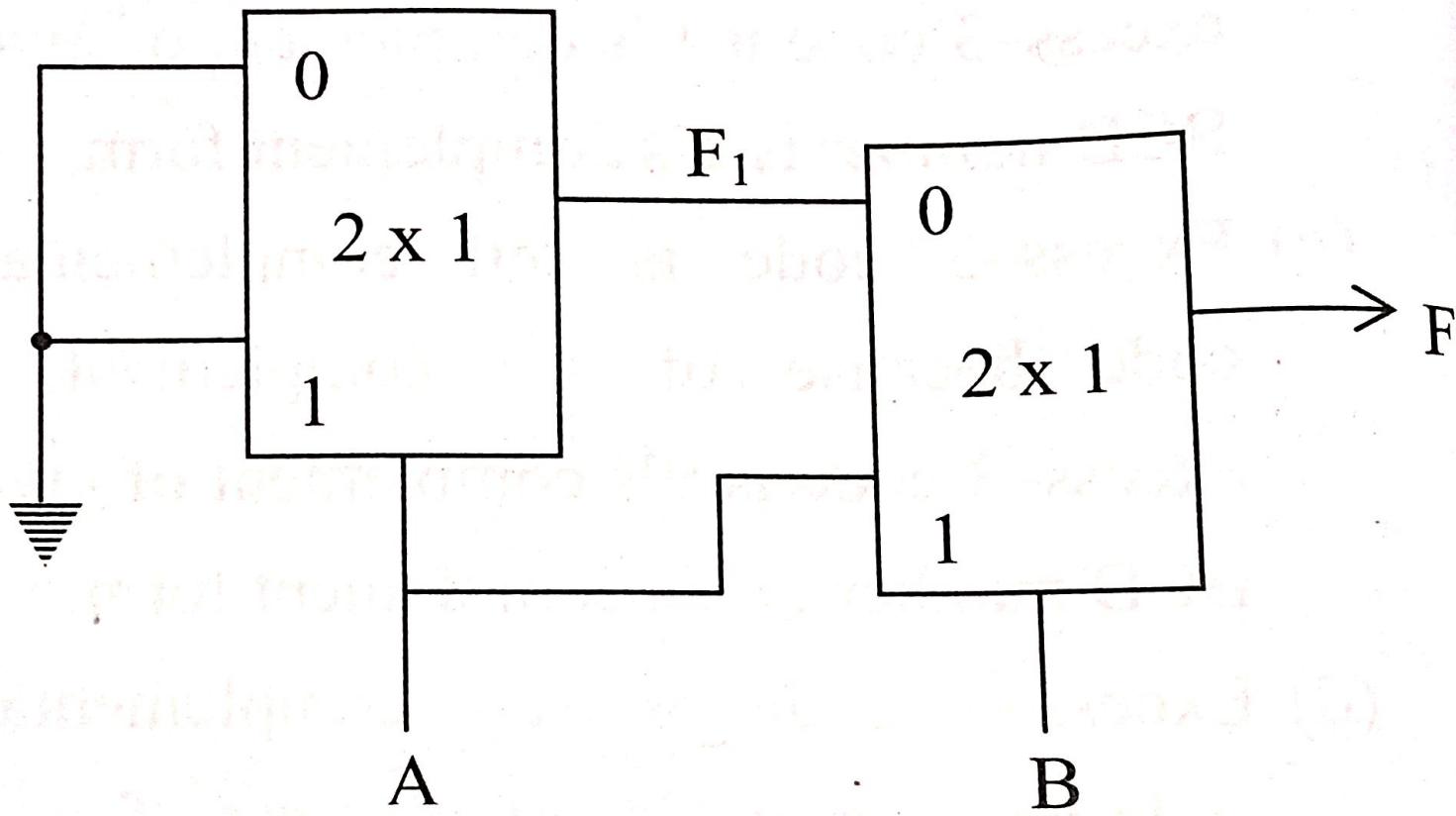
$$\underline{F = \sum m(1, 2, 4, 7)}$$

→ sum of full adder

(a)

Implementation of sum eq<sup>n</sup> of FA

15. Identify the operation of circuit shown in figure.

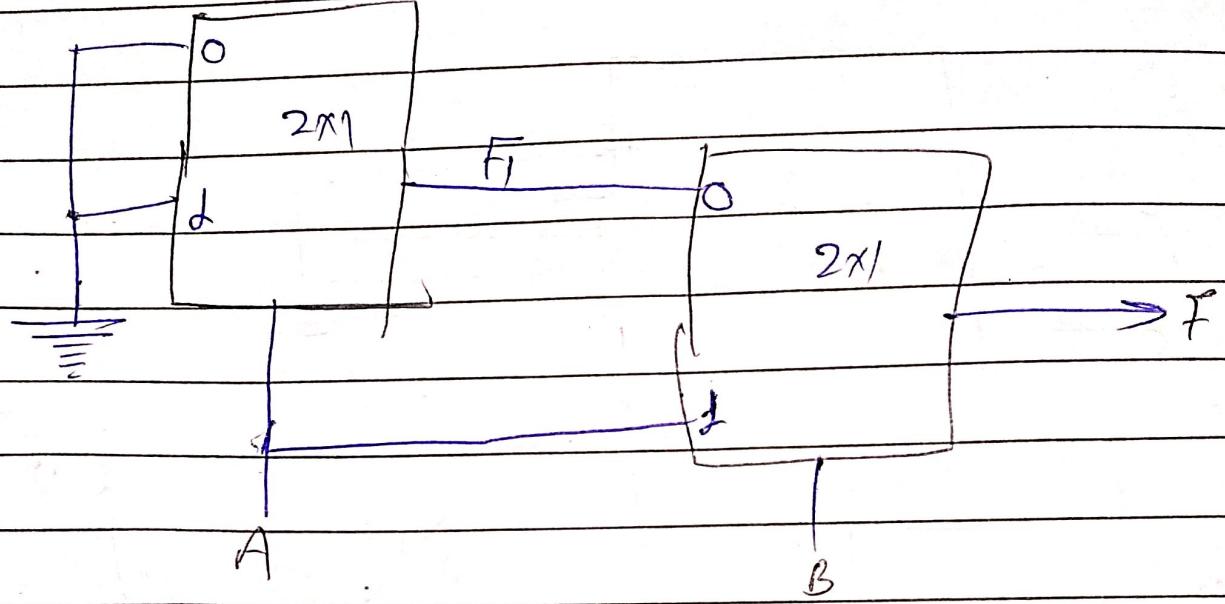


- (a)  $F = A \oplus B$
- (c)  $F = A \odot B$

- (b)  $F = A + B$
- (d)  $F = AB$

(d)

153



$$F = (I_0 \times \bar{S}_0 + I_1 \times \bar{S}_1) = F_1 \times AB + AB$$

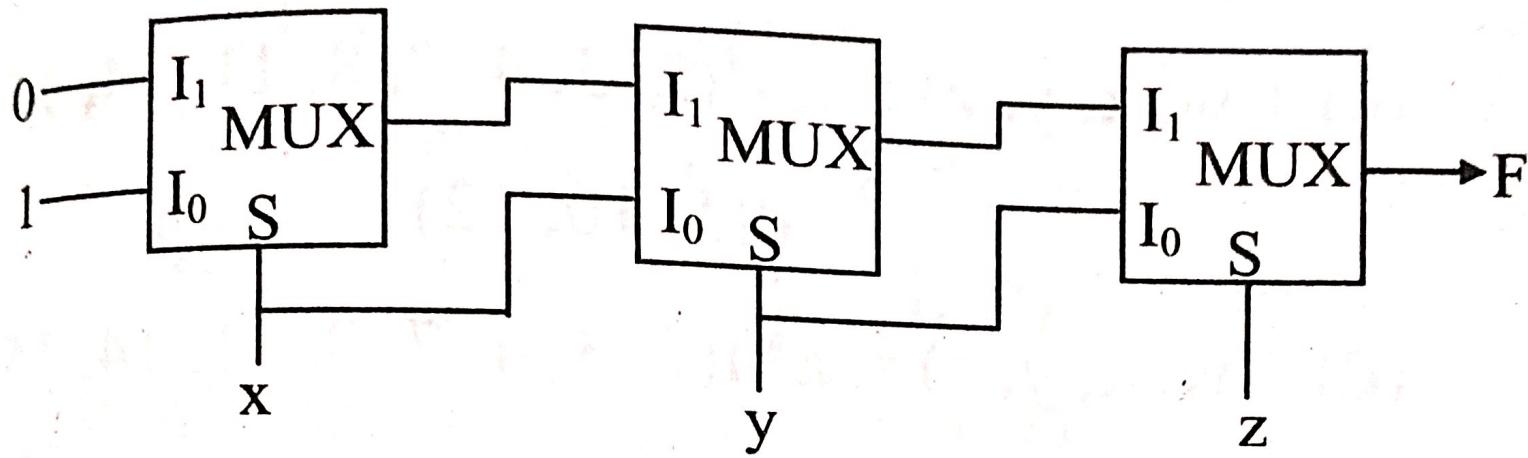
$$F_1 = 0 \cdot \bar{A} + 0 \cdot A = 0, \quad F_2 = 0 \cdot \bar{B} + A \bar{B}$$

(d)

$$\boxed{F_2 = AB}$$

Teacher's Signature .....

16. The output equation of the following digital circuit is



(a)  $F(x, y, z) = \sum m(1, 2, 4, 7)$

(b)  $F(x, y, z) = \sum m(2, 3, 4, 5)$

(c)  $F(x, y, z) = \sum m(2, 5, 6, 7)$

(d)  $F(x, y, z) = \sum m(1, 3, 5, 7)$

c)  $\xrightarrow{16 \Rightarrow}$

$$F = \mathbb{F}_0 S + \mathbb{I}_1 S$$

$$F_1 = 0 \cdot \bar{x} + 1 \cdot x = x$$

$$F_2 = F_1 \cdot \bar{y} + \pi \cdot \bar{y} = \cancel{x} (\bar{y} + \bar{y}) = \cancel{x}$$

$$F_3 = F_2 \cdot z + y \bar{z} = xz + y \bar{z} = (\cancel{xy} + \cancel{xy})z + y \bar{z} (\pi + \bar{\pi})$$

$$F = F_3 = \underset{(7)}{xz} + \underset{(5)}{x\bar{y}z} + \underset{(6)}{\pi y\bar{z}} + \underset{(2)}{\bar{\pi}y\bar{z}}$$

(8)  $F = \sum m(2, 5, 6, 7)$

17. **Assertion (A) :** A demultiplexer can be used as decoder.

**Reason (R) :** A demux selects one of many outputs where as a decoder selects an output corresponds to the coded input.

Q17 A): A de-mux can be used as decoder.

R): A demux selects one of many o/p's where as a decoder selects an o/p corresponds to the coded input.

Sol

A demux can be used as a decoder  
A demux selects one of many o/p's where as a decoder selects an o/p corresponding to the coded i/p.

## *Common Data for Questions 18 & 19*

It is required to implement a  $16 \times 1$  multiplexer.

Common

18 & 19

Implement

16x1

min -

- (c) 28) The no. of 2x1 min required to implement  
16x1 min -

$$\begin{array}{c|c|c|c} \frac{16}{2} = 8 & \frac{8}{2} = 4 & \frac{4}{2} = 2 & \frac{2}{2} = 1 \end{array}$$

$$8 + 4 + 2 + 1 =$$

15

(a) 15

- (a) 29) no. of 4x1 min required -

$$\begin{array}{c|c} \cancel{\frac{16}{4} = 4} & \cancel{\frac{8}{4} = 2} \\ \hline & 2 \end{array}$$

$$\begin{array}{c|c} \frac{16}{4} = 4 & \frac{4}{4} = 1 \end{array}$$

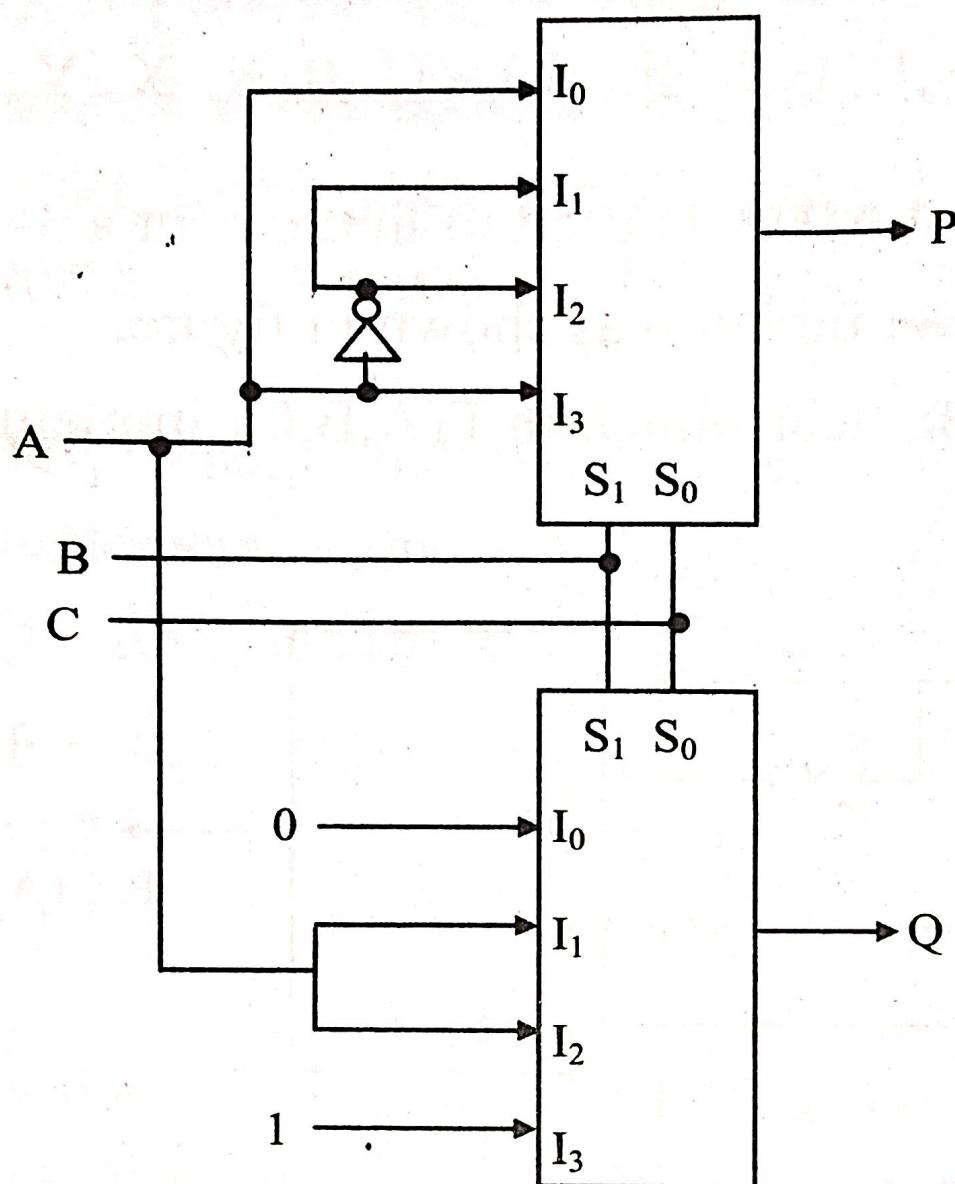
$$4 + 1 =$$

5

(a) 5

## **Linked Answer Questions 20 & 21**

Consider the combinational circuit shown below.



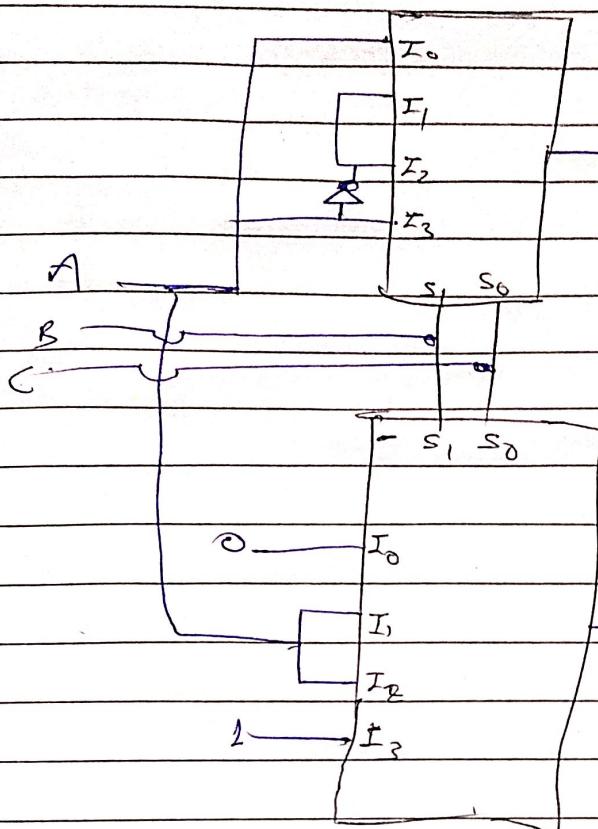
20. What is the circuit implemented in above diagram

- (a) Full Adder
- (b) Full Subtractor
- (c) Half Adder
- (d) Quarter Adder

21. Minimum number of two input NAND gates required to implement above circuit.

- (a) 8
- (b) 9
- (c) 10
- (d) 11

Common 20 & 21



$$\begin{aligned}
 P &= I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 \\
 &\quad + I_3 S_1 S_0 \\
 &= A \bar{B} \bar{C} + \bar{A} \bar{B} C + \bar{A} B \bar{C} \\
 &\quad + A B C \\
 &= A \oplus B \oplus C
 \end{aligned}$$

sum

$$\begin{aligned}
 Q &= \bar{I}_0 + A \bar{B} C + A B \bar{C} + I_1 \\
 &= 0 + A (\bar{B} \oplus C) + B C
 \end{aligned}$$

carry

Q 20  $\Rightarrow$  Above diagram - ( Circuit implements )

(a) Full Adder

Q 21  $\Rightarrow$

minimum 2 i/p NAND gates

Full Adder  $\rightarrow$  9 NAND gates

(b) 9