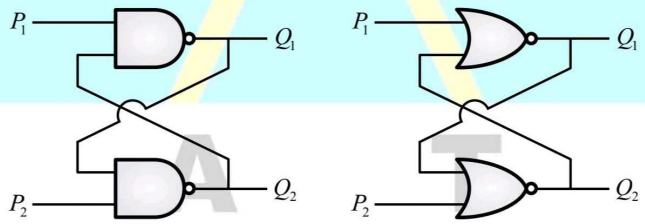
6. Sequential Circuit

Q.1 Refer to the NAND and NOR latches shown in the figure. The input (P_1, P_2) for both the latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable output (Q_1, Q_2) are

[GATE 2009, IIT Roorkee]



(A) NAND: first (0, 1) then (0, 1) NOR : first (1, 0) then (0, 0).

(B) NAND: first (1, 0) then (1, 0) NOR : first (1, 0) then (1, 0).

(C) NAND: first (1, 0) then (1, 0) NOR : first (1, 0) then (0, 0).

(D) NAND: first (1, 0) then (1, 1) NOR : first (0, 1) then (0, 1).

Q.2 Two D flip-flops are connected as a synchronous counter that goes through the following $Q_B\, Q_A$ sequence

$$00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \ldots$$

The connections to the inputs D_A and D_B are **[GATE 2011, IIT Madras]**

(A) $D_A = Q_B,\ D_B = Q_A$

(B) $D_A = \overline{Q}_A,\ D_B = \overline{Q}_B$

(C) $D_A = (Q_A\overline{Q}_B + \overline{Q}_A Q_B), D_B = Q_A$

(D) $D_A = (Q_A Q_B + \overline{Q}_A\overline{Q}_B), D_B = \overline{Q}_B$

Q.3 The next state table of a 2-bit saturating up- counter is given below.

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expression for T_1 and T_0 are

[GATE 2017, IIT Roorkee]

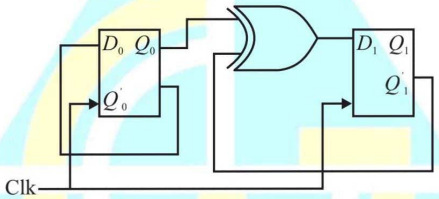
(A) $T_1 = Q_1Q_0, T_0 = \overline{Q_1}\,\overline{Q_0}$

(B) $T_1 = \overline{Q_1}Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(C) $T_1 = Q_1 + Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(D) $T_1 = \overline{Q_1}Q_0, T_0 = Q_1 + Q_0$

Q.4 Consider the following circuit.

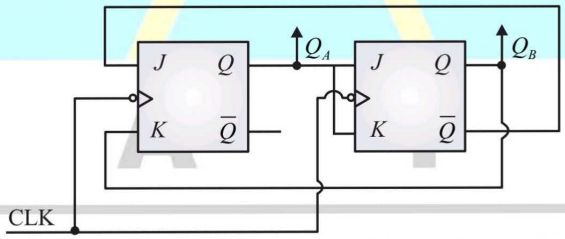


The flip-flops are positive edge triggered D FFs. Each state is designated as a two bit string Q_0Q_1. Let the initial state be 00. The state transition sequence is

[GATE 2005, IIT Bombay]

(A) $00 \rightarrow 11 \rightarrow 01$ (B) $00 \rightarrow 11$ (C) $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$ (D) $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

Q.5 A 2-bit counter circuit is shown below,

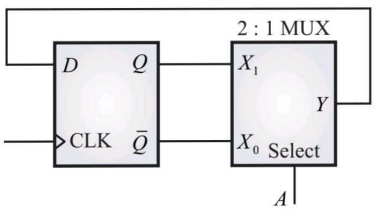


If the state $Q_A\,Q_B$ of the counter at the clock time t_n is "10" then the state Q_AQ_B of the counter at $t_n + 3$ (after three cycles) will be

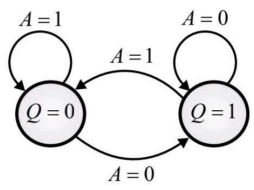
[GATE 2011, IIT Madras]

(A) 00 (B) 01 (C) 10 (D) 11

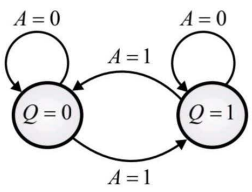
Q.6 The state transition diagram for the logic circuit shown is **[GATE 2012, IIT Delhi]**



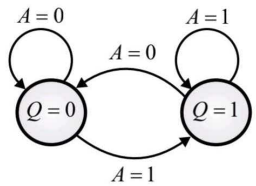
(A)



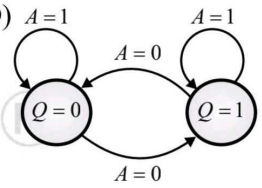
(B)



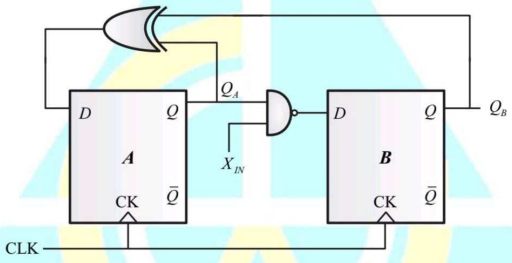
(C)



(D)



Q.7 A finite state machine (FSM) is implemented using the *D* flip-flops *A* and *B* and logic gates, as shown in the figure below. The four possible states of the FSM are Q_AQ_B = 00, 01, 10 and 11.



Assume that X_{IN} is held at a constant logic level throughout the operation of the FSM. When the FSM is initialized to the state Q_AQ_B = 00 and clocked, after a few clock cycles, it starts cycling through

[GATE 2017, IIT Roorkee]

(A) all of the four possible states if X_{IN} = 1.

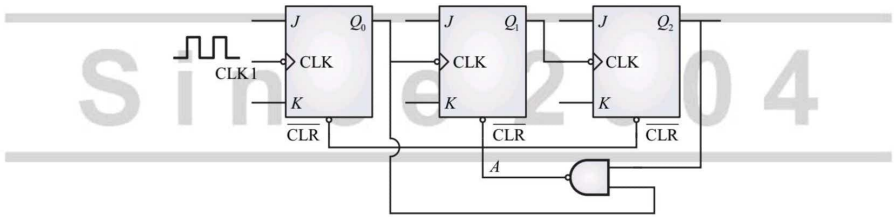
(B) three of the four possible states if X_{IN} = 0.

(C) only two of the four possible states if X_{IN} = 1.

(D) only two of the four possible states if X_{IN} = 0.

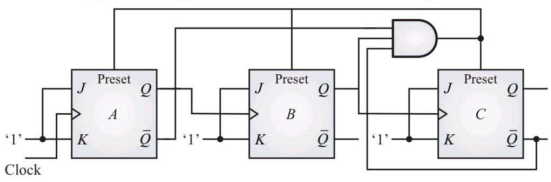
Q.8 The ripple counter shown in figure is made up of negative edge triggered *J-K* flip-flops. The signals levels at *J* and *K* inputs of all the flip-flops are maintained at logic 1. Assume all the outputs are cleared just prior to applying the clock signal. Module number of the counter is

[GATE 2002, IISc Bangalore]



(A) 7 (B) 5 (C) 4 (D) 8

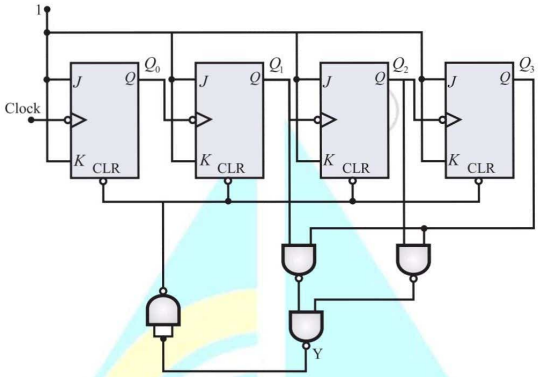
Q.9 The ripple counter shown in the given figure is works as a **[GATE 1999, IIT Bombay]**



(A) MOD-3 up counter.
(B) MOD-5 up counter.
(C) MOD-3 down counter.
(D) MOD-5 down counter.

Common Data for Questions 10 & 11

Consider the counter circuit shown below.



Q.10 In the above figure, Y can be expressed as

[GATE 2008, IISc Bangalore]

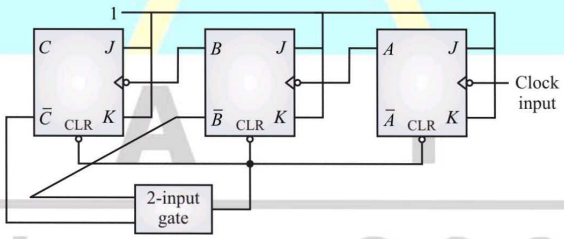
(A) $Q_3.(Q_1+Q_2)$
(B) $Q_3+Q_1.Q_2$
(C) $\overline{Q_3.(Q_1+Q_2)}$
(D) $\overline{Q_3+Q_1.Q_2}$

Q.11 The above circuit is a

[GATE 2008, IISc Bangalore]

(A) Mod-8 Counter
(B) Mod-9 Counter
(C) Mod-10 Counter
(D) Mod-11 Counter

Q.12 In the modulo-6 ripple counter shown in below, figure the output of the 2-input gate is used to clear the *J-K* flip-flops.



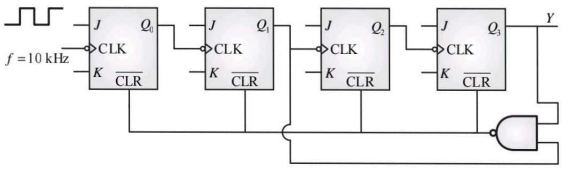
The 2-input gate is

[GATE 2004, IIT Delhi]

(A) a NAND gate
(B) a NOR gate
(C) an OR gate
(D) an AND gate

Q.13 In the figure, the *J* and *K* inputs of all the four flip-flops are made high. The frequency of the signal at output *Y* is

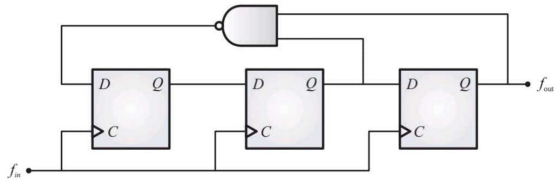
[GATE 2000, IIT Kharagpur]



(A) 0.833 kHz
(B) 1.0 kHz
(C) 0.91 kHz
(D) 0.77 kHz

Q.14 Which one of the following statements is true about the digital circuit shown in the figure.

[GATE 2018, IIT Guwahati]



(A) It can be used for dividing the input frequency by 3.

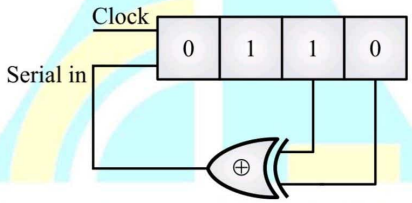
(B) It can be used for dividing the input frequency by 5.

(C) It can be used for dividing the input frequency by 7.

(D) It cannot be reliably used as a frequency divider due to disjoint internal cycles.

Q.15 The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in the figure is 0110. After three clock pulses are applied, the contents of the Shift Register will be

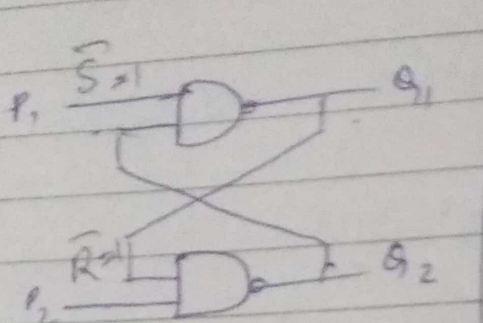
[GATE 1992, IIT Delhi]



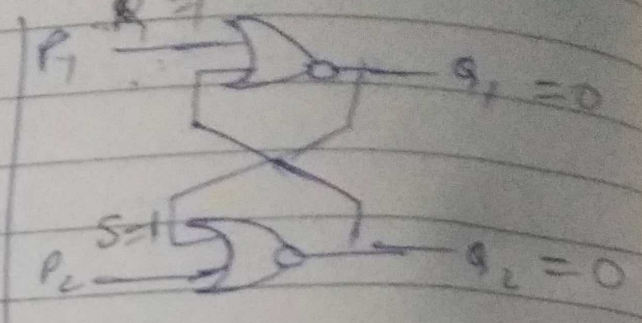
(A) 0000 (B) 0101 (C) 1010 (D) 1111

Sequential Circuit

1⇒



Hold



Invalid

(a) (i) NAND — (1,0) then (1,0)
NOR — (1,0) then (0,0)

Ans

2⇒ 00 → 11 → 01 → 10 → 00 → ——

(b) $D_A, D_B = ?$

Soln

Q_B	Q_A	Q_{B+1}	Q_{A+1}	D_B	D_A
0	0	0	1	1	1
0	1	1	0	1	0
1	0	0	0	0	0
1	1	0	1	0	1

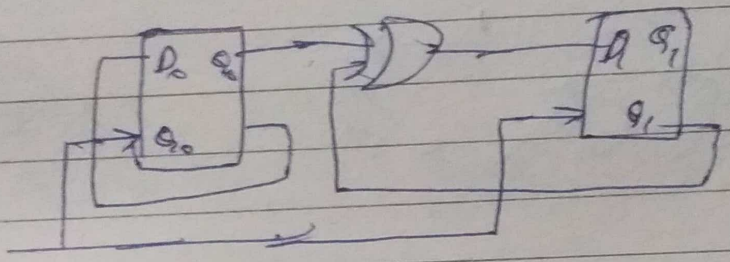
$D_A = (Q_A Q_B + \bar{Q}_A \bar{Q}_B)$, $D_B = \bar{Q}_B$

3.

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	0	0

$T_1 = \overline{Q_1} Q_0, \quad T_{0_2} = \overline{Q_1} + \overline{Q_0}$ Ans

4.



Q_0	Q_1	Q_0^+	Q_1^+
0	0	1	1
0	1	1	0
1	0	0	0
1	1	0	1

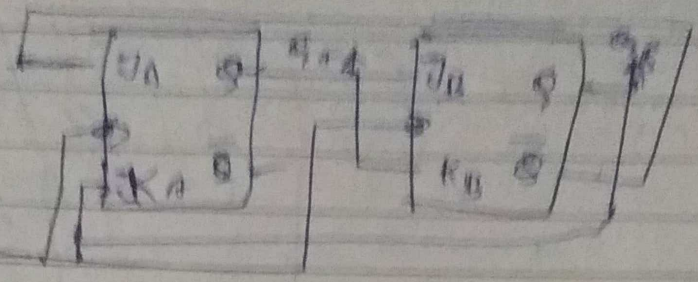
$Q_0^+ = D_0 = \overline{Q_0}$

$Q_1^+ = D_1$
$= Q_0 \oplus Q_1$
$= Q_0 \oplus Q_1$

00 → 11 → 01 → 10

Ans

5 ⇒



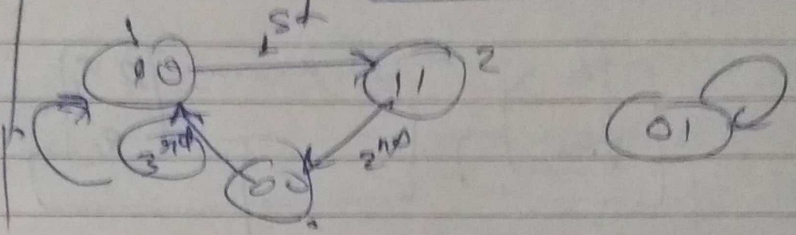
$Q_{A+1} = J_A\bar{Q}_A + \bar{K}_A Q_A$

$= \bar{Q}_B\bar{Q}_A + Q_B Q_A$

$= \bar{Q}_B$

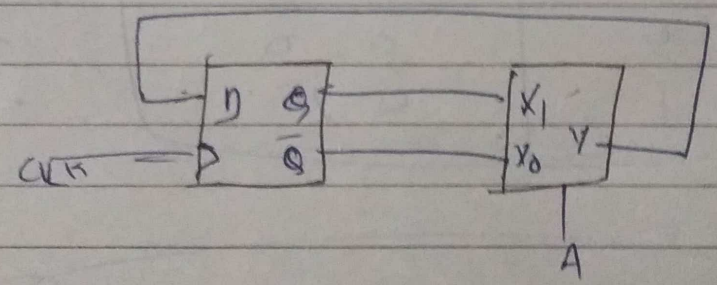
Q_A	Q_B	Q_{A+1}	Q_{B+1}
0	0	1	0
0	1	0	1
1	0	1	1
1	1	0	0

$Q_{B+1} = Q_B \oplus Q_A$



t_{3+n} = 10 Ans

6 ⇒



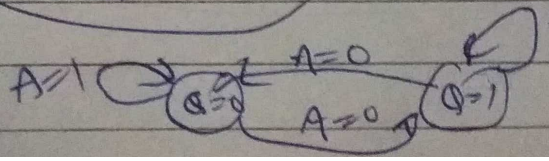
$Q_{n+1} = D = Y = \alpha_1$

$Q_{n+1} = Q_n$ A = 1

7

$Q_{n+1} = D = Y = X_0 = \bar{Q}_n$ A = 0

$Q_{n+1} = \bar{Q}_n$



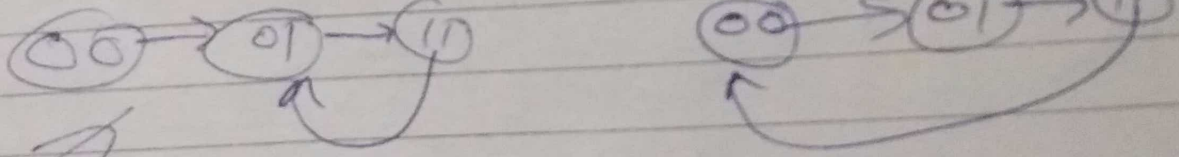
Q_A	Q_B	Q_{A+1}	Q_{B+1}
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	1

$Q_{A+1} = D_A = Q_A \oplus Q_B$ $\quad X_{in} = 0$

$Q_{B+1} = D_B = 1$

$Q_{A+1} = D_A = Q_A \oplus Q_B$ $\quad X_{in} = 1$

$Q_{B+1} = B_B = \overline{Q_A}$



2 step

→ Only 2 ~~step~~ of possible

if $X_{in} = 0$

Ans

(8)

Q_2	Q_1	Q_0	Q_2 Q_0
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	
1	1	1	

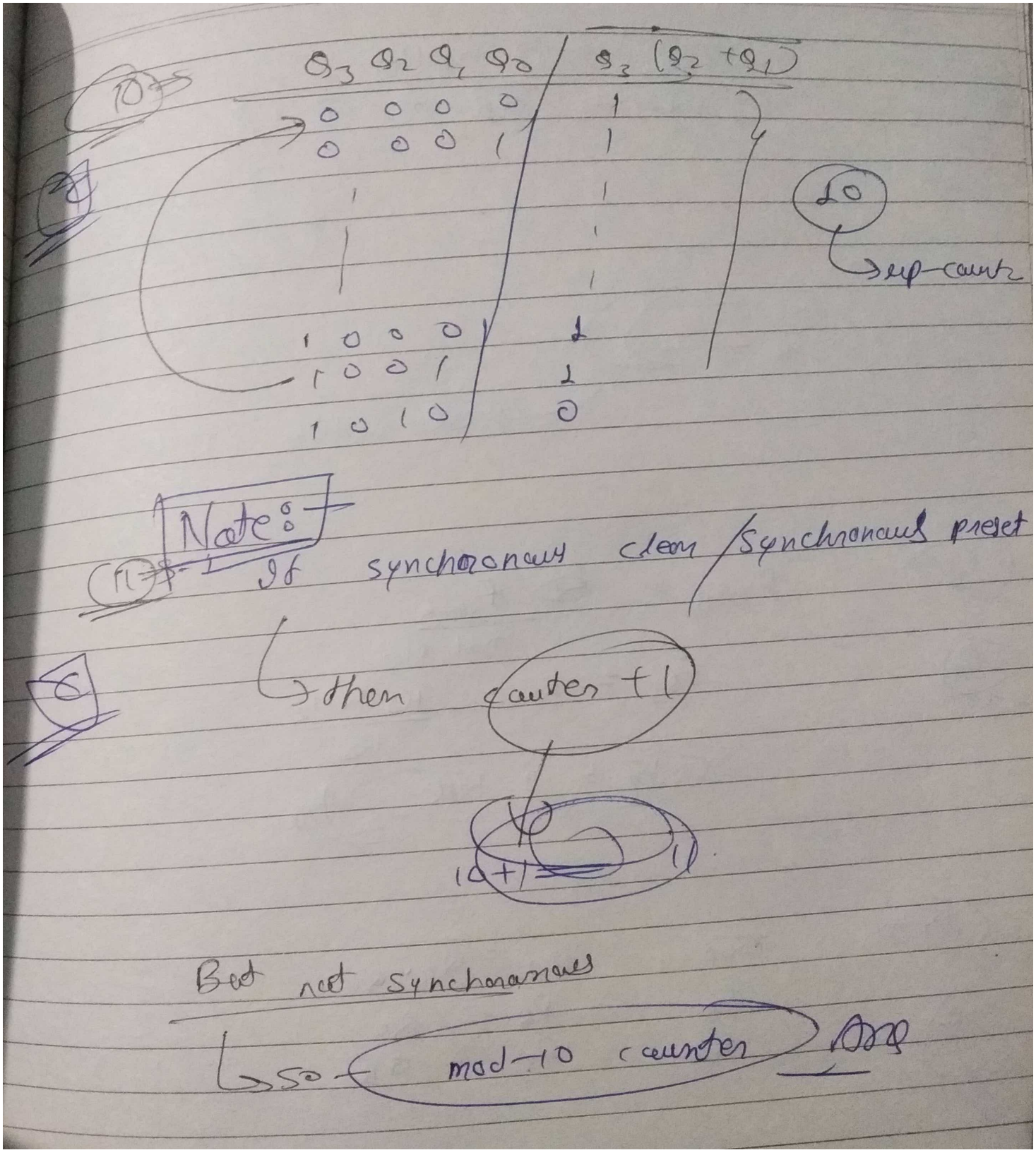
(5) → up-counter

(9)

Q_C	Q_B	Q_A	$\overline{Q_C}$ Q_B $\overline{Q_A}$
1	1	1	0
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	1

5

Mod-5 down-counter One


$Q_3\ Q_2\ Q_1\ Q_0$ / $S_3\ (Q_2 + Q_1)$
0 0 0 0 / 1
0 0 0 1 / 1
1 0 0 0 / 1
1 0 0 1 / 1
1 0 1 0 / 0
10
up-count
Note:-
If synchronous clear / Synchronous preset
then
counter + 1
10+1
1
But not synchronous
so
mod-10 counter

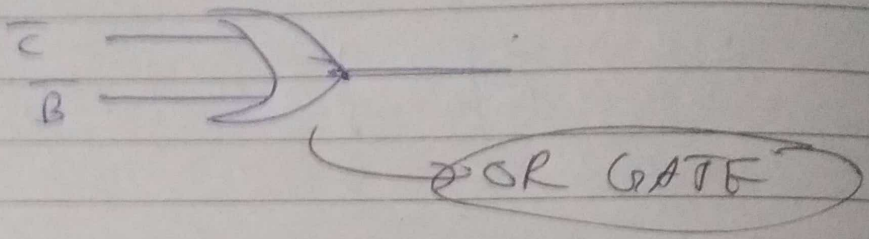
12

$\overline{CA}$ → NAND

$\overline{CA} \rightarrow \overline{C \cdot B} = \overline{C} + \overline{B}$

C

$\overline{C}$, $\overline{B}$ present



13

$f_{msB} = \dfrac{f_{clock}}{\text{mod NU}}$

B

$f_{Q_3} = f_y = \dfrac{10\ KHz}{10}$

$F_y = 1\ KHz$ Ans

14

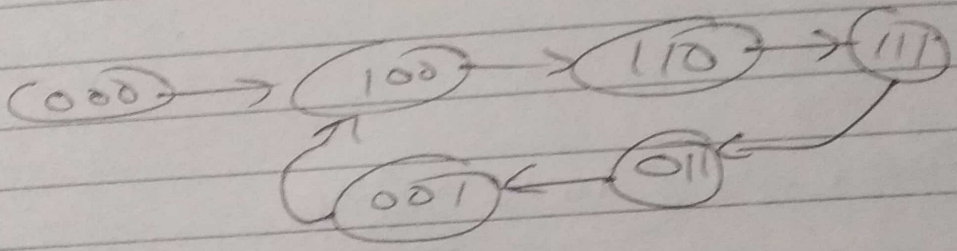
$Q_{A+1} = D_A = \overline{Q_B \cdot Q_C}$

$Q_{B+1} = D_B = Q_A$

B

$Q_{C+1} = D_C = Q_B$

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

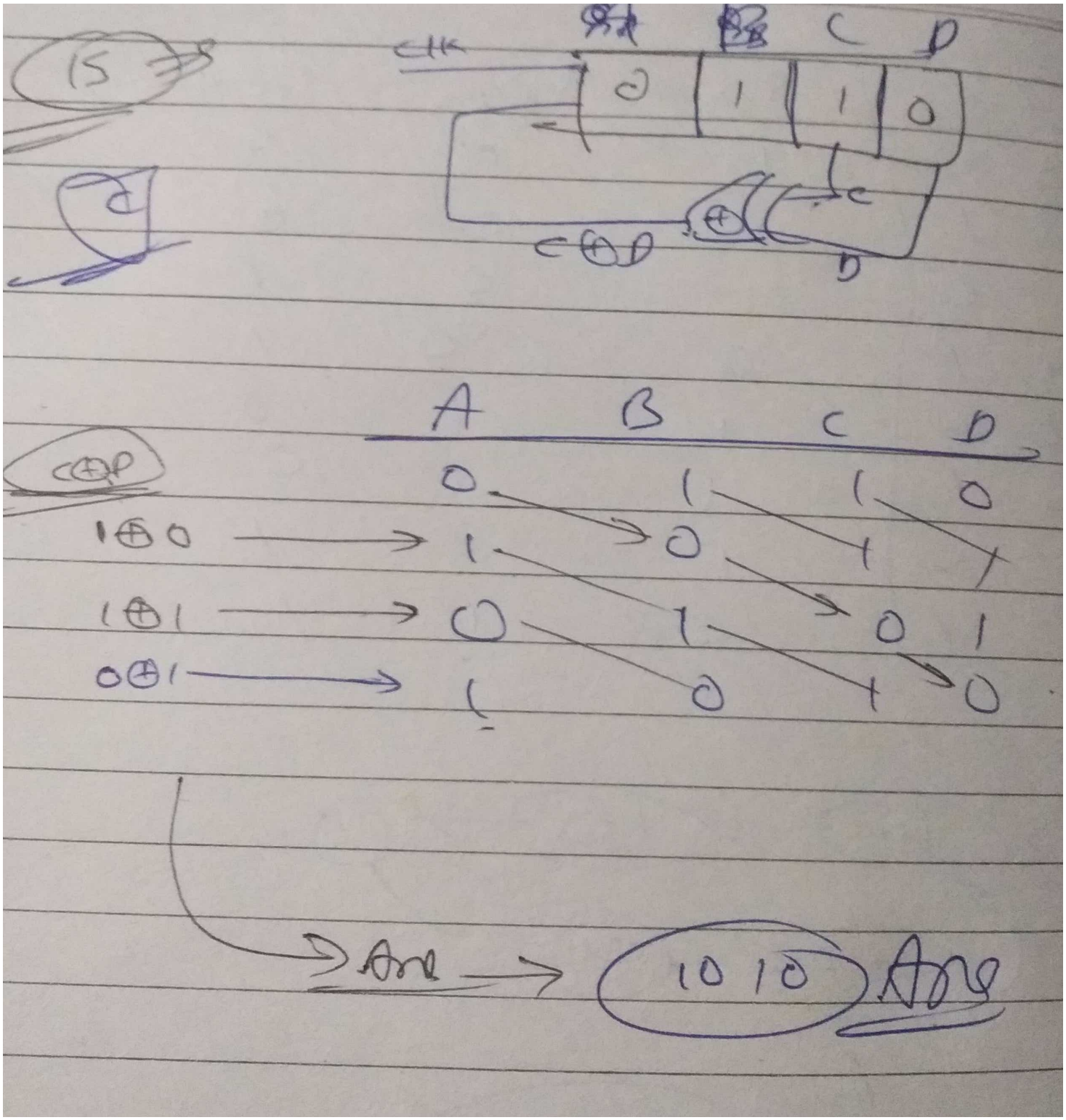


Mod-5

$$F_{mSB} = \frac{F_{clock}}{Mod\ No} = \frac{F_{clock}}{5}$$

It can be used dividing i/p frequency by 5

Ans


A B C D
0 1 1 0
1 0 0 1 1
1 1 0 0 1
0 1 1 0 0
Ans → 1010 Ans