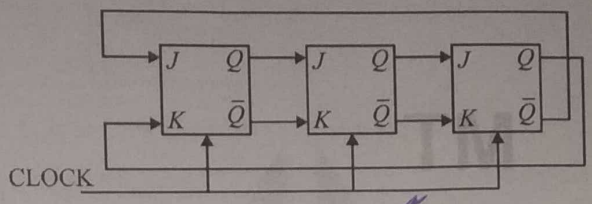
Q.98 For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:

[GATE : 1993]



(A) Shift Register (B) Mod-3 Counter (C) Mod-6 Counter (D) Mod-2 Counter

Q.99 Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

[GATE : 2015]

(A) 0, 1, 3, 7, 15, 14, 12, 8, 0 (B) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0

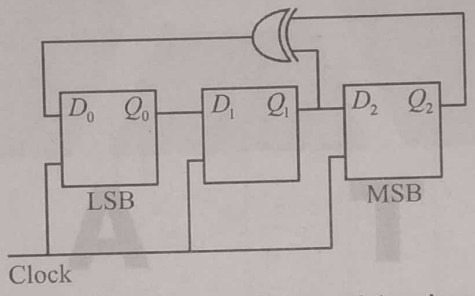
(C) 0, 2, 4, 6, 8, 10, 12, 14, 0 (D) 0, 8, 12, 14, 15, 7, 3, 1, 0

Q.100 The minimum number of J-K flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, ...) is _____. **[GATE : 2015]**

Q.101 We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is _____. **[GATE : 2016]**

Q.102 Consider the circuit given below with initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value of $4Q_2 + 2Q_1 + Q_0$.

[GATE : 2016]



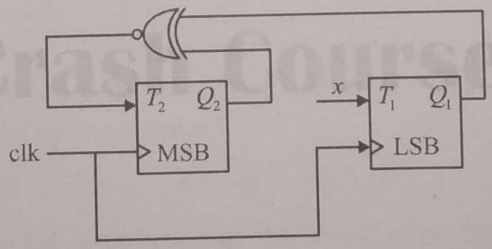
Which one of the following is the correct state sequence of the circuit?

(A) 1, 3, 4, 6, 7, 5, 2 (B) 1, 2, 5, 3, 7, 6, 4

(C) 1, 2, 7, 3, 5, 6, 4 (D) 1, 6, 5, 7, 2, 3, 4

Q.103 Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below.

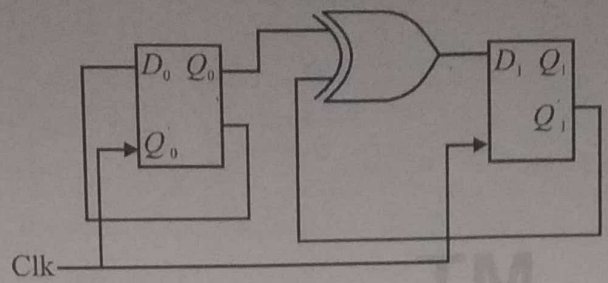
[GATE : 2004]



To complete the circuit, the input X should be

(A) Q_2' (B) $Q_2 + Q_1$ (C) $(Q_1 \oplus Q_2)'$ (D) $(Q_1 \oplus Q_2)$

Q.104 Consider the following circuit. **[GATE : 2005]**



Q_0	Q_1	D_0	D_1	Q_0^+	Q_1^+
0	0	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0
1	1	0	1	0	1

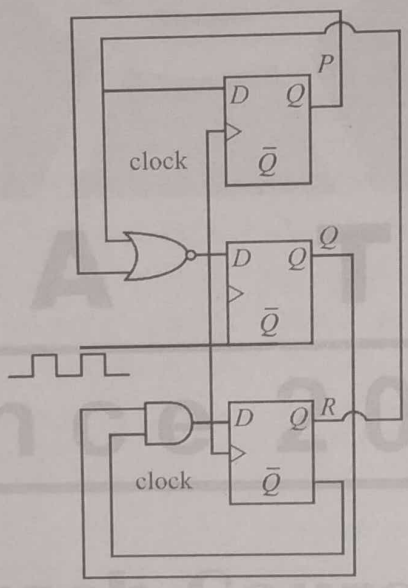
$Q_0^+ = Q_0 \oplus Q_1$

The flip-flops are positive edge triggered D FFs. Each state is designated as a two bit string Q_0Q_1. Let the initial state be 00. The state transition sequence is:

(A) $00 \rightarrow 11 \rightarrow 01$ (B) $00 \rightarrow 11$ (C) $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$ (D) $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

Common Data for Questions 105 to 106

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. **[GATE : 2011]**



Q.105 If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by *PQR* generated by the counter? **[GATE : 2011]**

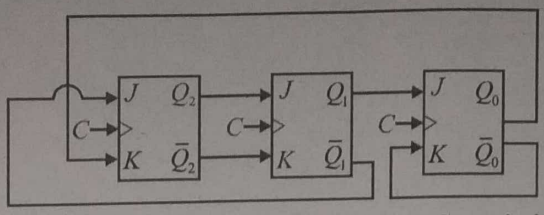
(A) 3 (B) 4 (C) 5 (D) 6

Q.106 If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of *PQR* after the clock edge? **[GATE : 2011]**

$\bar{P} = R$
$\bar{Q} = \bar{P} + R$
$\bar{R} = Q\bar{R}$

(A) 000 (B) 001 (C) 010 (D) 011

Q.107



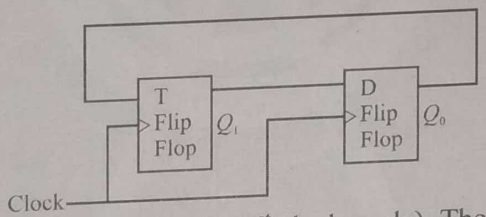
The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is _____. **[GATE : 2014]**

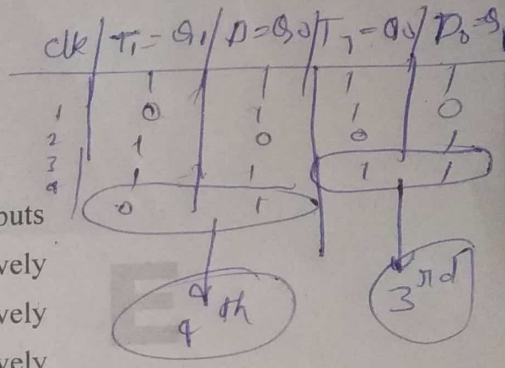
(A) 001, 010, 011 (B) 111, 110, 101 (C) 100, 110, 111 (D) 100, 011, 001

Q.108 A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip- flop, is connected to the input of the D flip-flop. Initially, the output of the D flip- flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays. **[GATE : 2015]**

(A) 0110110….. (B) 0100100…. (C) 011101110… (D) 011001100…

Q.109 Consider a combination of T and D flip-flops connected as shown below. The output of the D flip- flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop. **[GATE : 2017]**





Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

(A) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 00 respectively

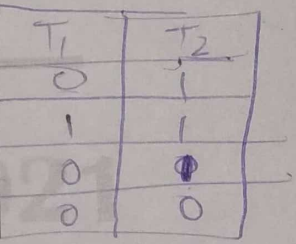
(B) $Q_1 Q_0$ after the 3rd cycle are 11 and after the 4th cycle are 01 respectively

(C) $Q_1 Q_0$ after the 3rd cycle are 00 and after the 4th cycle are 11 respectively

(D) $Q_1 Q_0$ after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

Q.110 The next state table of a 2-bit saturating up- counter is given below. **[GATE : 2017]**

Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1



The counter is built as a synchronous sequential circuit using T flip-flops. The expression for T_1 and T_0 are

(A) $T_1 = Q_1Q_0, T_0 = \overline{Q_1}\,\overline{Q_0}$

(B) $T_1 = \overline{Q_1}Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(C) $T_1 = Q_1 + Q_0, T_0 = \overline{Q_1} + \overline{Q_0}$

(D) $T_1 = \overline{Q_1}Q_0, T_0 = Q_1 + Q_0$

❖❖❖❖