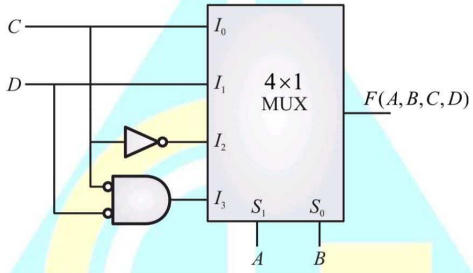
5. Combination Circuit

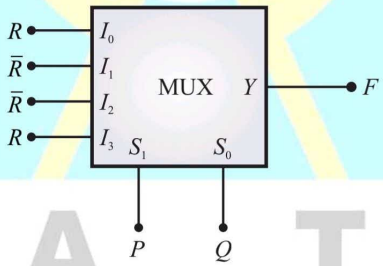
Q.1 The Boolean function realized by the logic circuit shown is **[GATE 2010, IIT Guwahati]**



(A) $F = \Sigma m(0,1,3,5,9,10,14)$ (B) $F = \Sigma m(2,3,5,7,8,12,13)$

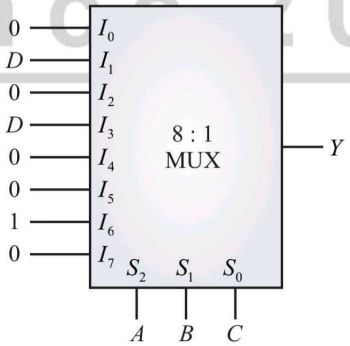
(C) $F = \Sigma m(1,2,4,5,11,14,15)$ (D) $F = \Sigma m(2,3,5,7,8,9,12)$

Q.2 The output F of the multiplexer circuit shown below expressed in terms of the input P, Q and R is **[GATE 2008, IISc Bangalore]**



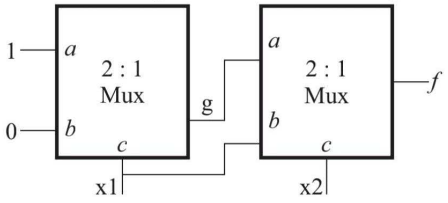
(A) $F = P \oplus Q \oplus R$ (B) $F = PQ + QR + RP$ (C) $F = (P \oplus Q)R$ (D) $F = (P \oplus Q)\overline{R}$

Q.3 An 8 to 1 multiplexer is used to implement a logical function Y as shown in the figure. The output Y is given by **[GATE 2014, IIT Kharagpur]**



(A) $Y = A\bar{B}C + A\bar{C}D$ (B) $Y = \bar{A}BC + A\bar{B}D$ (C) $Y = AB\bar{C} + \bar{A}CD$ (D) $Y = \bar{A}\bar{B}C + A\bar{B}C$

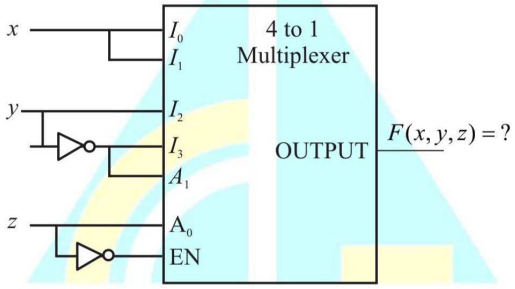
Q.4 Consider the circuit shown below. The output of a 2: 1 Mux is given by the function (ac' + bc).



Which of the following is true? **[GATE 2001, IIT Kanpur]**

(A) f = x1' + x2 (B) f = x1' x2 + x1x2' (C) f = x1 x2 + x1'x2' (D) f = x1 + x2'

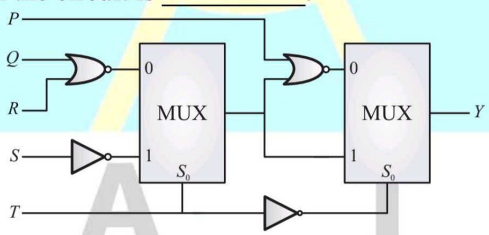
Q.5 Consider the following multiplexer where $I_0, I_1, I_2, I_3,$ are four data input lines selected by two address line combinations A_1 $A_0 = 00, 01, 10, 11$ respectively and f is the output of the multiplex (or). EN is the Enable input. **[GATE 2002, IISc Bangalore]**



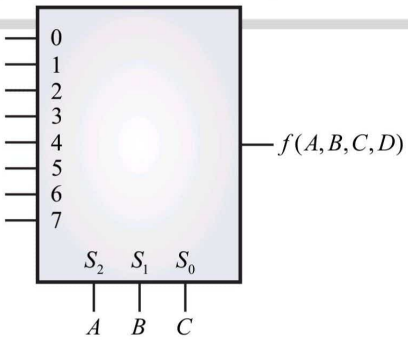
The function f (x,y,z) implemented by the above circuit is

(A) $xy\bar{z}$ (B) $xy + z$ (C) $x + y$ (D) None of the above

Q.6 For the circuit shown in the figure, the delays of NOR gates, multiplexers and inverters are 2 ns, 1.5 ns and 1 ns, respectively. If all the inputs *P, Q, R, S* and *T* are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____. **[GATE 2016, IISc Bangalore]**



Q.7 A Boolean function $f(A, B, C, D) = \Pi M\ (1, 5, 12, 15)$ is to be implemented using an 8 × 1 multiplexer (*A* is MSB). The inputs *ABC* are connected to the select input $S_2\ S_1\ S_0$ of the multiplexer respectively. Which one of the following options gives the correct inputs to pins 0, 1, 2, 3, 4, 5, 6, 7 in order? **[GATE 2015, IIT Kanpur]**



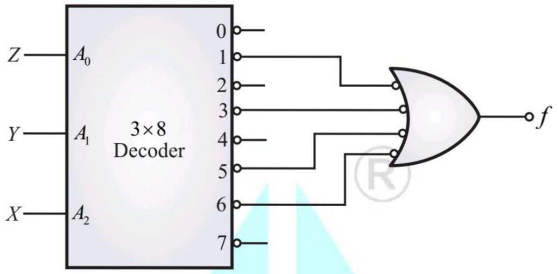
(A) $D, 0, D, 0, 0, 0, \bar{D}, D$

(B) $\bar{D}, 1, \bar{D}, 1, 1, 1, D, \bar{D}$

(C) $D, 1, D, 1, 1, 1, \bar{D}, D$

(D) $\bar{D}, 0, \bar{D}, 0, 0, 0, D, \bar{D}$

Q.8 A 3 line to 8 line decoder, with active low outputs, is used to implement a 3 variable Boolean functions as shown in the figure.



The simplified form of Boolean function $F(X,Y,Z)$ implemented in 'Product of Sum' form will be

[GATE 2008, IISc Bangalore]

(A) $(X+Z).(\bar{X}+\bar{Y}+\bar{Z}).(Y+Z)$

(B) $(\bar{X}+\bar{Z}).(X+Y+Z).(\bar{Y}+\bar{Z})$

(C) $(\bar{X}+\bar{Y}+Z).(\bar{X}+Y+Z).\ (X+\bar{Y}+Z).(X+Y+\bar{Z})$

(D) $(\bar{X}+\bar{Y}+Z).(\bar{X}+Y+\bar{Z}).\ (X+\bar{Y}+Z).(X+\bar{Y}+\bar{Z})$

Q.9 In a half-subtractor circuit with X and Y as inputs, the Borrow (M) and Difference $(N = X - Y)$ are given by

[GATE 2014, IIT Kharagpur]

(A) $M = X \oplus Y,\ N = XY$

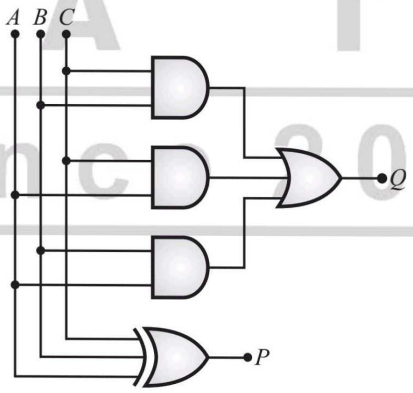
(B) $M = X\,Y,\ N = X \oplus Y$

(C) $M = \bar{X}\,Y,\ N = X \oplus Y$

(D) $M = X\,\bar{Y},\ N = \overline{X \oplus Y}$

Q.10 In the given circuit of figure, A, B and C are the inputs and P, Q are the two outputs. The circuit is a

[GATE 2004, IIT Delhi]



(A) Half adder where P is the sum and Q is the carry.

(B) Half adder where P is the carry and Q is the sum.

(C) Full adder where P is the sum and Q is the carry.

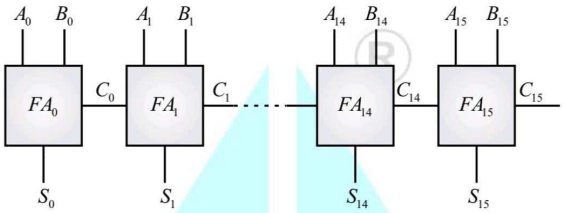
(D) Full adder where P is the carry and Q is the sum.

Q.11 A 1 bit full adder takes 20 ns to generator carry-out bit and 40 ns for the sum bit. What is the maximum rate of addition per second when four 1-bit full adders are cascaded ?

(A) 10^7 (B) 1.25×10^7 (C) 6.25×10^6 (D) 10^5

Q.12 A 16 bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation delay of each FA is 12 ns and the sum-propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be_____.

[GATE 2016, IISc Bangalore]

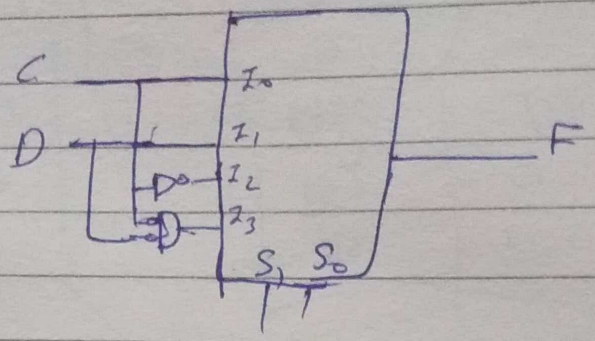


Q.13 A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple- carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

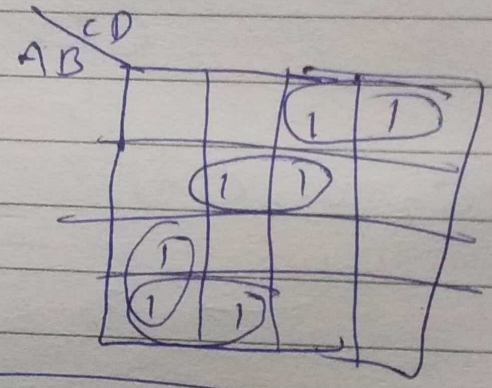
[GATE 2015, IIT Kanpur]

Combination Circuit

1 →



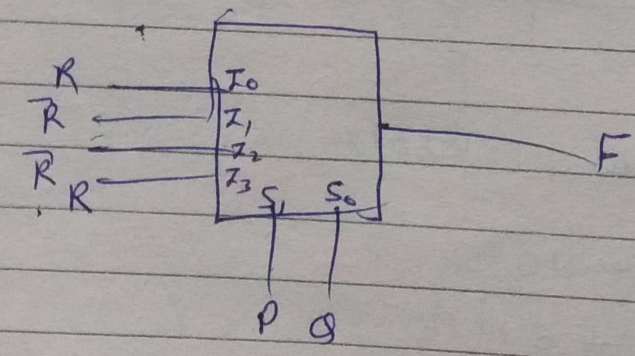
P

F = 

$F = \Sigma m(2, 3, 5, 7, 8, 9, 12)$ Ans

2 →

A

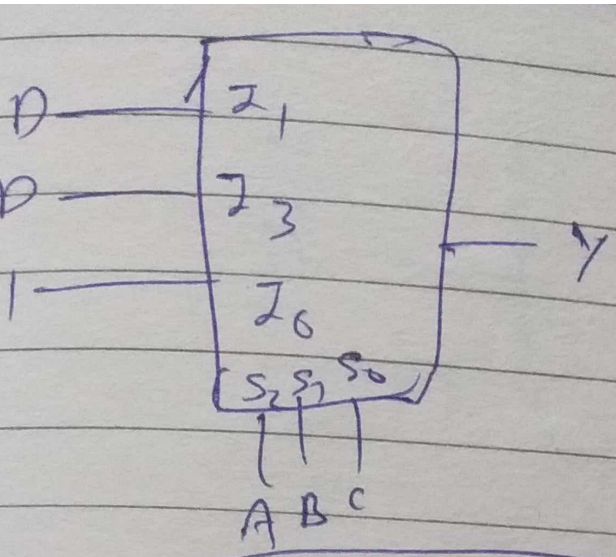


$$F = \bar{Q}\bar{P}R + \bar{Q}P\bar{R} + Q\bar{P}\bar{R} + QPR$$

$$= \bar{Q}(P \oplus R) + Q\overline{(P \oplus R)}$$

$$F = P \oplus Q \oplus R$$ Ans

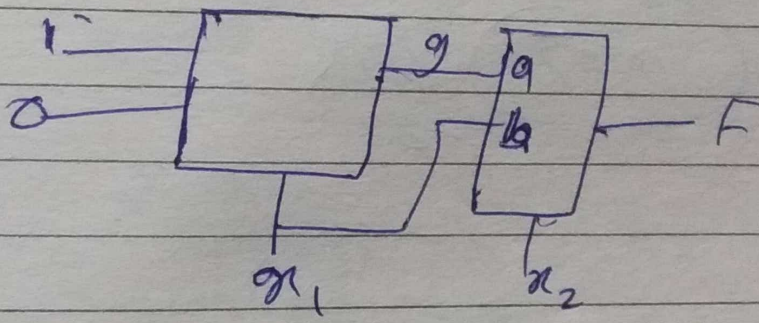
(3) ⇒



C

$$Y = AB\bar{C} + \bar{A}BD$$ Ans

(4) ⇒



C

$$g = a\bar{c} + bc = 1\cdot\bar{x} + 0 = \bar{x}$$

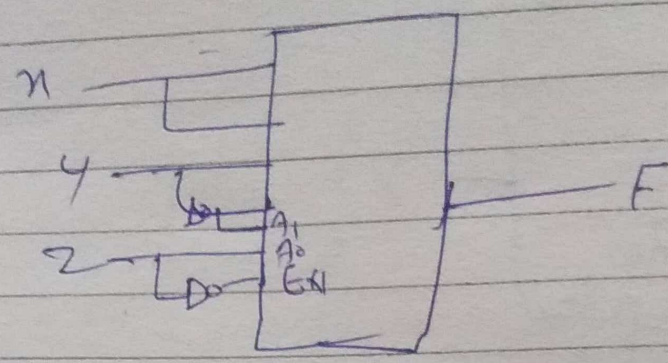
$$f = a\bar{c} + bc$$

$$f = g\cdot\bar{x_2} + x_1x_2$$

$$f = \bar{x_1}\cdot\bar{x_2} + x_1x_2$$ Ans

(5)

(A)

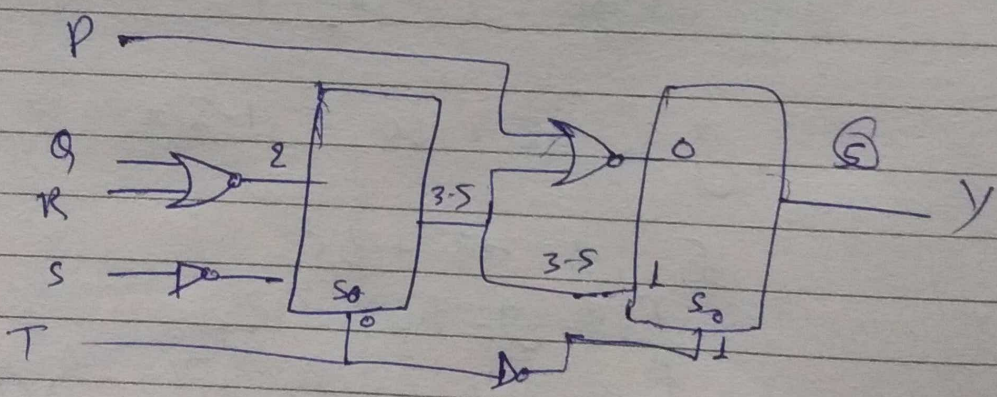


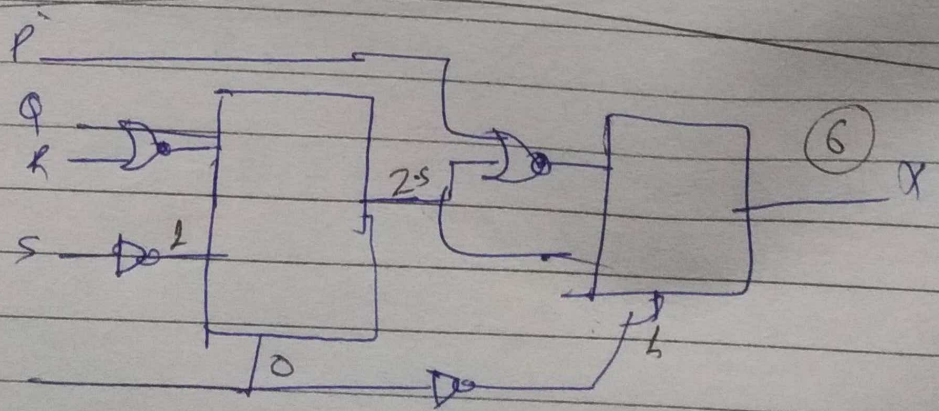
$$Y = EN(\bar{A}_1\bar{A}_0 I_0 + \bar{A}_1 A_0 I_1 + A_1\bar{A}_0 I_2 + A_1 A_0 I_3)$$

$$= y\bar{z}\,x\bar{z} + yz\bar{z} + \bar{y}z\,y\bar{z} + \bar{y}z\bar{y}\bar{z}$$

$$= (xy\bar{z}) \quad \text{Ans}$$

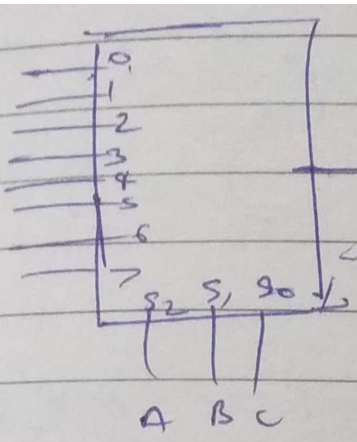
(6)





max(5,6) = (6) Ans

7 → B



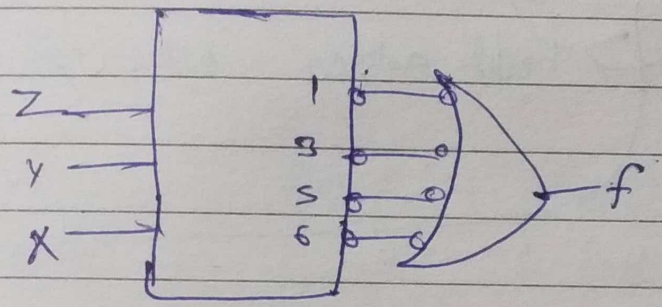
$\bar{D} = (0,2,4,6,8,10,12,14)$

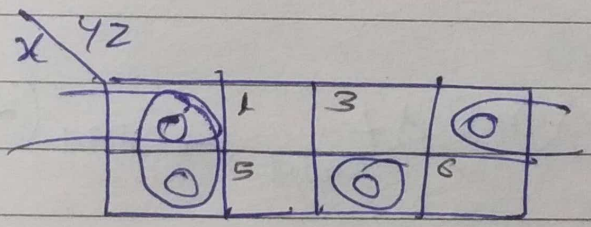
$D = (3,5,7,9,11,13,15)$

$\bar{D}\ \bar{I}\ \bar{D}\ III\ D\ \bar{D}$

Ans

8 → A





$(x+z)(\bar{x}+\bar{y}+z)(y+z)$

Ans

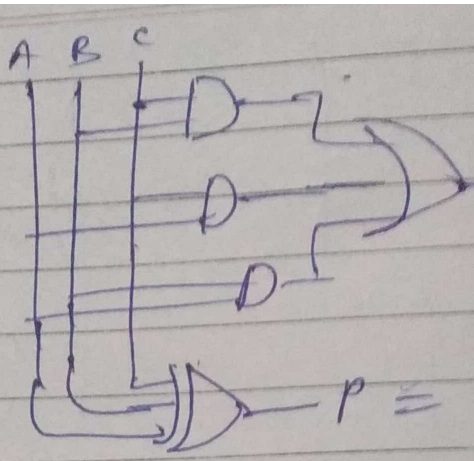
9 → C

Borrow (M) $= \bar{x}y$

Difference (N) $= x \oplus y$

Ans

(10) ⇒



⇒ Full adder where P → Sum
Q → Carry

Ans

(11) ⇒

$$T = (n-1)\Delta t_{carry} + \max(\Delta t_{sum}, \Delta t_{carry})$$

$$= 3 \times 20 + 40$$

$$= 100\,ns$$

1 Add ⟶ 100 ns

1 Sec ⟶ $\frac{1}{100 \times 10^{-9}}$ = 10^7 Ans

12⇒ $T = (n-1)\Delta t_{cout} + \max(\Delta t_{sum}, \Delta t_{cout})$

$= 15 \times 12 + \max(15, 12)$

$= 180 + 15$

$= 195$ ns Ans

13⇒ HA = XOR + AND

FA = 2 HA + 1 OR

Delay (XOR) = 2 × Delay (OR/AND)

$= 2 \times 1.2$

$= 2.4$ μs

$T = 3 \times \Delta t_{cout} + \max(\Delta t_{sum}, \Delta t_{cout})$

$= 3 \times 4.8 + \max(4.8, 4.8)$

$T = 19.2$ μs Ans