KLE Technological University

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School

of

Electronics and Communication Engineering

Course Project Report

on

1Kbyte Dual Port SRAM

By:

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0.1 Problem statement

Design and implementation of 1Kbyte Dual Port SRAM

0.2 Introduction

SRAM (Static Random Access Memory) is a type of semiconductor memory that stores data in a static form, which means that it retains the stored data as long as the power supply is maintained. It is widely used in various electronic devices, including microprocessors, digital signal processors, and other digital systems.

SRAM is designed to provide faster access to data than other types of memory, such as DRAM (Dynamic Random Access Memory). Unlike DRAM, which requires constant refreshing to maintain data integrity, SRAM can hold data for an extended period without the need for refreshing. This makes it ideal for use in applications that require fast access to data and low power consumption.

SRAM is typically used in cache memory, where it is used to store frequently accessed data for faster retrieval. It is also used in embedded systems, where it is used for data storage and temporary data buffering.

SRAM is available in different configurations, including single-port, dual-port, and quad-port. Single-port SRAM has a single access point for data, while dual-port SRAM has two independent access ports for simultaneous reading and writing of data. Quad-port SRAM has four access ports, allowing multiple users to access the memory simultaneously.

In summary, SRAM is a fast and reliable form of semiconductor memory that provides efficient data storage and retrieval for various electronic devices. Its static design and low power consumption make it an ideal choice for use in embedded systems and other applications that require fast and efficient access to data.

Chapter 1

Architecture

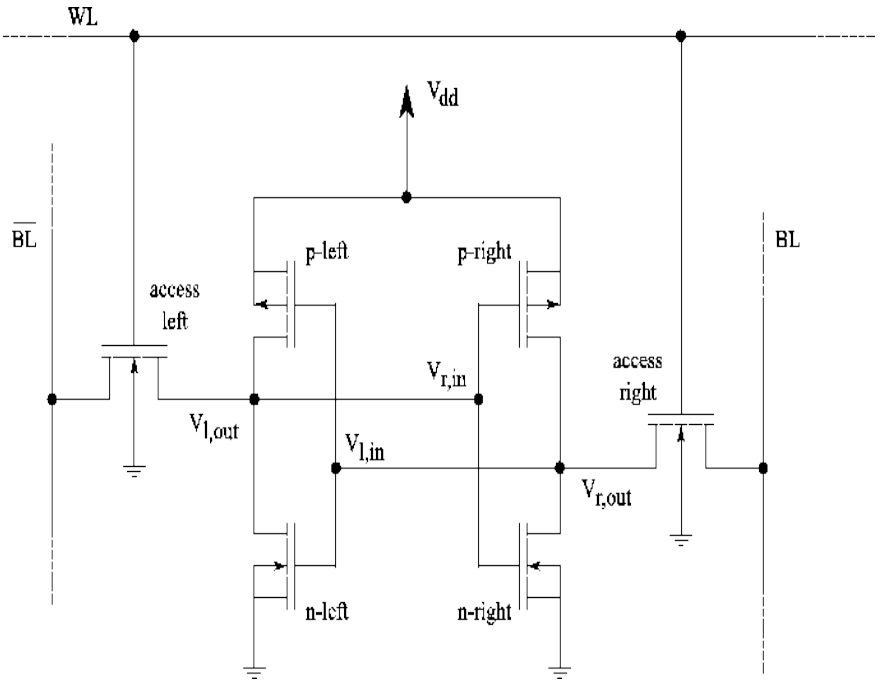

Figure 1.1: Architecture of SRAM

SRAM is a type of volatile memory that is commonly used in computer systems, cache memories, and other applications where fast and efficient data access is required.

The 6T SRAM cell is one of the most widely used SRAM cell designs due to its simplicity and reliability.

It consists of six transistors (hence the name 6T), which are arranged in a cross-coupled configuration to store a single bit of data.

The six transistors in the cell are typically implemented using complementary metal-oxide-semiconductor (CMOS) technology.

The basic operation of a 6T SRAM cell involves two stable states, known as the ”0” state and the ”1” state.

These states are determined by the voltage levels applied to the transistors within the cell.

To read the data stored in the cell, a bit-line is connected to the cross-coupled transistors, and the voltage on the bit-line is sensed.

To write data into the cell, the word-line is activated, and the desired voltage levels are applied to the bit-line.

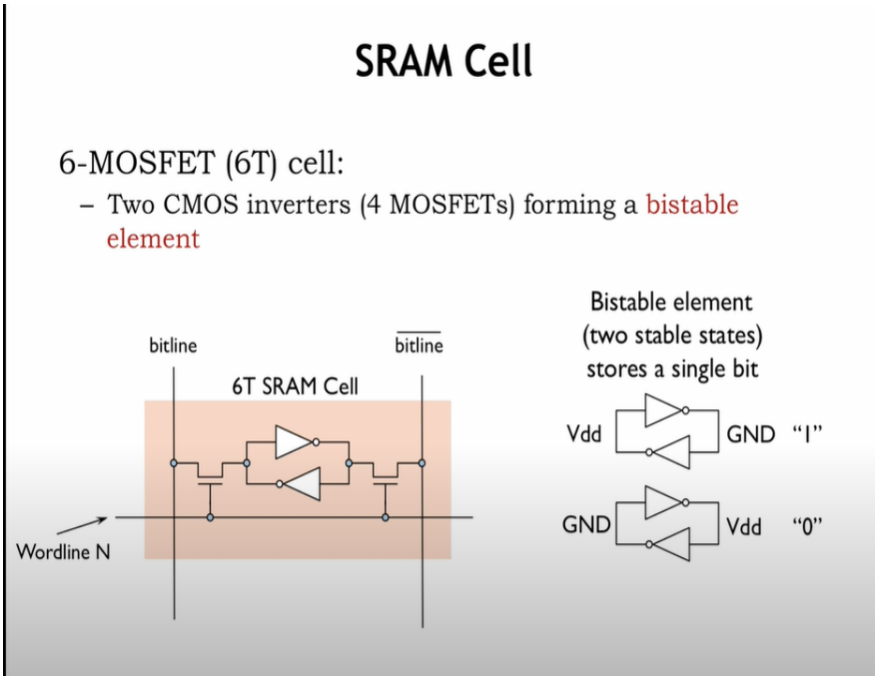

Figure 1.2: SRAM CELL

Here’s a step-by-step explanation of the operation of a 6T SRAM cell:

Hold operation:

During the hold operation, the data stored in the SRAM cell is retained even when there is no active read or write operation taking place.

The hold operation is achieved by maintaining a stable voltage on the cell’s bitlines and wordlines, which keeps the transistors in the cell in a non-conductive state.

To initiate the hold operation, the wordlines are deactivated, and the bitlines are precharged to a stable voltage level.

This ensures that the voltage level on the bitlines is higher than the threshold voltage of

the access transistors in the SRAM cell, which prevents the cell from being inadvertently overwritten.

Read operation:

The read operation of the 6T SRAM cell is initiated by activating the wordline that connects to the SRAM cell.
When the wordline is activated, it creates a path of low resistance between the cell's two access transistors, which allows the stored data to be read.
The word line is activated, enabling the access transistors.
The bit lines (BL and BL) are precharged to a voltage level.
The voltage on the bit line connected to the desired cell is sensed.
If the voltage on the bit line is high, it represents a logic "1" stored in the cell. If the voltage is low, it represents a logic "0."

Write operation:

The write operation of the 6T SRAM cell is initiated by activating the wordline that connects to the SRAM cell and setting the appropriate voltage levels on the bitlines to represent the new data to be stored.

The word line is activated, enabling the access transistors.

The desired data value is applied to the bit lines.

The voltage on the bit lines overpowers the cross-coupled inverters, forcing them into the desired state (0 or 1).

After the write operation, the word line is deactivated to prevent further changes to the cell.

1.1 Advantages and Dis advantages of SRAM

Advantages:

High speed: The 6T SRAM cell offers fast access times, making it suitable for applications that require quick data retrieval and processing.

Low power consumption: Compared to dynamic random-access memory (DRAM), SRAM cells, including the 6T SRAM, consume less power because they do not require periodic refreshing. This makes them more energy-efficient.

Non-volatile: SRAM cells retain their data as long as power is supplied, unlike dynamic random-access memory (DRAM) cells that require constant refreshing. This characteristic makes SRAM cells, including the 6T SRAM, suitable for applications where data persistence is critical.

Noise immunity: The 6T SRAM cell is less susceptible to noise interference, which improves data reliability and integrity.

Disadvantages:

Larger area requirement: The 6T SRAM cell requires a larger physical footprint compared to other SRAM cell designs, such as the 4T SRAM cell. This larger area requirement can limit the overall memory density that can be achieved on a chip.

Increased power consumption during standby: While the 6T SRAM offers low power consumption during active operation, it still consumes power when in standby mode. This standby power consumption can be a concern for battery-operated devices that strive for maximum energy efficiency.

Complexity: The 6T SRAM cell is more complex compared to other memory cell designs, such as the 1T SRAM or 4T SRAM cells. This complexity can lead to increased manufacturing costs and potential yield issues.

Chapter 2

Results

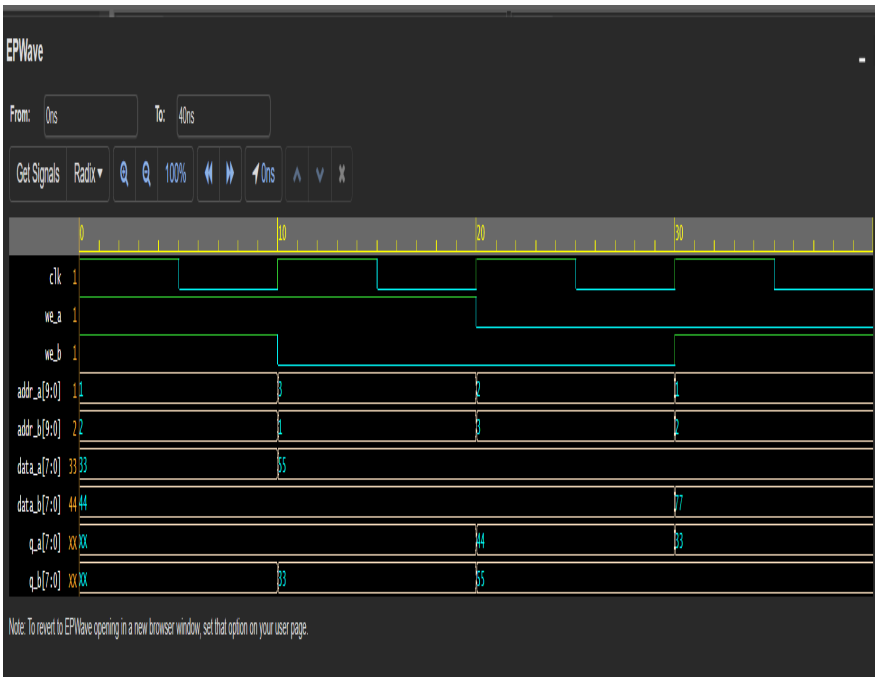

Figure 2.1: Waveform of SRAM

Chapter 3

Conclusions

In conclusion, the development of a 1kbyte dual port SRAM project is a significant achievement in the field of digital electronics. The project aimed to design and implement a dual-port memory module that can read and write data simultaneously from two independent sources.

The project involved various stages, including conceptualization, design, simulation, testing, and implementation. The final product was a functional dual-port SRAM module that met the project's design specifications.

The development of this project has several potential applications, including use in high-speed data processing systems, digital signal processing, and telecommunications. The dual-port design offers a significant advantage over traditional single-port memory modules, allowing for increased flexibility and data throughput.