Slok Shah

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Education & Training

Master's in Electrical & Computer Engineering, DREXEL UNIVERSITY | PA-US | June 2017
Bachelors of Engineering, Electronics Engineering, MUMBAI UNIVERSITY| INDIA

Area of Skills

- Synopsys Primetime
- Cadence Virtuoso
- DRC, LVS and PEX
- HTML, CSS and JavaScript
- OpenMP and pthread
- Static Timing Analysis
- C, C++ and Python
- Perl and Bash Scripting
- System Verilog Basics
- DC and IC Compiler
- Verilog and VHDL
- MATLAB and LabView

Project Experience

ASIC Verification Trainee, Verifast Technologies, San Jose, CA 7/2017– Present

- Designed a filer based self-checking verification environment with driver, monitor and checker modules.
- Verified for UART protocols. Developed a PERL script to launch regression tests and analyze the results using system verilog.

OpenSparc T1-DC Synthesis and Design Planning using Synopsys Primetime 1/2017 – 3/2017

- Performed DC Synthesis on OpenSparc T1 FPU using design compiler and IC compiler tools for 90nm.
- Successfully conducted Static timing analysis using primetime. Running the processor on as low as 2ns period and a relatively low power consumption.
- Implemented the back-end of IC design flow range, including logic synthesis, floor planning, placement, clock tree synthesis, routing and verification. Performed power and timing optimization.
- Synthesized OpenSparc T1 FPU using cadence encounter. Performed Parasitic extraction using PEX.
- The goal was to get familiar with Synopsys tools in transforming a gate-level netlist into a routed layout.

IC Design Project: 8-bit Pico Processor using Cadence 1/2016 – 3/2016

- Designed and implemented 8-bit Pico Processor based on MIPS/RISC architecture. Used 9500 transistors.
- Performed schematic and layout design using cadence virtuoso and successfully completed LVS and DRC checks.
- Implemented the Program counter, register bank, and ALU in Verilog RTL.

Modeling a Two-Level Power Distribution Network 3/2016 – 6/2016

- The primary objective of this project was to design two level power distribution networks consisting of a Global PDN and six Local PDNs. The local PDNs were designed with a specific power budget.

Parallelization of mathematical algorithm using C 9/2015 – 12/2015

- Simulated benchmarks and evaluated the performance impact on a processor by varying cache sizes using gem 5
- Observed speedup in parallel versions over serial versions in multi core systems by performing parallel threaded matrix-matrix multiplication using Pthreads, OpenMP and CUDA. Achieved maximum speedups.

Cache Simulator using programming language C++ 3/2016 – 6/2016

- Developed a multilevel basic cache simulator, that returns read-write hit and miss rate of the cache.
- The purpose of the project was to understand the use of multithreading to run processes faster.
- Perlbench and bzip benchmarks where used for the analysis.

Teaching Assistant, Drexel University, Philadelphia, PA 9/2016 – 6/2017

- Assisted laboratory for undergraduate courses like ENGR 201- Evaluation and Presentation of experimental data I & II. Explained effectively, the basics of MS Excel, MATLAB, LabVIEW.

Project Assistant, Research & Design Lab(RIIDL), Mumbai 7/2012 – 4/2013

- Facilitated in projects and helped to commercialize the project. Interactive staircase and Eco-mappers. Configured control systems and sensors to collect data about dust, pollution and noise levels around the city.

Relevant Coursework 9/2015 – 6/2017

- Dependable Computing, Web Security, Advance Programming, ASIC Design, High Performance & Parallel Computer Architecture, Microwave Active Subsystems, Custom VLSI Design, Computing in the small.