

Assignment No. 7

Ques - I

Why is data transfer needed ? What are different Data Transfer Schemes ?

Ans -

We can connect several I/O devices and memory peripherals to a microprocessor. However, since different technologies are involved, there will be differences in the speed of operation and of data transfer.

A wide variety of I/O devices are available which can be connected to a microprocessor to form a micro computer system. These I/O devices are manufactured by using different manufacturing techniques like electrical, electronics, electro mechanical, mechanical, optical, optoelectronics etc.

* Data Transfer Schemes :-

It is classified into the two categories :

1. Programmed Data Transfer Scheme (Microprocessor controlled data transfer)
 - a) Synchronous data transfer scheme
 - b) Asynchronous data transfer scheme
 - c) Interrupt driven data transfer scheme
2. DMA (Direct Memory Access) scheme of data transfer
 - a) Burst mode of DMA data transfer

b) Cycle Steal technique of DMA data transfer

Que-2 Differentiate between Parallel Data Transfer and Serial Data Transfer Schemes.

Aus -

Parallel Data Transfer

- In Parallel Data Transfer, data flows in multiple lines.
- Parallel Transfer transmission is not cost-efficient.
- In Parallel Transmission, eight bits transferred at one clock pulse.
- Parallel Transmission is fast in comparison of serial transmission.
- Generally, Parallel Transmission is used for short distance.
- The circuit used in parallel Transmission is relatively complex.

Serial Data Transfer

- In Serial Data Transfer, data (bit) flows in bi-direction.
- Serial Transmission is cost-efficient.
- In serial transmission, one bit transferred at one clock pulse.
- Serial transfer transmission is slow in comparison of Parallel Transmission.
- Generally, Serial Transmission is used for long-distance.
- The circuit used in Serial Transmission is simple.

Ques-3

Explain Parallel Data Transfer Techniques in detail.

Aus -

Parallel Data Transfer Techniques are :-

- i) Programmed I/O Data Transfer
- ii) Interrupt Driven I/O Data Transfer
- iii) Device or Direct memory Access (DMA) Data Transfer

(i) Programmed I/O Data Transfer -

In a programmed data transfer scheme, also called the processor controlled data transfer scheme, the data are transferred under the control of the CPU. In this data transfer scheme, data transfer from microprocessor or memory or I/O devices can take place under the control of stored program which are stored in the memory.

The programmed data transfer scheme can be further classified into the following two categories :-

- a) Synchronous data transfer scheme
- b) Asynchronous data transfer scheme

(ii) Interrupt Driven I/O Data Transfer -

The 8085 microprocessor (and all other microprocessor) has a facility that while executing the main program, the microprocessor can be interrupted to do some specific task and after completing

this specific task it can go on executing the main program.

(iii) Device or Direct Memory Access (DMA) data Transfer -

DMA scheme of Data Transfer is a technique, in which the data transfer takes place directly between the I/O devices and the memory. During DMA transfer, the CPU has no control over the buses. Data transfer is controlled by I/O devices or a DMA controller.

The DMA scheme of data transfer is of the following two types -

- Burst mode of DMA data transfer
- Cycle steal technique of DMA data transfer

Ques-4 Explain Interrupt Driven I/O Data transfer techniques schemes.

Aus-

The different Interrupt Driven I/O data transfer schemes are -

- Seri...

Several I/O devices are connected to a single interrupt level.

- One I/O device is connected to each interrupt level

- More than one I/O device is connected to each interrupt level

- a) Several I/O devices are connected to a single interrupt level -

In this situation, a microprocessor may have only one interrupt level and several I/O devices can be connected to this single interrupt level. The several I/O devices are connected to single interrupt level through a logical OR circuit.

When any I/O device interrupts the microprocessor for transfer of data, the microprocessor has to identify which device has interrupted.

- b) One I/O device is connected to each interrupt level.

In this situation, a microprocessor has several interrupt levels and one I/O device can be connected to each interrupt level.

In this situation, when a device interrupts the microprocessor, the microprocessor immediately knows which of the I/O devices has interrupted.

- c) More than one I/O device is connected to each interrupt level.

In this situation, a microprocessor has several interrupt levels and more than one I/O devices may be connected to each interrupt level. In this interrupt driven data transfer scheme, the microprocessor employs both vectored interrupt scheme and

and device pulling scheme to identify which of the I/O device has interrupted the microprocessor for transfer of data.

Ques 5 Explain in detail Direct Memory Access (DMA) data transfer schemes in detail.

Ans -

The DMA scheme of data transfer is of the following two types -

(i) Burst mode of DMA data transfer -

This is the fastest mode of DMA data transfer. In this technique, a block of data is transferred continuously. The I/O device withdraws the DMA request only when all the data bytes are transferred. This technique is used by magnetic disc drives.

(ii) Cycle Steal Technique of DMA Data Transfer -

In this technique, a long block of data is transferred by a sequence of DMA cycles. Only one byte of data is transferred at a time. After transferring one byte, the DMA controller disables the HOLD signal and reactivates this signal only when the next byte actually needs to be transferred. Here the DMA controller gives control of the buses back to the microprocessor in between successive byte transfers.

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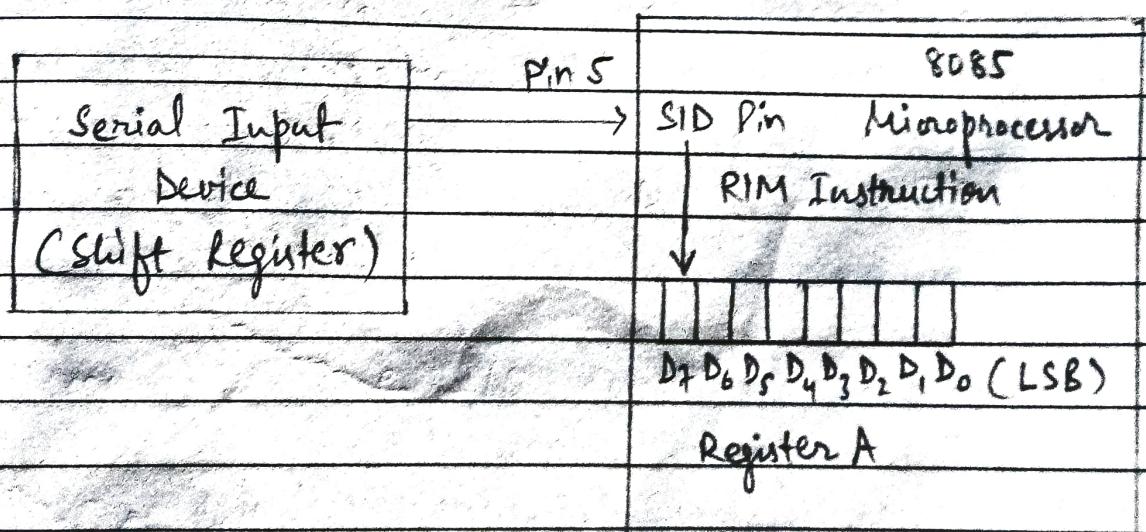
Aus-6 Explain Serial Data Transfer Techniques in detail.

Aus- The instructions used for serial communication are RIM and SIM.

Serial Data Input :

8085 microprocessor reads serial input data bit via the SID pin (serial input data) - pin 5 using RIM (Read Interrupt Mask) instruction.

Serial input device is connected to pin 5 (SID pin) of the microprocessor. Whenever, RIM instruction is executed, pin 5 input status is stored at bit D₇ of the accumulator. Thus after RIM instruction, bit D₇ is the serial input bit.



Serial Data Output :

8085 microprocessor output serial data output bit via its SOD pin (Serial output Data - pin 4) using SIM (Set

Interrupt Mask) instruction.

