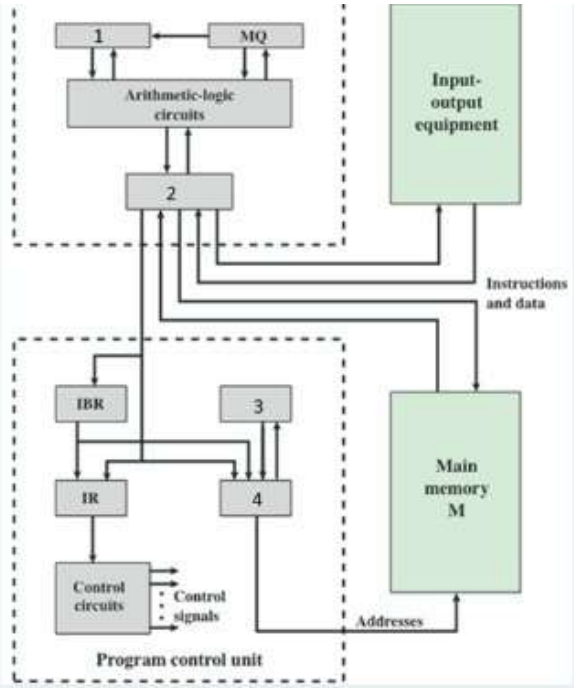

Considering the following IAS computer structure, write the name of the terms in the numbered locations in order.
For example:

1- XXX
2-YYY
3-ZZZ
4-MMM
(-/8 Puan)

Accumulator
Memory Buffer Register
Program Counter
Memory Address Register

How is synchronization achieved in asynchronous data transfer over a data bus?
(-/2 Puan)

ack signals

10

What is QPI?
(-/2 Puan)

Quick Path Interconnect. Its goal is to get a higher speed.

11

Is it possible to use PCI Express x4 card on a PCI Express x16 Slot? Explain your answer.
(-/2 Puan)

Yes, there may be space on the card, but it only works because it will use 4 sections.

12

Explain the main difference between the North Bridge South and South bridgeç
(-/3 Puan)

The northbridge is a chip within the chipset of a motherboard that straightforwardly connects to the CPU whereas the southbridge is a chip within the chipset of a motherboard that does not straightforwardly interfaces to the CPU

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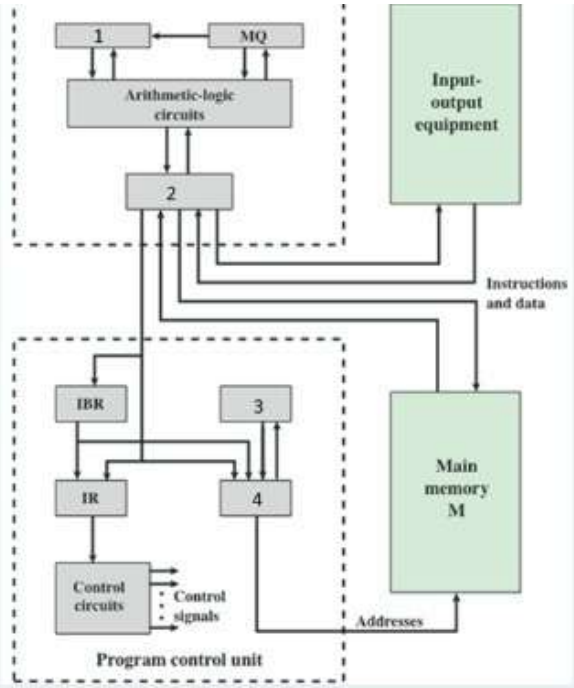

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What are the four main structural components of o computer?
(-/4 Puan)

Main Memory, CPU, Input Units, Output Units

7

Which of the following memory types are example for a shared memory?
(2/2 Puan)

- [x] Dynamic memory (RAM) ✓
- [ ] L1 Cache
- [ ] L2 Cache
- [x] L3 Cache ✓

8

If 40% of an application is performed serially, what is the speedup if there are 6 processors used? Write the formula and solution. (Anonim olmayan soru ⓘ)
(-/4 Puan)

8_OKAN ORKUN.jpeg

2

What is the main difference between X64 and IA-64?
(-/3 Puan)

The IA-64 can be a 64-bit Itanium engineering that is elite to Intel, while the x64 is a 64-bit expansion to the x86 design that is not selected.

3

Consider a memory system that uses a 16-bit address to address at the byte level, plus a cache that uses a 32-byte line size. Assume a direct mapped cache with a tag field in the address of 7 bits. Show the address format and determine the following parameters:
a) Number of addressable units:
b) Number of blocks in main memory
c) Number of lines in cache
d) Total cache memory capacity in bytes
e) Size of the tag

Not: You have to show your calculations, otherwise you can not get any point from this question. (Anonim olmayan soru ⓘ)
(-/15 Puan)

3_OKAN ORKUN.jpeg

5

Write an IAS program to compute f(n)=2^n using instructions from the Table 1 where the input value of n is stored at the memory location 0FA. After the execution of your program the output value f(n) must be stored at location 0FB. For example, if the content of 0FA is 4 then a value of 16 (2^4) must be present in memory location 0FB. Write your code using symbolic representation below.

08AL.....
08AR.....
08BL.....
08BR.....
08CL.....
08CR.....
08DL.....
08DR.....
08EL.....
08ER.....
08FL.....
08FR.....
090L.....
090R.....
091L.....
091R.....
092L.....
092R.....
093L.....
093R..... (Anonim olmayan soru ⓘ)
(-/20 Puan)

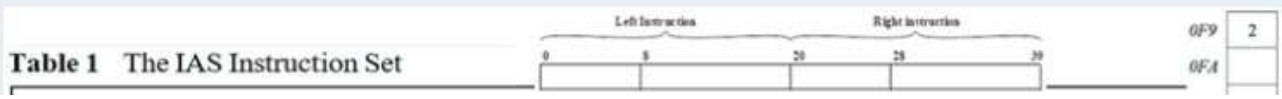

Table 1 The IAS Instruction Set

What are the name of the different cache mapping techniques?
(-/3 Puan)

direct mapping, associative mapping, set-associative mapping

14

We have an 16KB of Associative cache. It has line size of 16 bytes. The main memory size is 4GB.
a) How many TAG bits required?
b) How many comparators required?
c) What is the comparator size in bits? (Anonim olmayan soru ⓘ)
(-/15 Puan)

14_OKAN ORKUN.jpeg

15

Give two example for the cache replacement algorithms?
(-/4 Puan)

FIFO and LFU

16

What is the two different solutions for the cache coherency problem?
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Bus watching with write through, Hardware Transparency

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4

Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes. (Anonim olmayan soru ⓘ) (-/10 Puan)

a) For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache.

F0010	*01234*	*CABBE*

b) Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache.

4_OKAN ORKUN.jpeg

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