Assume that the data segment begins at 00325020h: what is the value of ESI ?
(5 Puan)

```
.data
bVal BYTE ?
wVal WORD ?
var4 BYTE 10,3 DUP(0),20
dValFirst DWORD ?
dValSecond DWORD ?
.code
mov esi,OFFSET dValFirst    ; ESI = .....
```

- 00325044h
- 00325030h
- 00325020h
- (●) 00325028h
- 00325026h

2

If 80% of an application is performed serially, what is the maximum speedup?
(5 Puan)

1/0.8

3

Twos complement of -1 as a nibble is ....
(2 Puan)

- 0111
- (●) 11111111
- 1111

1110

4

Assembly is a case sensitive language.
(2 Puan)

True

False

5

Zero flag is set when the destination is non zero.
(2 Puan)

True

False

6

SRAM is used for ..... memory, and DRAM is used for ..... memory.
(3 Puan)

short-long

high-low

dynamic-static

cache-main

low-high

Considering the input 11001010, what will be the new number if we perform the arithmetic right shift operations 3 times consecutively.
(4 Puan)

- 00011001
- 11111001
- 01010000
- 11011001
- 01010110

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Table 1 The IAS Instruction Set

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Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
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Write an IAS program to compute the factorial f(n)=n! using instructions from the Table 2 where the value of n is stored at the memory location 0FA. After the execution of your program the output value f(n) must be stored at location 0FB. For example if the content of 0FA is 4 then a value of 24 must be present in memory location 0FB. Write your code below: Hint: I added a new instruction (MOV) in Table 2 to assign a scalar value to AC. At first, think about the pseudocode (Anonim olmayan soru ⓘ)
(20 Puan)

↑ Dosyayı karşıya yükle

Dosya sayısı üst sınırı: 1 Tek dosya boyutu üst sınırı: 10MB İzin verilen dosya türleri: Word, Excel, PPT, PDF, Resim, Video, Ses

9

Overflow flag can be set due to an addition of positive and negative number.
(2 Puan)

- ○ True
- ◉ False

10

What will be the result after each operation? (Anonim olmayan soru ⓘ)
(10 Puan)

```
.data
myByte BYTE 0FFh, 0
.code
   mov al,myByte      ; AL =.....
   mov ah,[myByte+1]  ; AH =.....
   dec ah             ; AH =.....
   inc al             ; AL =.....
   dec ax             ; AX =.....
```

10.jpeg

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a) How is an 8-bit memory address divided into tag, line number, and byte number?
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c) Suppose the byte with address 1011101011 is stored in the cache. What are the addresses of the other bytes stored along with it?
(12 Puan)

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a) tag: 5 ; line: 3; bytenum:2 ; b)Line 5=101 c) 10111 010 00 , 10111 010 01 , 10111 010 10 , 10111 010 11

12

Considering the following assembly code, write the contents of the registers on an Intel CPU (Little Endian order) (Anonim olmayan soru ⓘ)
(10 Puan)

```
.data
myBytes BYTE 19h,23h,0A1h,36h
varW WORD  5432h,10FFh
.code
mov ax,WORD PTR [myBytes]          ; AX  = .....
mov ax,WORD PTR [myBytes+1]        ; AX  = .....
mov ax,WORD PTR [myBytes+2]        ; AX  = .....
mov eax,DWORD PTR myBytes          ; EAX = .....
mov bl,BYTE PTR [varW+2]           ; BL  = .....
```

12.jpeg

Dosya sayısı üst sınırı: 1 Tek dosya boyutu üst sınırı: 10MB İzin verilen dosya türleri: Word, Excel, PPT, PDF, Resim, Video, Ses

13

..... requires periodic charge refreshing to maintain data storage.
(3 Puan)

- ○ SSD
- ○ Registers
- ◉ DDR RAM
- ○ Cache

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The least significant byte occurs at the first (lowest) memory address in ..... order.
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The MOV instruction never affects the flags.
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We have an 32KB of Associative cache. It has line size of 16 bytes. The main memory size is 2GB.
a) How many TAG bits required?
b) How many comparators required?
c) What is the comparator size in bits? (Anonim olmayan soru ⓘ)
(15 Puan)

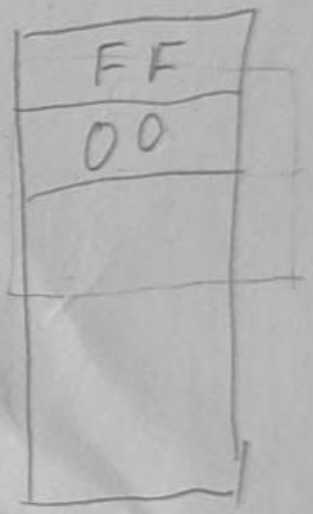
16.jpeg

Dosya sayısı üst sınırı: 1 Tek dosya boyutu üst sınırı: 10MB İzin verilen dosya türleri: Word, Excel, PPT, PDF, Resim, Video, Ses

Suleyman Dadashov 201f080f004 1:1

10)

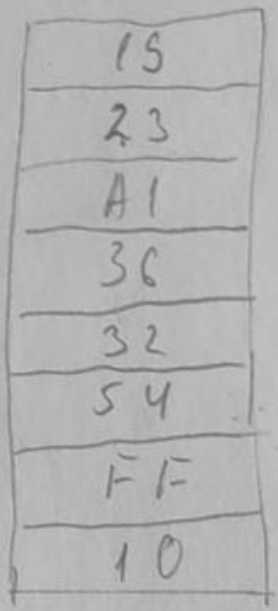
```
.data
myByte OFFh, 0
.code
  mov al, myByte          ; AL = 0FFH
  mov ah, [myByte+1]      ; AH = 00h
  dec ah                  ; AH = 0FFh
  inc al                  ; AL = 00h
  dec ax                  ; AX = FEFFh
```



Suleyman Dadashov 20180808004 1/2

12.

```
.data
myBytes Byte 19h,23h,0A1h,36h
varW    Word 5432h,10FFh
.code
mov  ax, Word PTR [myBytes] ;   Ax = 2319h
mov  ax, Word PTR [myBytes+1];  Ax = 0A123h
mov  ax, Word PTR [myBytes+2];  Ax = 36A1h
mov  eax, DWord PTR myBytes ;   Eax = 36A12319h
mov  bl, Byte PTR [varW+2];     BL = FFh
```



Suleyman Dadashov 2018080000 1-/

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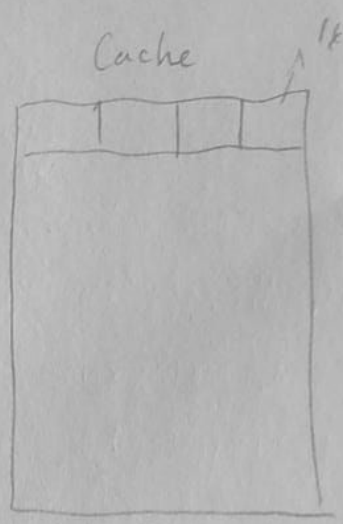
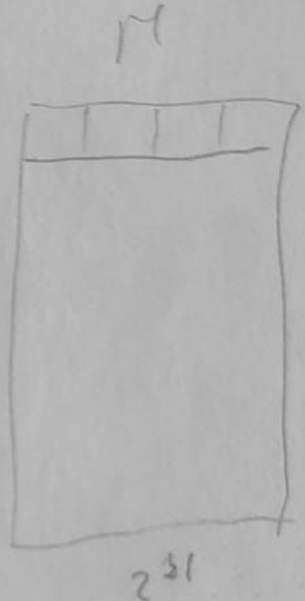




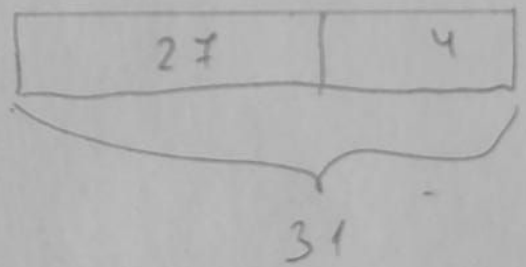
1GB $\rightarrow 2^{30}$

2GB $\rightarrow 2^{31}$

1KB $\rightarrow 2^{10}$

!

32KB $\rightarrow 2^{15}$



a.) 27

b.) 2^{11}

c.) 27

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(4 Puan)

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12.jpeg

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(5 Puan)

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dValFirst DWORD ?
dValSecond DWORD ?
.code
mov esi,OFFSET dValFirst    ; ESI = .....
```

- 00325044h
- 00325030h
- 00325020h
- (•) 00325028h
- 00325026h

2

If 80% of an application is performed serially, what is the maximum speedup?
(5 Puan)

1/0.8

3

Twos complement of -1 as a nibble is ....
(2 Puan)

- 0111
- (•) 11111111
- 1111

- 1110

4

Assembly is a case sensitive language.
(2 Puan)

- True
- False

5

Zero flag is set when the destination is non zero.
(2 Puan)

- True
- False

6

SRAM is used for ..... memory, and DRAM is used for ..... memory.
(3 Puan)

- short-long
- high-low
- dynamic-static
- cache-main
- low-high

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(10 Puan)

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   dec ah             ; AH =.....
   inc al             ; AL =.....
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10.jpeg

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WhatsApp Image 2023-06-...

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(5 Puan)

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wVal WORD ?
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```

- 00325044h
- 00325030h
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1/0.8

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- 11111111
- 1111

28

Considering LRU algorithm with a 3 byte cache area, what would be the content of the cache area after accessing the bytes A,B,B,A,C,E,D,C,A respectively. (4 Points)

- [x] ABC
- [ ] DCA
- [x] ABC
- [ ] EDA
- [ ] DAC
- [ ] ABB

14

The least significant byte occurs at the first (lowest) memory address in ..... order.
(3 Puan)

- ○ Big endian
- ◉ Little endian
- ○ Mid endian
- ○ Inverse endian

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The MOV instruction never affects the flags.
(2 Puan)

- ◉ True
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a) How many TAG bits required?
b) How many comparators required?
c) What is the comparator size in bits? (Anonim olmayan soru ⓘ)
(15 Puan)

2

What is the purpose of the control unit in a CPU?

(2 Points)

- ○ Perform arithmetic operations
- ○ Manage data storage
- ○ Execute program instructions
- ◉ Coordinate the operations of the CPU

24

Which of the following is/are DEFINITELY CORRECT after executing the "MOV AX, 0" command (3 Puan)

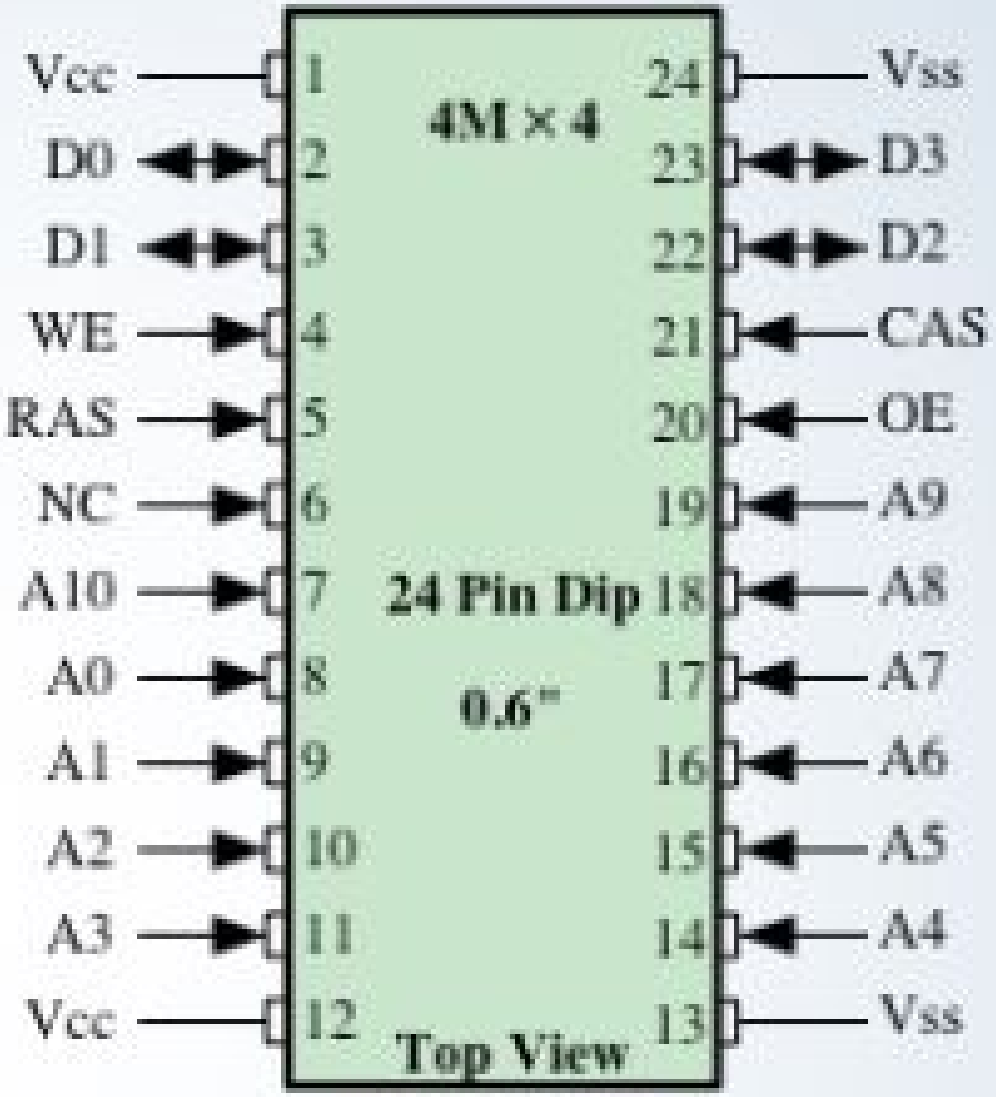
- [x] The content of AX is 0
- [x] Content of AH is 0
- [ ] The Zero flag is set to 1
- [ ] The sign flag is set to 0
- [ ] Overflow flag is 0
- [x] Content of AL is 0
- [ ] The zero flag is set to 0

Examples of processors with the RISC architecture include MIPS, PowerPC, Atmel's AVR, the Microchip PIC processors, Arm processors, RISC-V, and all modern microprocessors have at least some elements of RISC. The progression from 8- and 16-bit to 32-bit architectures essentially forced the need for RISC architectures. 9 Oca 2018

Who developed the concept of a stored-program computer?

(2 Points)

- ○ Alan Turing
- ◉ John von Neumann
- ○ Charles Babbage
- ○ Dennis Ritchie
- ○ Edsger Dijkstra



(b) 16 Mbit DRAM

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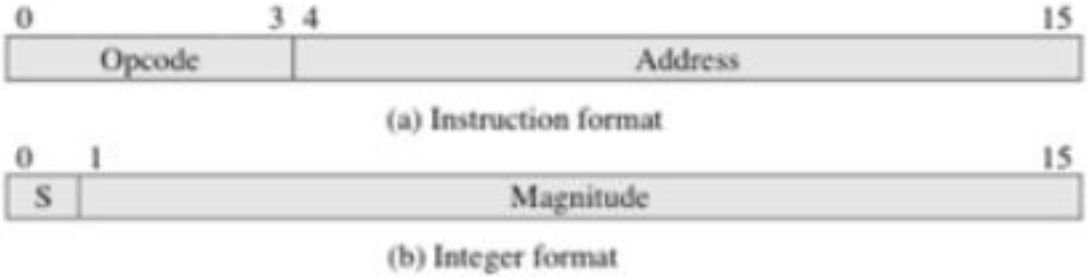
- ABC
- DCA
- ABC
- EDA
- DAC
- ABB

What will be the value in memory addresses 453, 454 and 455 at the end of the execution.

(6 Points)



Partial instruction set:

0001 : Load AC from Memory
0010 : Store AC to Memory
0011 : Subtract AC from Memory
0100 : Multiply to AC from Memory
0101 : Add to AC from Memory
0110 : Halt

Memory

199	2 2 0 2
200	1 4 5 3
201	4 4 5 5
202	2 4 5 4
203	6 4 5 4
.....	
453	0 0 0 3
454	0 0 0 7
455	0 0 0 2

CPU Registers

PC	0 2 0 0
AC	
IR	

Memory

199	
200	
201	
202	
203	
453	
454	
455	

CPU Registers

PC	
AC	
IR	

3,7,2

3B_CSE 206_Computer Organization_Ö_1)

Lower cost and reduced power consumption

8

What is the concept of spatial locality in cache memory?
(2 Puan)

Instructions and data that are used together tend to be used together in the future

Instructions and data that are far apart tend to be accessed together

Recently accessed instructions and data are likely to be accessed again soon

Instructions and data that are spatially close to each other tend to be used together

9

Which cache organization uses a combination of direct mapping and set-associa mapping?
(2 Puan)

Virtual cache

N-way set-associative cache

Fully associative cache

B_CSE 206_Computer Organization_Ö_1)

- Multi-level cache

10

What is the purpose of the dirty bit in a cache memory entry?

(2 Puan)

- To indicate that the cache line has been accessed recently
- To indicate that the cache line is invalid and needs to be replaced
- To indicate that the cache line contains modified data that needs to be written back to the m
- To indicate that the cache line is shared among multiple processors
- To indicate that the cache line is malfunctioning

11

Which interface standard is commonly used for high-speed data transfer betwee and external storage devices?

(2 Puan)

- USB
- SATA

B_CSE 206_Computer Organization_Ö_1)

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- DCA
- CED
- ACD
- ABC
- ABD
- DCB
- DAC

25

What is the main function of the Link Layer in the QPI protocol? (2 Puan)

- It provides error detection and correction mechanisms.
- It manages the flow control and error control between nodes.
- It handles the logical addressing and routing of packets.
- It performs data encoding and decoding operations

26

Which bridges do PCI and PCIe slots are connected respectively? (3 Puan)

- North Bridge, South Bridge
- South Bridge, North Bridge
- Both to North Bridge
- Both to South Bridge

27

Which of the following code group is in row major order? (6 Puan)

24°C

```
for (i = 0; i < row; i++) {
    for (j = 0; j < col; j++) {
        a[i][j] = 0;
        for (k = 0; k < row; k++) {
            //Matrix Multiplation
            a[i][j] += b[i][k] * c[k][j];
        }
    }
}
```

31

Which of the following is not valid for an SSD drive (2 Puan)

- [ ] Seek time
- [ ] Rotational delay
- [ ] Access time
- [ ] Transfer time

Which of the following is an example of a RISC architecture?

(2 Puan)

- Sun SPARC
- AMD64
- ARM Cortex
- Intel Itanium
- X64

6

Which type of computer memory provides the fastest access time?

(2 Puan)

- ROM
- Primary Storage
- Secondary Storage
- Static memory
- DDR4

7

What is the advantage of a fully associative cache mapping technique?

(2 Puan)

- Lower cache access time and reduced latency
- Higher cache hit rate and reduced cache conflicts
- Simpler cache indexing and addressing
- Lower cost and reduced power consumption

8

What is the concept of spatial locality in cache memory?

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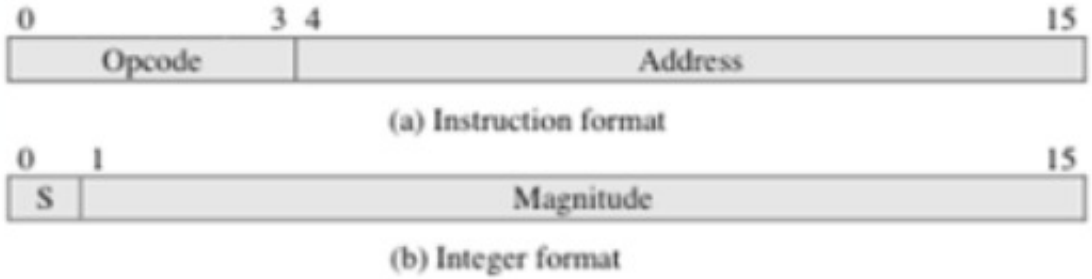
What will be the value in memory addresses 453, 454 and 455 at the end of the execution.

(6 Puan)



Partial instruction set:

0001 : Load AC from Memory
0010 : Store AC to Memory
0011 : Subtract AC from Memory
0100 : Multiply to AC from Memory
0101 : Add to AC from Memory
0110 : Halt

Memory

199	2 2 0 2
200	1 4 5 3
201	4 4 5 5
202	2 4 5 4
203	6 4 5 4
.....	
453	0 0 0 3
454	0 0 0 7
455	0 0 0 2

CPU Registers

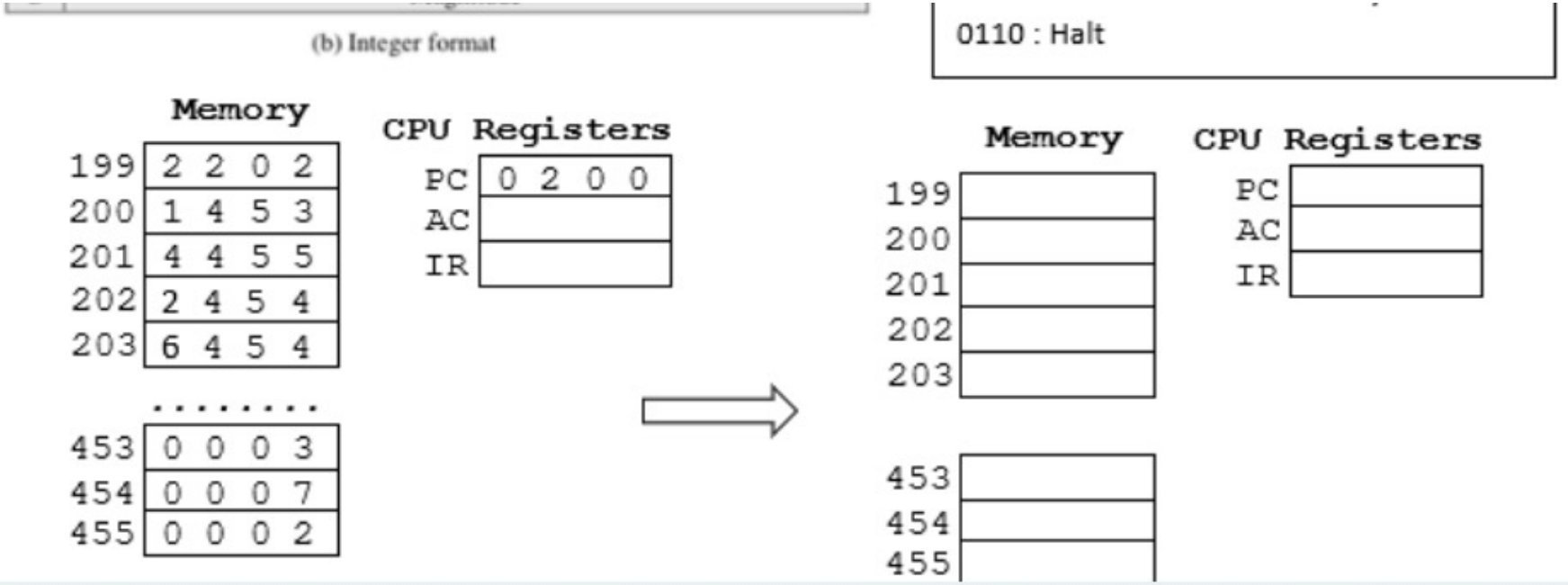
PC	0 2 0 0
AC	
IR	

Memory

199	
200	
201	
202	
203	
453	
454	
455	

CPU Registers

PC	
AC	
IR	



- 3,7,2
- 3,6,2
- 3,9,2
- 10,7,2

13

What is the purpose of a DMA (Direct Memory Access) controller in a computer system? (3 Puan)

- (●) To manage the memory hierarchy and handle memory requests from the CPU
- ( ) To control the flow of data between the CPU and cache memory
- ( ) To execute I/O instructions and perform logic operations
- ( ) To transfer data directly between external devices and memory without CPU intervention

14

1. What is the purpose of the memory-mapped I/O technique? (2 Puan)

- ( ) To connect multiple external memory devices in parallel
- ( ) To allocate memory dynamically for I/O operations
- (●) To use the same address space for both memory and I/O operations, simplifying the communication between the CPU and external devices
- ( ) To improve the access time of external memory devices

26

Which bridges do PCI and PCIe slots are connected respectively? (3 Points)

- North Bridge, South Bridge
- South Bridge, North Bridge
- Both to North Bridge
- Both to South Bridge