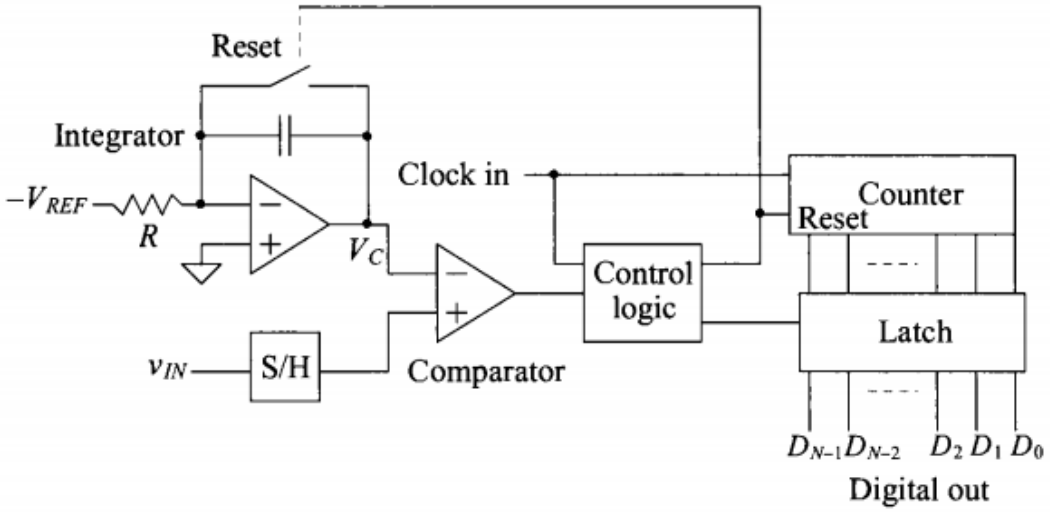
## GETTING STARTED WITH CADENCE

1. Starting the Cadence Software Use the installed database to do your work and the steps are as follows:
2. Change to the course directory by entering this command: > cd ~/Database/***cadence_analog_labs_613***
3. You will start the Cadence Design Framework II environment from this directory because it contains cds.lib, which is the local initialization file. T
4. The library search paths are defined in this file.
5. The ***Cadence_Analog_labs_613*** directory contains Solutions folder and also Work folder.
6. Inside Work folder you can create new cell / modifications of the cell locally without affecting your Source cell present inside Solutions directory.
7. In the same terminal window, enter: > ***virtuoso*** & The virtuoso or Command Interpreter Window (CIW) appears at the bottom of the screen.

## BLOCK DIAGRAM

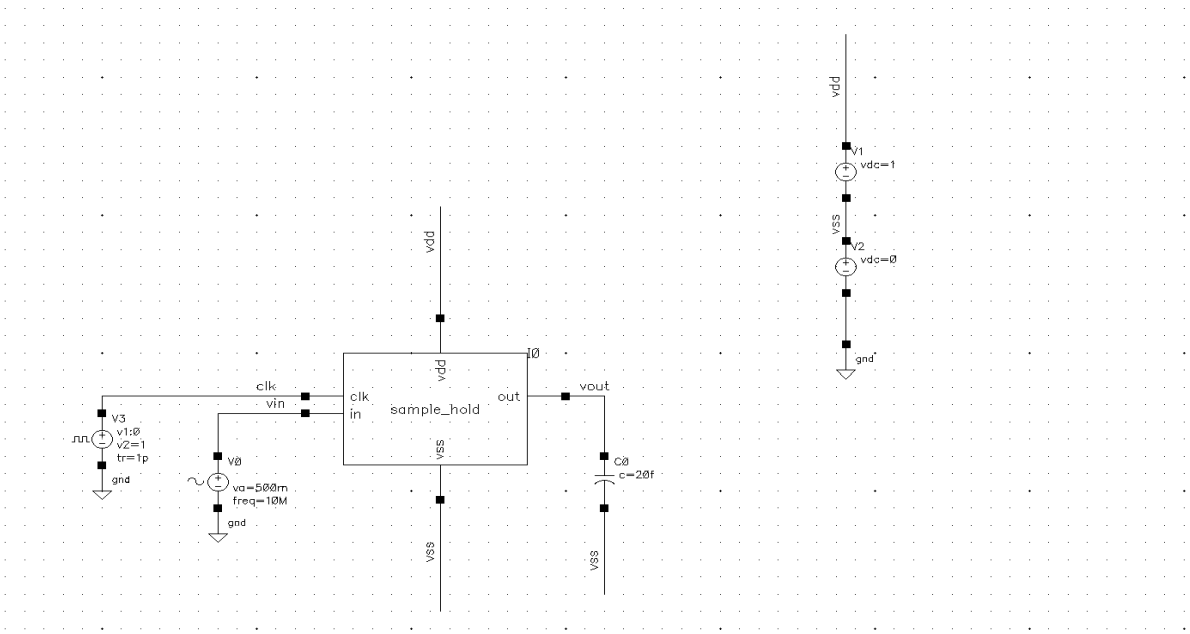


# 1. SAMPLE AND HOLD CIRCUIT

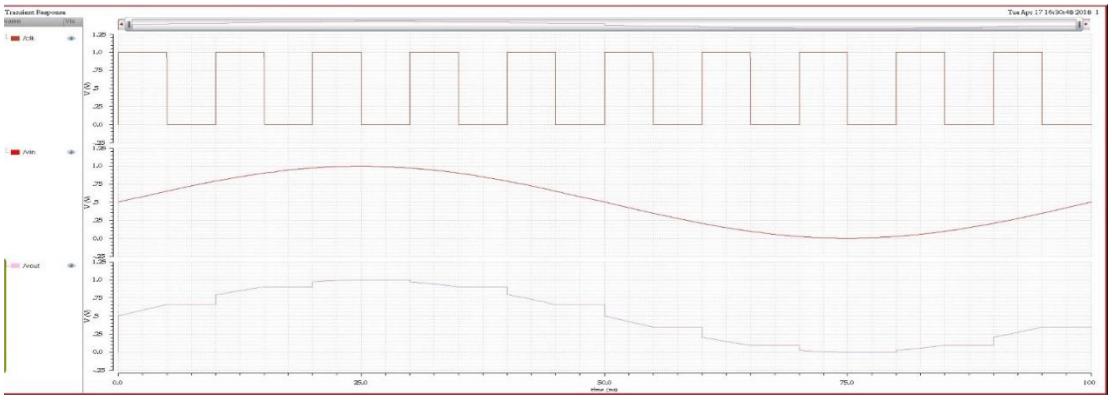
In electronics, a **sample and hold** (**S/H**, also "follow-and-hold") circuit is an analog device that samples (captures, takes) the voltage of a continuously varying analog signal and holds (locks, freezes) its value at a constant level for a specified minimum period of time. Sample and hold circuits and related peak detectors are the elementary analog memory devices. They are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process.

```
`include "constants.vams"
`include "disciplines.vams"

module sample_hold(vdd,vss,in,out,clk);

inout vdd,vss;
input in,clk;
output out;
electrical in,out,clk;

parameter real clk_vth=0.5,delay=0,ttime=1p;
real v;

analog
begin
if((V(clk)>clk_vth))
v=V(in);
// @(cross(V(clk)-clk_vth,+1))
// v=V(in);
V(out) <+ transition(v,delay,ttime);
end


endmodule
```

## 1.1 Test Circuit




| Library name | Cellview name | Properties/Comments |
|---|---|---|
| analogLib | Vpulse | v1=0, v2=1,td=0 tr=tf=1ps, ton=10n, T=20n |
| analogLib | vdc,vsin | vdc=1,0 va=500m,10Mhz |
| analogLib | Gnd | |
| myDesignLib | SampleAndHold symbol | |



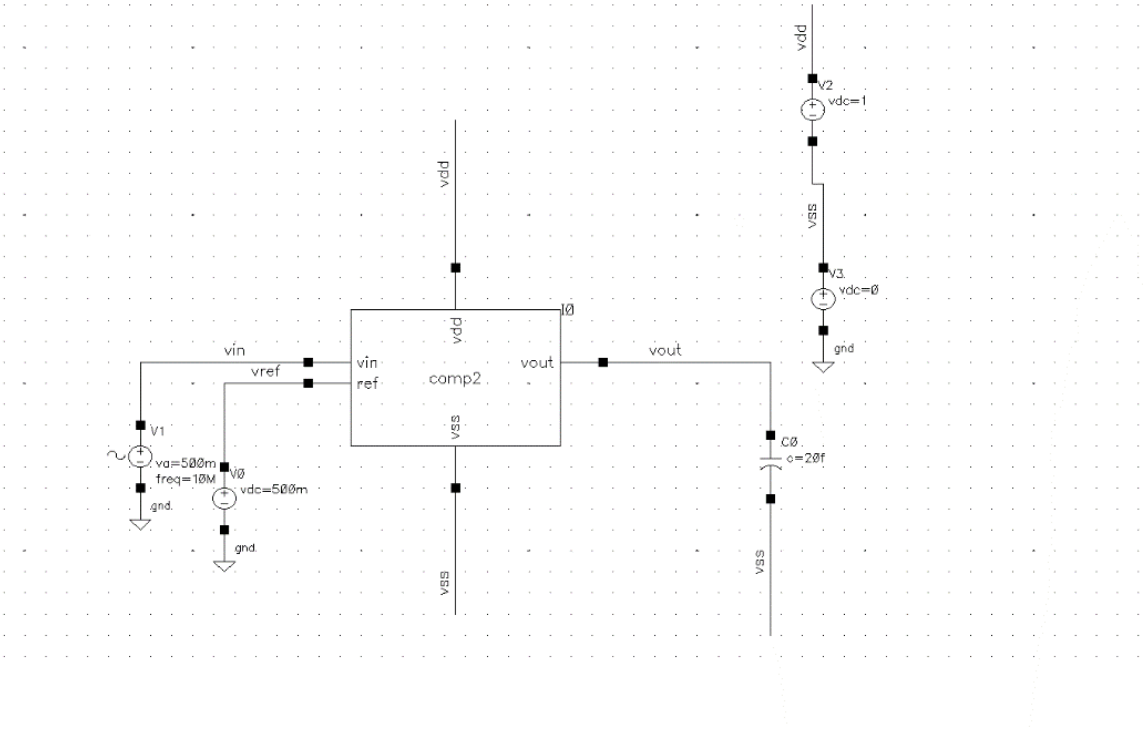
## 2. **COMPARATOR**

In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger.It has two analog input terminals V+ and V- and one binary digital output Vo. The output is ideally

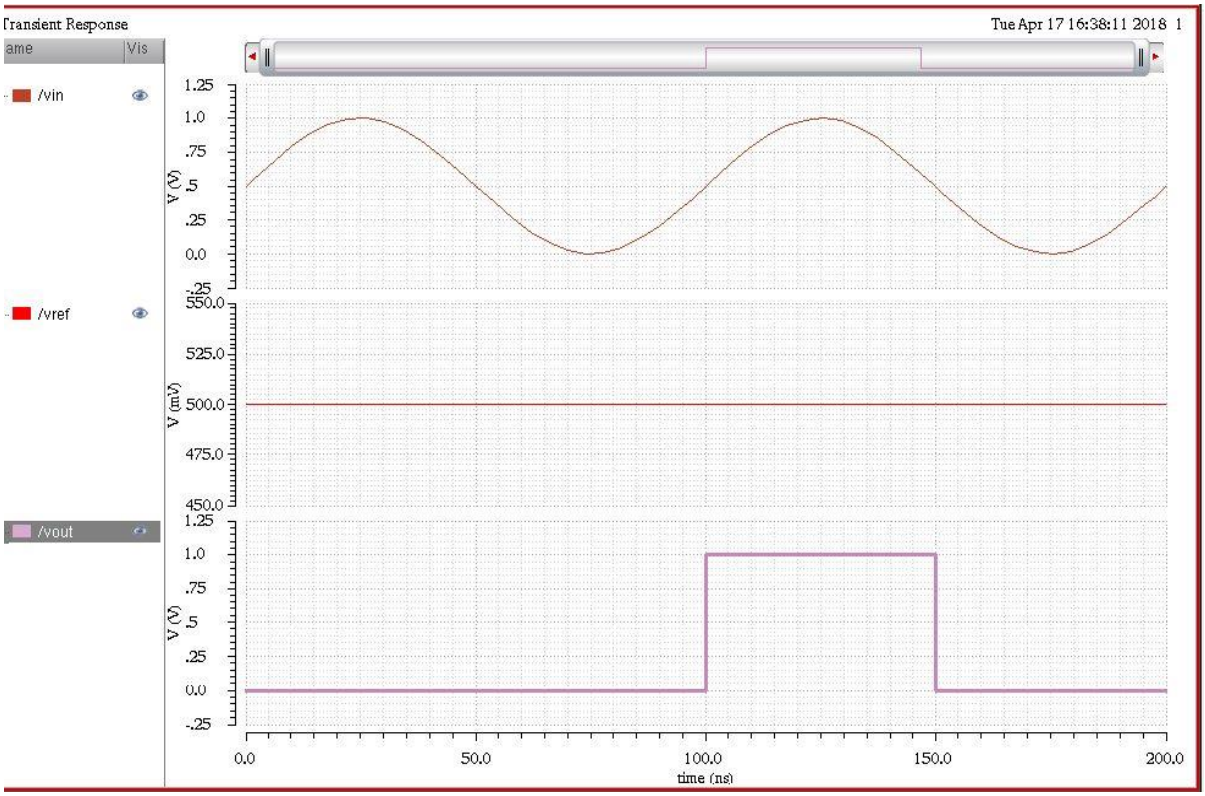
Vo= 1, if V+ > V-

0, if V- > V+

```
`include "constants.vams"
`include "disciplines.vams"

module comp2(vin,vout,vdd,vss,ref);

input vin,ref;
inout vss,vdd;
output vout;

parameter delay=0,ttime=1p;
electrical vin,ref,vdd,vout,vss;
real result;
analog begin
@(cross((V(vin)-V(ref)),0) or initial_step)
if (V(vin)>V(ref))
result=V(vdd);
else
result=V(vss);
V(vout)<+ transition(result,delay,ttime);
end


endmodule
```

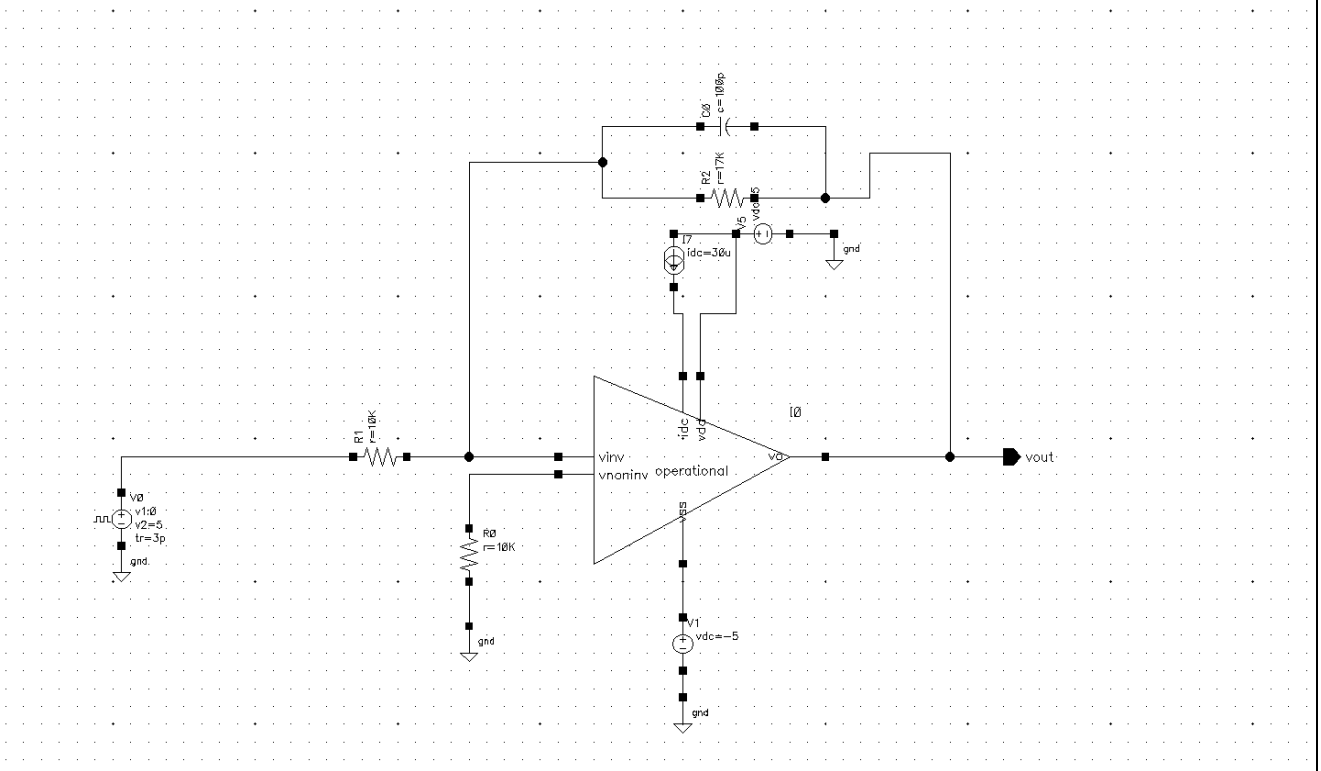


| Library name | Cellview name | Properties/Comments |
|---|---|---|
| analogLib | Vsin | Va=500m<br>Frequency=10M Hz |
| analogLib | vdc, | vdc=500m |
| analogLib | Gnd | |
| MyDesign Lib | Comparator symbol | |



# 3. INTEGRATOR

An **integrator** in measurement and control applications is an element whose output signal is the time integral of its input signal. It accumulates the input quantity over a defined time to produce a representative output.

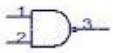



| Library name | Cellview name | Properties/Comments |
|---|---|---|
| analogLib | Vpulse | v1=0, v2=5,td=0 tr=tf=3ps, ton=10n, T=20n |
| analogLib | vdc, | vdc=5,-5 |
| analogLib | Gnd | |
| | Idc | 30uA |
| analogLib | Res | R1=5.6K,R2=10K |
| analogLib | Cap | C=100pF |
| myDesignLib | Operational amplifier symbol | |

# 4. NAND GATE

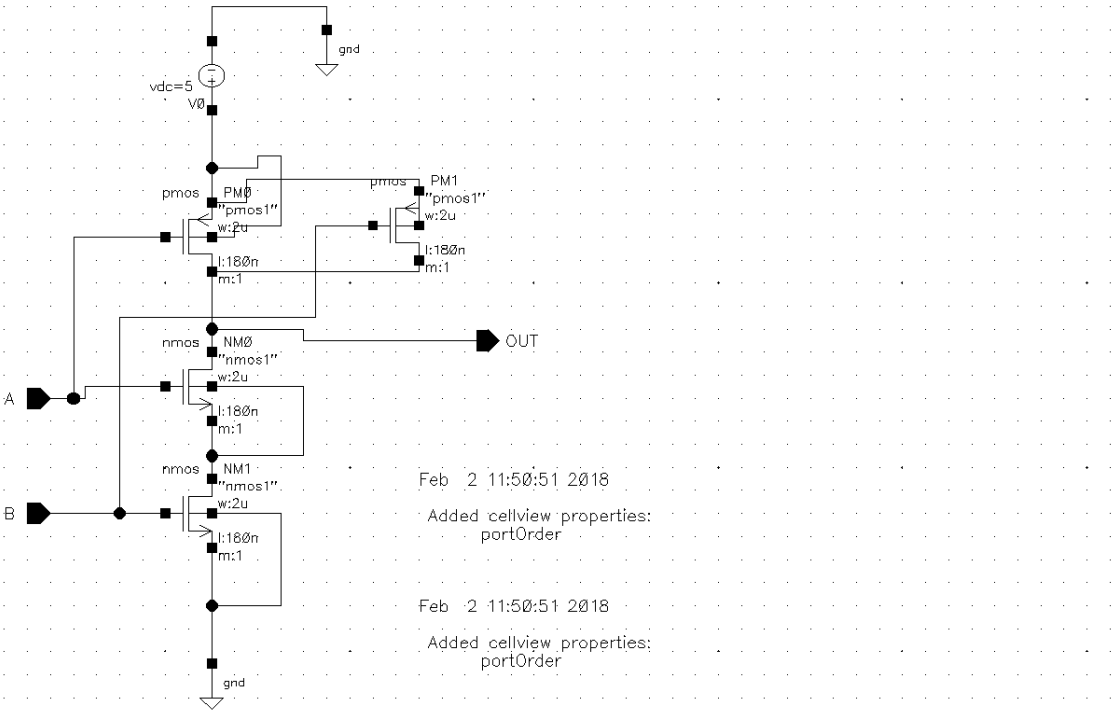
2 Input NAND Gate

NAND Gate




TRUTH TABLE

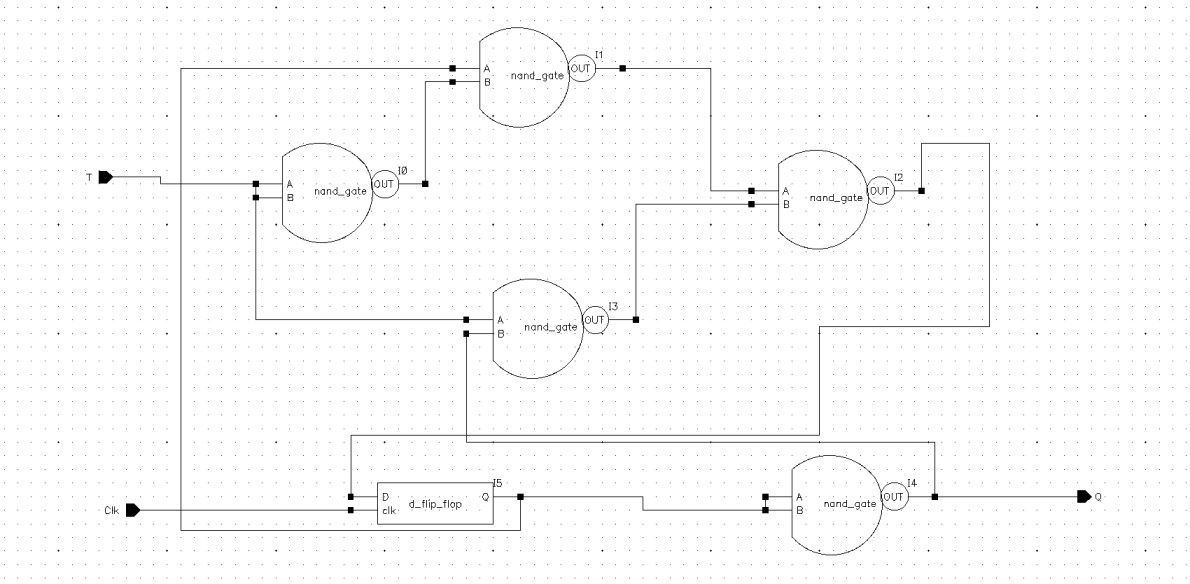
| INPUTS | | OUTPUT |
|---|---|---|
| X | Y | Z |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



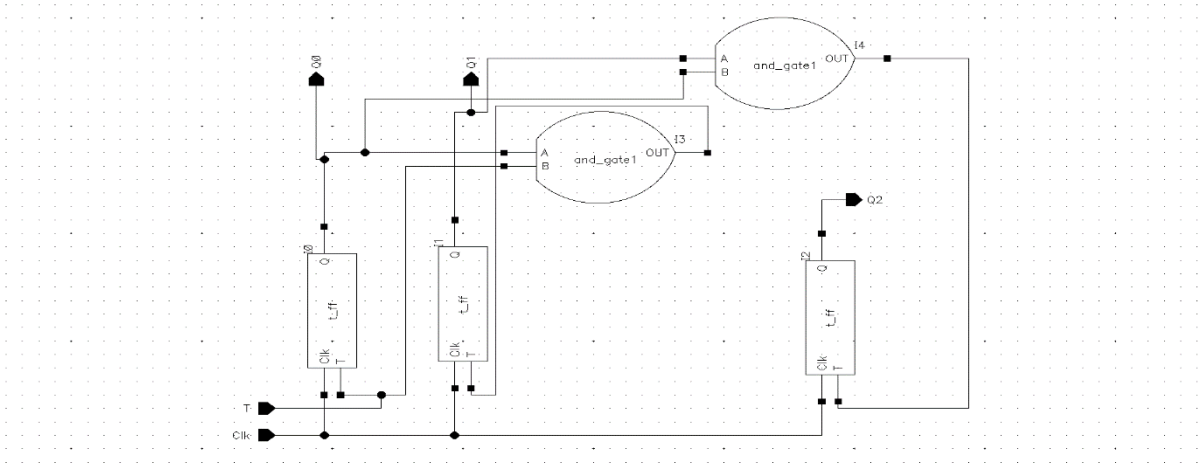

# 5. COUNTER FORMATION

## 5.1 T-Flip Flop

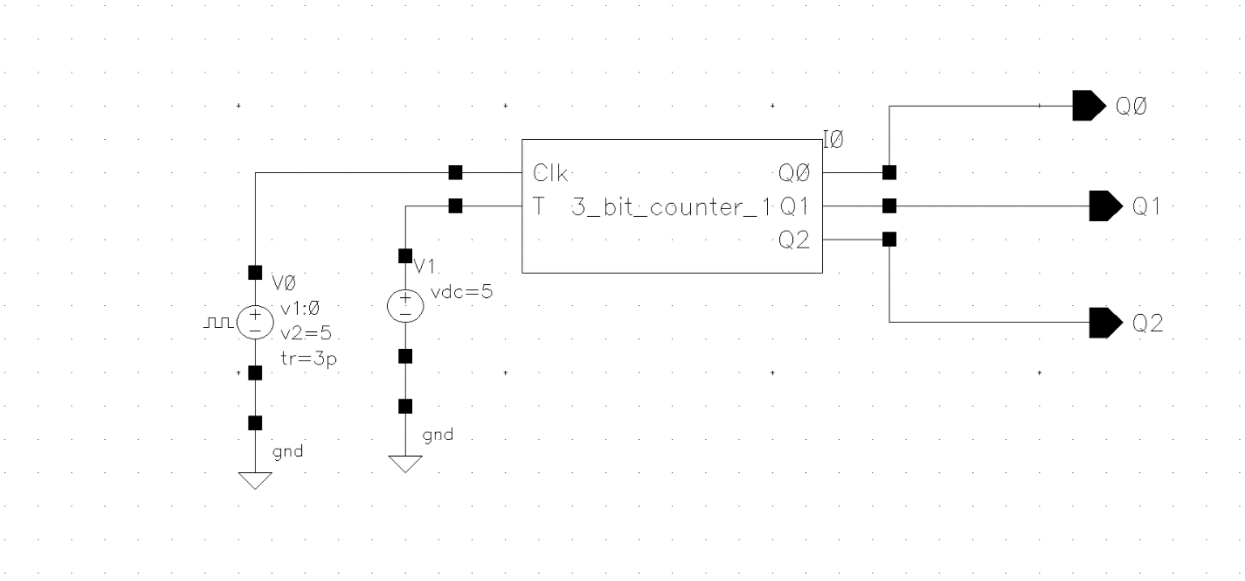
| T | Q | Q' |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |



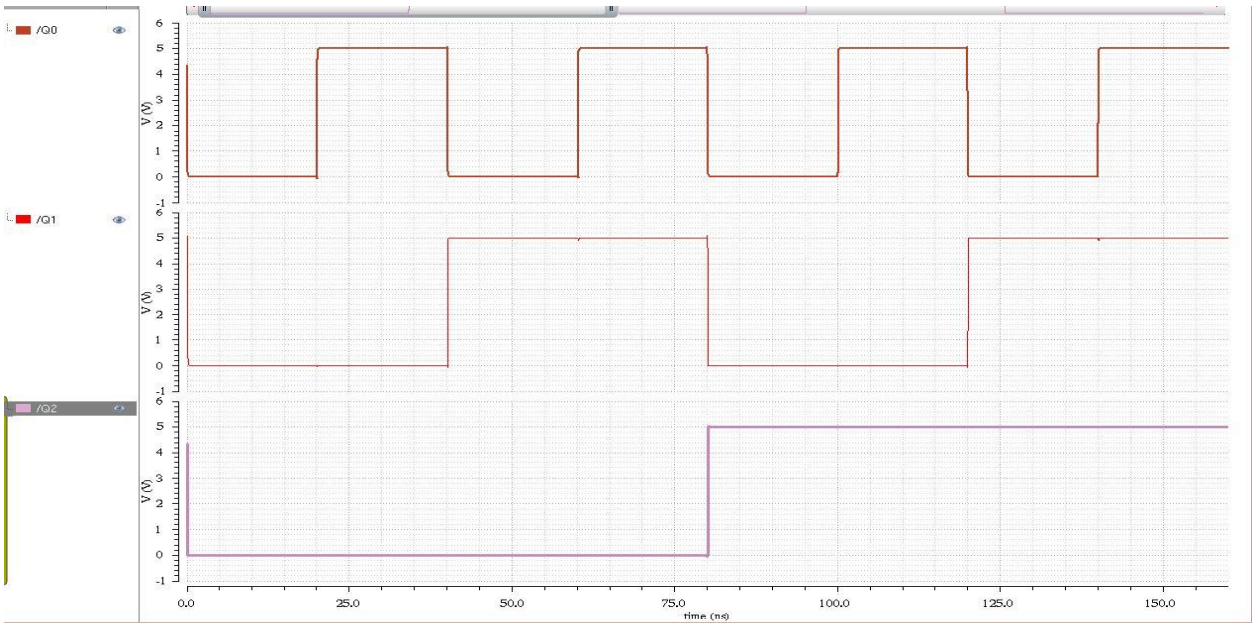

## 5.2 COUNTER CIRCUIT



## 5.3 COUNTER TEST CIRCUIT

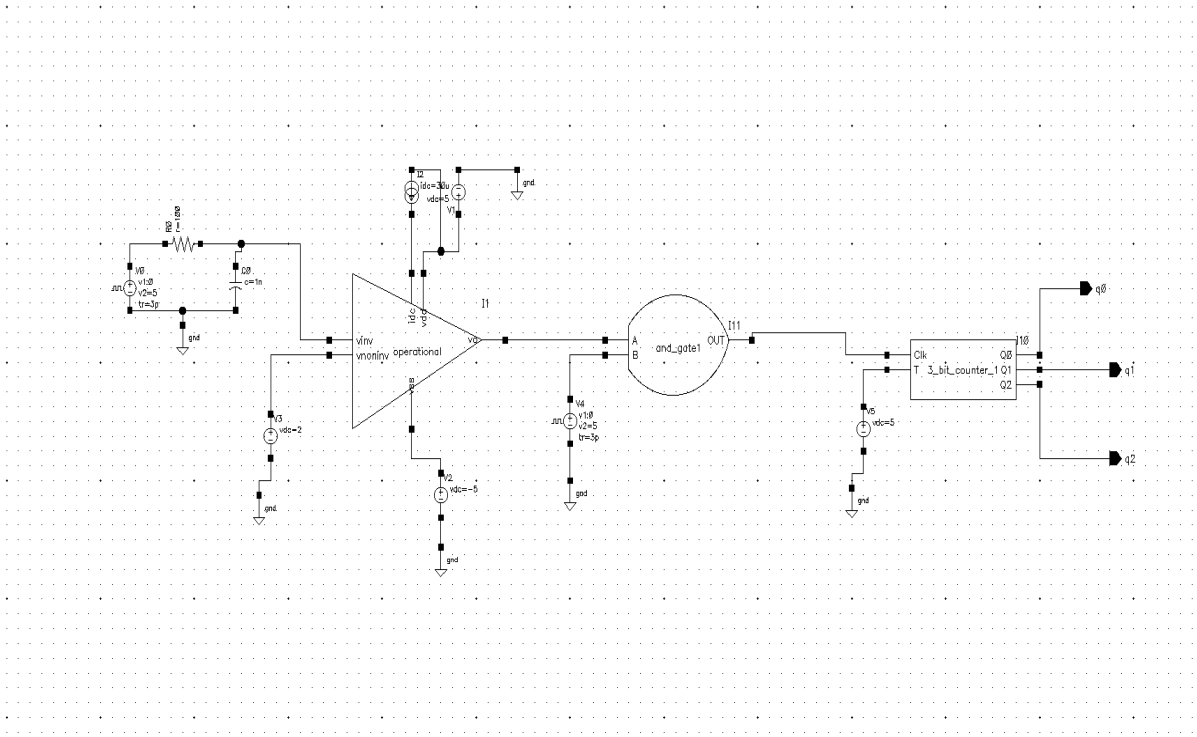



| Library name | Cellview name | Properties/Comments |
|---|---|---|
| myDesignLib | vpulse | v1=0, v2=5 ,td=0 tr=tf=3ps, ton=25n, T=150n |
| analogLib | vdc, | vdc=5 |
| analogLib | gnd | |
| myDesignLib | Counter symbol | |

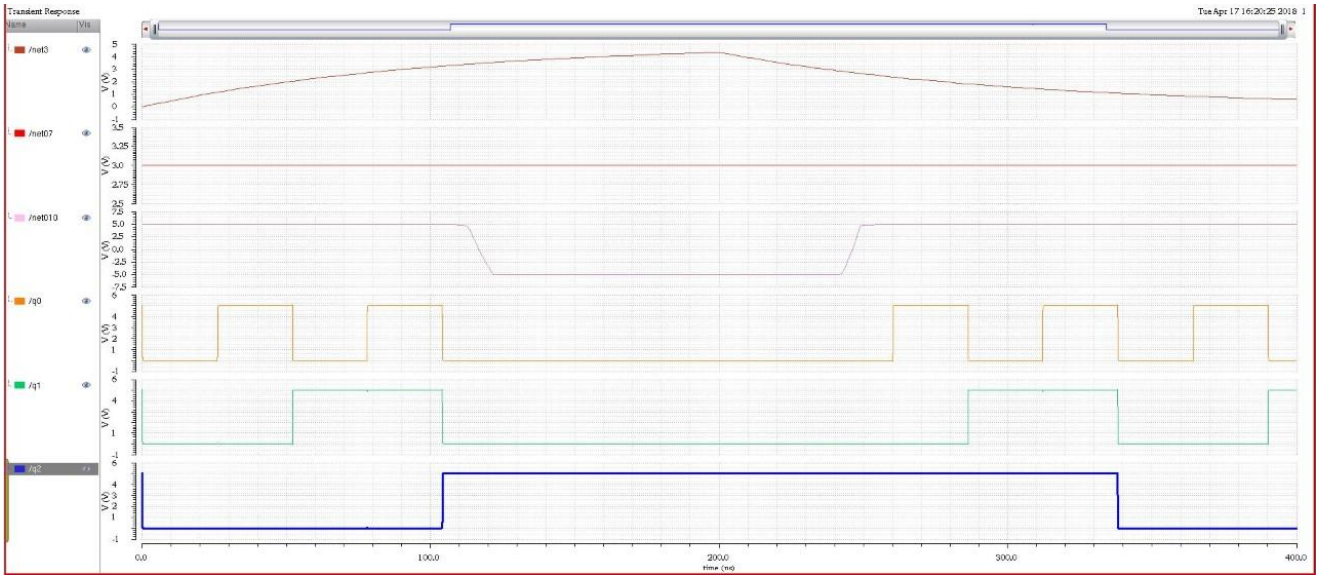


# 6. OUTPUT

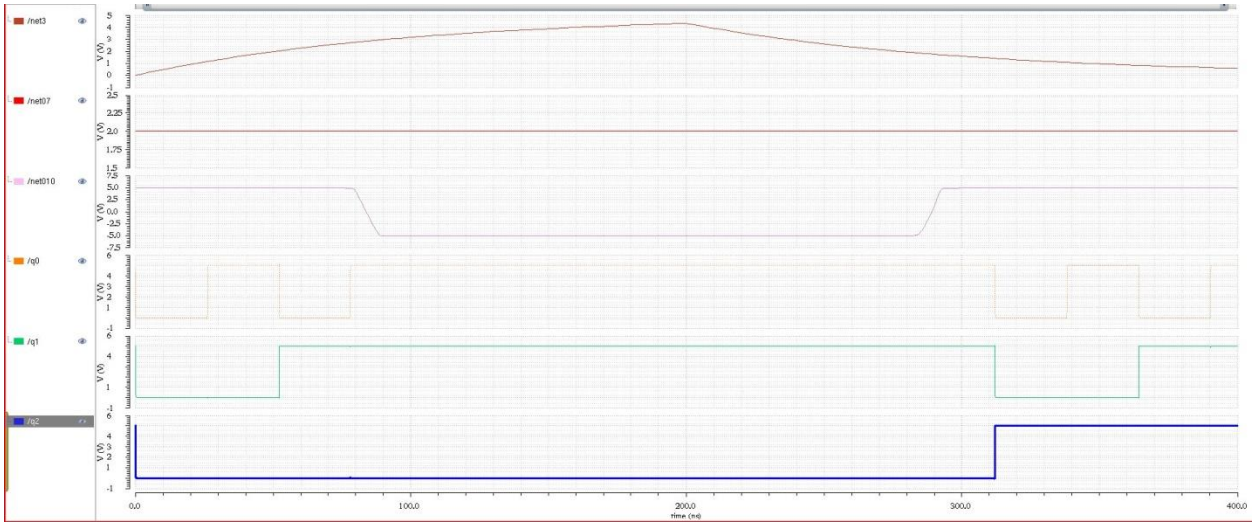
A counter determines the number of clock pulses that are required before the integrated value of reference voltage is equal to the sampled input signal. The number of clock pulses is proportional to the actual value of the input, and the output of the counter is the actual digital representation of the analog voltage.
Since the reference is a DC voltage, the output of the integrator should start at zero and linearly increase with a slope that depends on the gain of the integrator. Notice that the reference voltage is defined as negative so that the output of the inverting integrator is positive.



Vin=3v Output-100




Vin=2v Output- 011



## 7. CONCLUSION

- The single-slope ADC suffers the disadvantage of calibration drift. The accurate correspondence of this ADC's output with its input is dependent on the voltage slope of the integrator being matched to the counting rate of the counter (the clock frequency). With the digital ramp ADC, the clock frequency had no effect on conversion accuracy, only on update time. In this circuit, since the rate of integration and the rate of count are independent of each other, variation between the two is inevitable as it ages, and will result in a loss of accuracy. The only good thing to say about this circuit is that it avoids the use of a DAC, which reduces circuit complexity.
- An answer to this calibration drift dilemma is found in a design variation called the dual-slope converter. In the dual-slope converter, an integrator circuit is driven positive and negative in alternating cycles to ramp down and then up, rather than being reset to 0 volts at the end of every cycle. In one direction of ramping, the integrator is driven by the positive analog input signal (producing a negative, variable rate of output voltage change, or output slope) for a fixed amount of time, as measured by a counter with a precision frequency clock.
- Then, in the other direction, with a fixed reference voltage (producing a fixed rate of output voltage change) with time measured by the same counter. The counter stops counting when the integrator's output reaches the same voltage as it was when it started the fixed-time portion of the cycle.
- The amount of time it takes for the integrator's capacitor to discharge back to its original output voltage, as measured by the magnitude accrued by the counter, becomes the digital output of the ADC circuit.