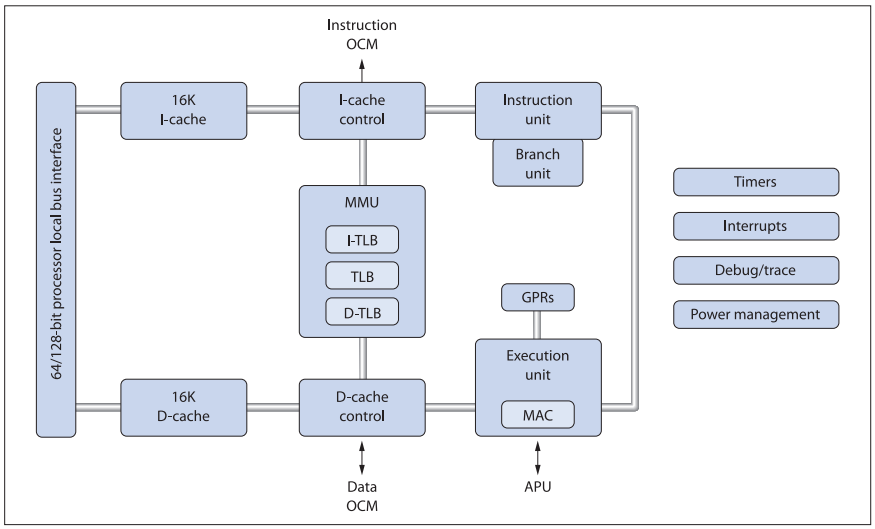
IBM PowerPC 405 Embedded Core

Highlights

- ***Compatible with the scalable and flexible PowerPC® instruction set architecture to facilitate ease of software migration***
- ***Optimized for price/performance leadership and low power system-on-a-chip (SoC) designs***
- ***Available through the Power Architecture™ licensing program and in the IBM core library for integration with peripheral and application-specific macro cores to develop SoC solutions***
- ***Supports product differentiation via inclusion of custom logic and instructions on the auxiliary processor unit (APU) interface***
- ***JTAG and trace FIFO ports enable robust debug capabilities, even in complex SoC designs***
- ***Supported by an extensive ecosystem through IBM's PowerPC tools program***
- ***Full-function simulation models are available to support SystemC environments***



PowerPC 405 core block diagram

Overview

The IBM PowerPC 405 core is a 32-bit RISC CPU core providing up to 400 MHz and 608 DMIPS performance as implemented in IBM's advanced 90-nm copper CMOS technology. The 405 core employs the scalable and flexible Power Architecture technology, optimized for embedded applications.

The licensable embedded core integrates a scalar five-stage pipeline, separate instruction and data caches, a JTAG port, trace FIFO, multiple timers and a memory management unit (MMU), with 1.52 DMIPS/MHz performance.

The PowerPC 405 core's performance, low power specifications and design attributes make it an ideal solution for emerging consumer, storage and wired or wireless communications applications.

Hard and soft core options

The PowerPC 405 core is available as a hard (fixed layout) or soft macro. The hard cores are available in IBM's premium process technologies or fab-optimized versions with the IBM Business Partner fabs. The fully synthesizable soft core provides the flexibility of fabrication in multiple foundries.

PowerPC 405 core parametrics

Technology	130 nm	90 nm	Fully synthesizable
Fabs supported	IBM, Chartered	IBM, Chartered, Samsung	All
Frequency (worst-case conditions)	366 MHz	400 MHz	250-300 MHz (process dependent)
Performance (estimated)	555 DMIPS	608 DMIPS	380-456 DMIPS
Typical power dissipation (estimated)	0.5 mW/MHz @ 1.5 V 0.3 mW/MHz @ 0.9 V	0.19 mW/MHz @ 1.1 V	0.25-0.6 mW/MHz (process dependent)
Power supply	1.5 V	1.1 V	Process dependent
Temperature range	-40°C to +105°C	-40°C to +105°C	-40°C to +105°C
Die size, CPU + L1	3.8 mm^2	2.0 mm^2	Process dependent

The 405 core can be integrated with peripheral and application-specific macro cores using the CoreConnect™ bus architecture to develop custom SoC solutions. Peripheral options include memory controllers, DMA controllers, PCI interface bridges and interrupt controllers.

A comprehensive portfolio of PowerPC family support tools is available through the extensive IBM Business Partners network. Offerings include peripheral IP, operating systems, compilers, debuggers, simulators and emulators and design services. The PowerPC 405 core is designed to work with industry-standard EDA tools.

PowerPC 405 CPU

- *Compatible with PowerPC user instruction set architecture*
- *Scalar five-stage pipeline*
- *Thirty-two 32-bit general purpose registers*
- *Hardware multiply and divide*
- *16-bit x 16-bit MAC*
- *Branch prediction*

Cache controllers

- *Separate 16-KB I- and D-cache units with parity*
- *Fill-first, data forwarding*
- *Non-blocking flush operations*
- *Programmable loads and stores*

Memory management unit

- *Variable page sizes (1 KB – 16 MB)*
- *64-entry fully-associative translation lookaside buffer (TLB)*

I/O interfaces

- *64/128-bit CoreConnect processor local bus (PLB) interface supported*
- *Supports n:1 and n:2 CPU-to-PLB frequency ratios*
- *APU interface*
- *On-chip memory (OCM)*
- *JTAG*

Timers

- *64-bit time-base*
- *Programmable interval timer*
- *Fixed interval timer*
- *Watchdog timer*

Debug support

- *4 instruction address, 2 data address, and 2 data value breakpoints*
- *Real-time non-invasive trace*
- *Exclusive traceback capability*

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IBM Systems and Technology Group
2070 Route 52, Bldg. 330
Hopewell Junction, NY 12533-6351

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