

Spineboard Testing Report U4

(LTC blew up) Pt 1

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Background

This report will be used as a new iteration of the testing reports from before. This report aims to check and validate further to help understand the spine boards more. Bench testing will split into 2 stages. The first stage will be using two 25 V supply on both sides and then the second stage will be testing with two 25 V supply in series on one of the LTC chips and a third 25V supply on the other LTC chip so it can still communicate. The second stage was added so we can simulate the LTC chip on the segment a bit better. Cell balancing will be also tested using old m19e cells.

Resources to understand Spine Boards

[Datasheets](#)

[Spineboard Schematic](#)

[Spineboard BOM](#)

BLOCK DIAGRAM

LTC6811-1

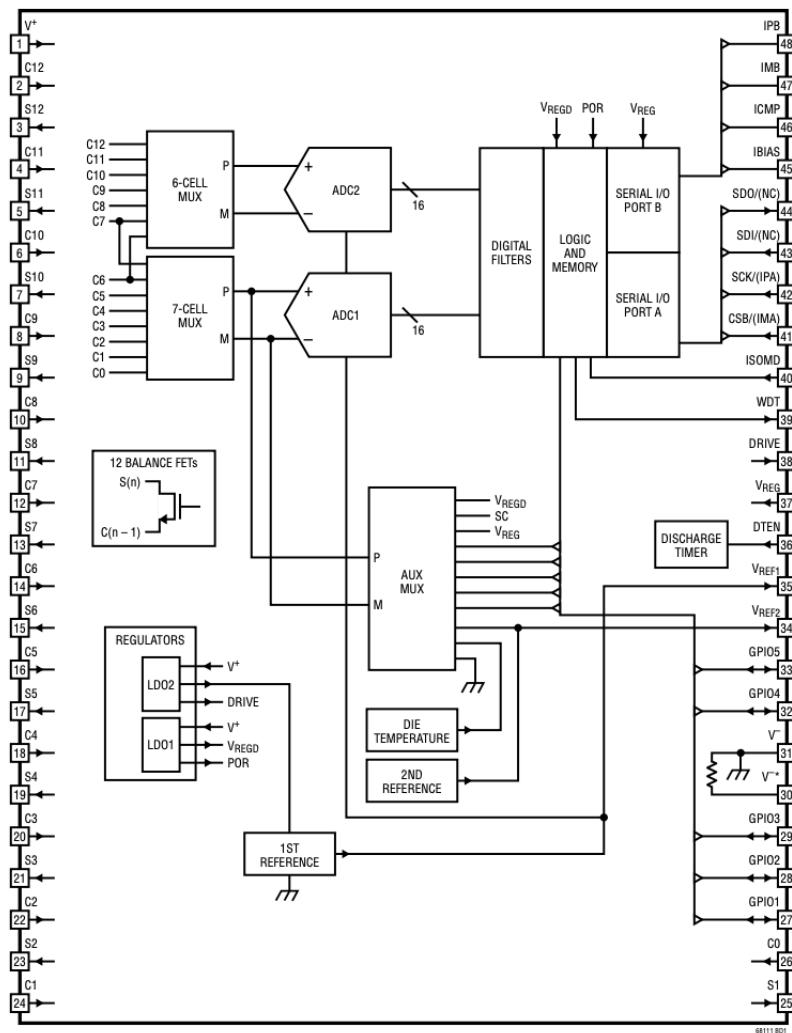


Figure 1- Block diagram of the LTC 6811-1 chip

Definitions

T2 end of board: This refers to the end of the board that has the transformer labelled T2 on it. It is the end that needs to be connected to the masterboard or the previous spineboard in the daisy chain (the previous board being closer to the masterboard in the daisy chain). A close up picture of the T2 end of the board can be seen below:

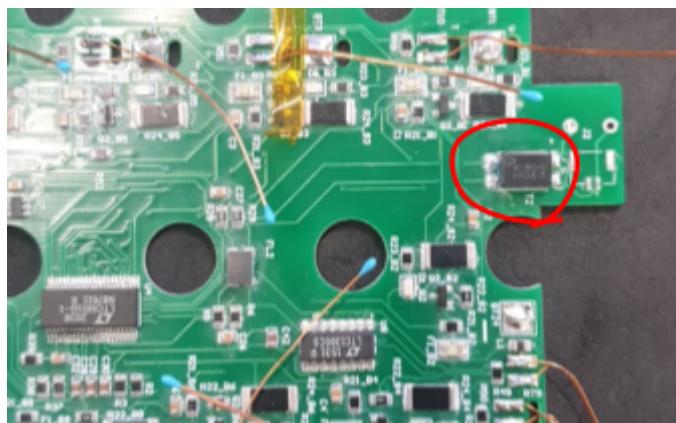


Figure 2: Close up of T2 end of board with the T2 transformer circled

Voltage taps: labelled BT xx on the board. They are labelled in order, with the most positive cell being connected to BT23. The exception to this is BT24, which is the ground of the most negative cell. The red lines in the image below show the order of connections for the cells (or for the connections in a resistive voltage divider network), the most positive being at the top

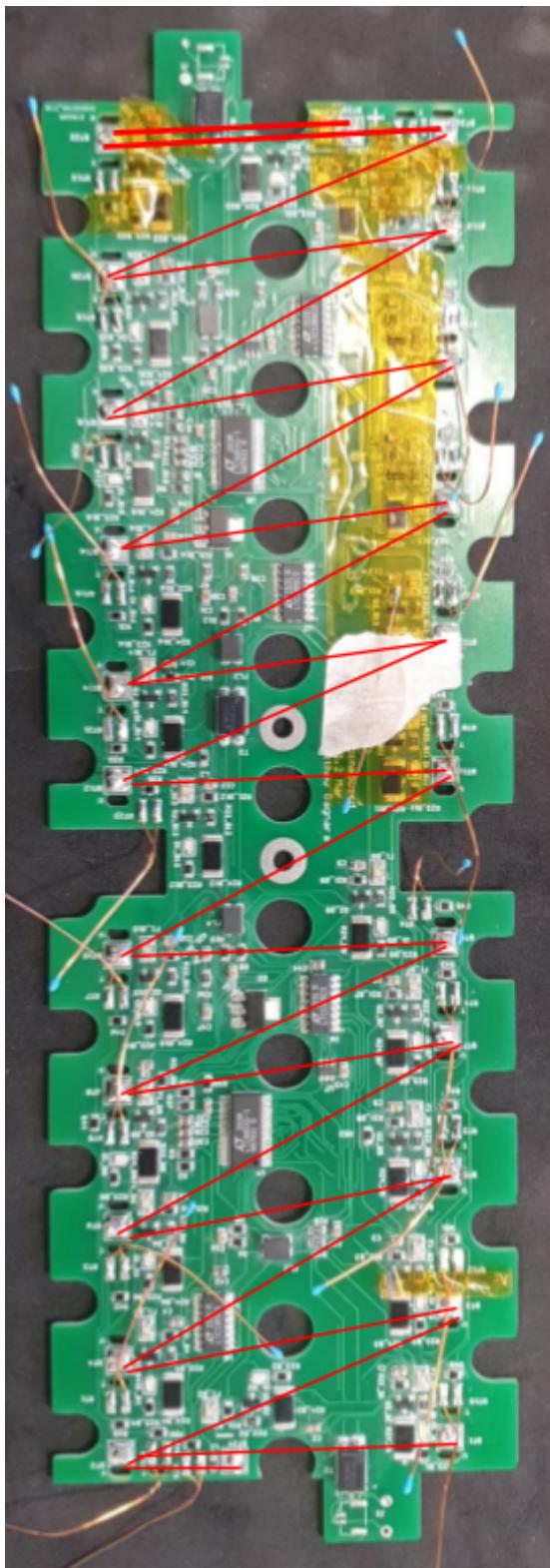


Figure 3: Picture of full rev2 unmirrored spineboard with cell connection order denoted by the red lines with the most positive cell at the top

INSPECTION

Inspection List

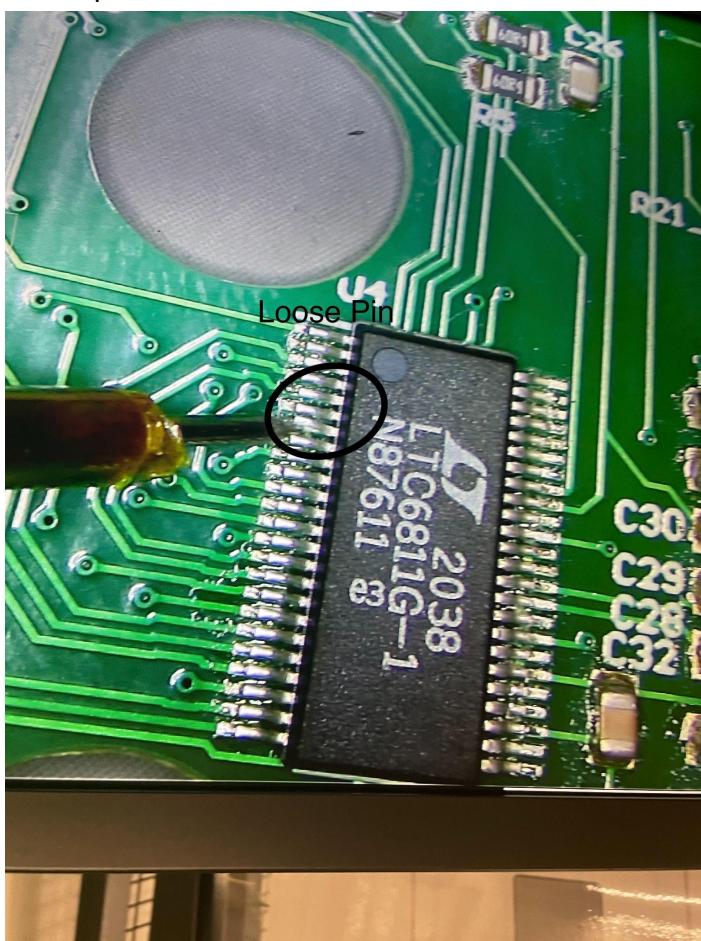
Tools needed

Danger probes

LTC checks

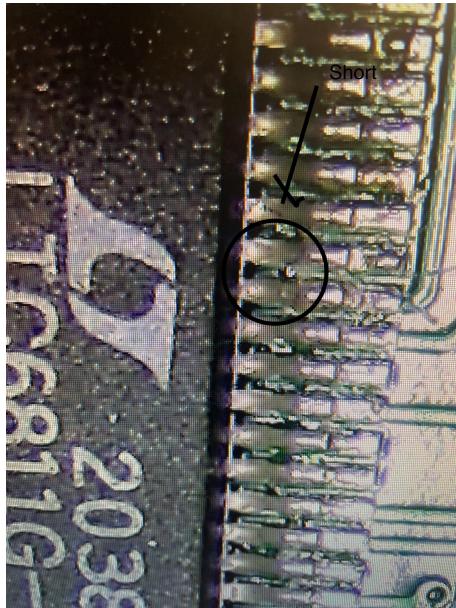
- Check if pads are soldered properly by wiggling it (U4)

Notes: pin 6 was loose



- Check if there are any shorts between the LTC pins (there are 2 pairs of pins that are meant to be shorted) (U4)

Notes: pin 42-41



Notes : pin 47-48 (the transformer will appear as low - the resistance over this pin should be around 13 ohm (not something like 1 ohms)

- Check if pads are soldered properly by wiggling it (U5)
 - Check if there are any shorts between the LTC pins (there are 2 pairs of pins that are meant to be shorted) (U5)
- Notes: Careful not to bump ground pin (will cause a short)

MUX checks

- Check if pins are soldered properly by wiggling it (U2)
- Check if there are any shorts between the MUX pins (U2)
- Check if pins are soldered properly by wiggling it (U1)
- Check if there are any shorts between the MUX pins (U1)
- Check if pins are soldered properly by wiggling it (U6)
- Check if there are any shorts between the MUX pins (U6)
- Check if pins are soldered properly by wiggling it (U8)
- Check if there are any shorts between the MUX pins (U8)

Op Amps checks

- Check if pins are soldered properly by wiggling it (U3)
- Check if there are any shorts between the Op amp pins (U3)
- Check if pins are soldered properly by wiggling it (U7)
- Check if there are any shorts between the Op amp pins (U7)

NPN transistors checks

- ~~Check if pads are on properly by wiggling it (Q3)~~
- ~~Check if there are any shorts between the NPN transistors pins (Q3)~~
- ~~Check if pads are on properly by wiggling it (Q1)~~
- ~~Check if there are any shorts between the NPN transistors pins (Q1)~~

MOSFET Transistors checks

- ~~Check if pads are on properly by wiggling it~~
- ~~Check if the pads and transistors pins are continuous~~
- ~~Check if there are any shorts between the NPN transistors pins~~

LED Diode

- ~~Inspect the direction of the LEDs~~

Check 5V circuitry

- ~~Use a multimeter to probe C29 to BT24 (should be high resistance in the Mega Ohms)~~
- ~~Use a multimeter to probe C to BT24 (should be high resistance in the mega Ohms)~~

Bench Testing

Bench Testing with two 25V supply

Test 1: LTC/Masterboard Communication Test (Rev2)			
Date Started	8-02-22	Date Finished	29-07-21
Author(s)	Akheel, Harj		

Aim(s)

- Test whether the spineboard can communicate with the masterboard.
- Check that LTC6811-1 chips are working (not dead, shorted, etc.)

Hypothesis

Should be able to return total voltage across each LTC6811-1 chip.

Procedure

Initial Setup

1. Solder wires to voltage tap pads BT23, BT12 and BT24
2. Solder wires with JST to through hole pads at T2 end of board
3. Plug teensey on masterboard into laptop using microusb cable
4. Connect assembled spineboard to M19E masterboard
5. Setup software on masterboard (Git hash: 361d7c)
6. Attach the positive of the first power supply to BT23, the negative of the first power supply to BT12, the positive of the second power supply to BT12 and the negative of the second power supply to BT24(between 20V and 30V for each power supply. 300mA current limit). There is some more context for this provided in the definitions section.

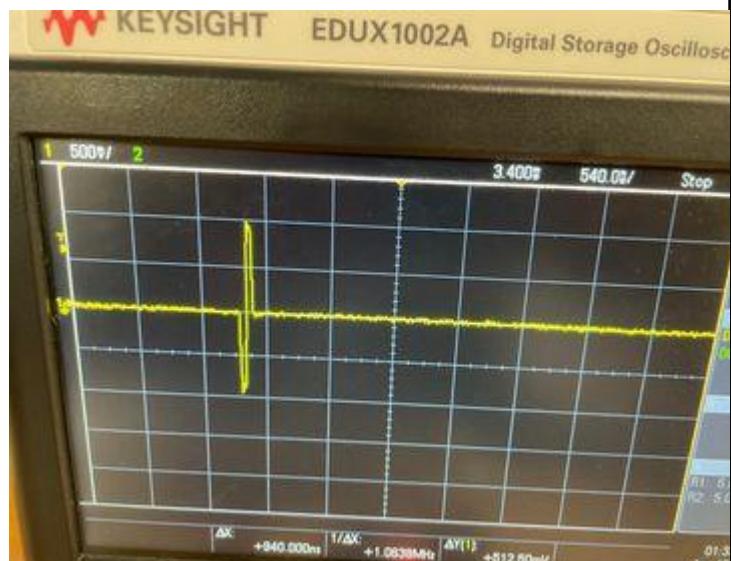
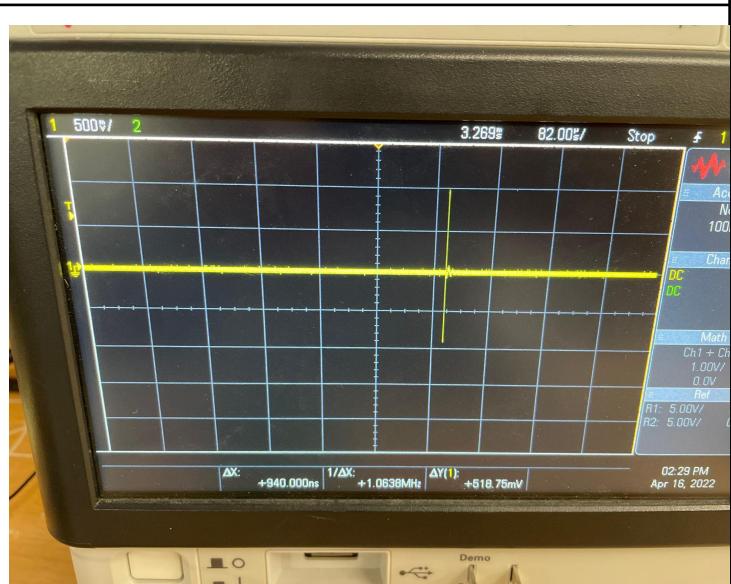
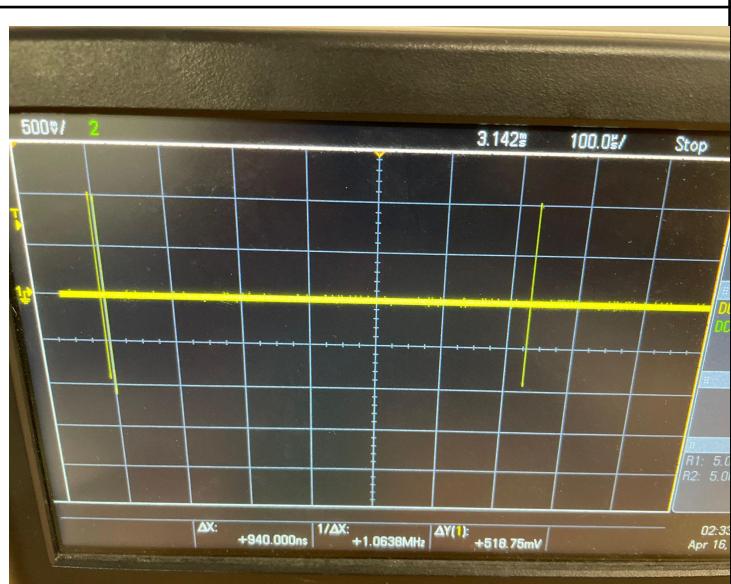
Sub-Test A

7. Write m then 10 to the console to tell the masterboard to request info from the LTC6811-1

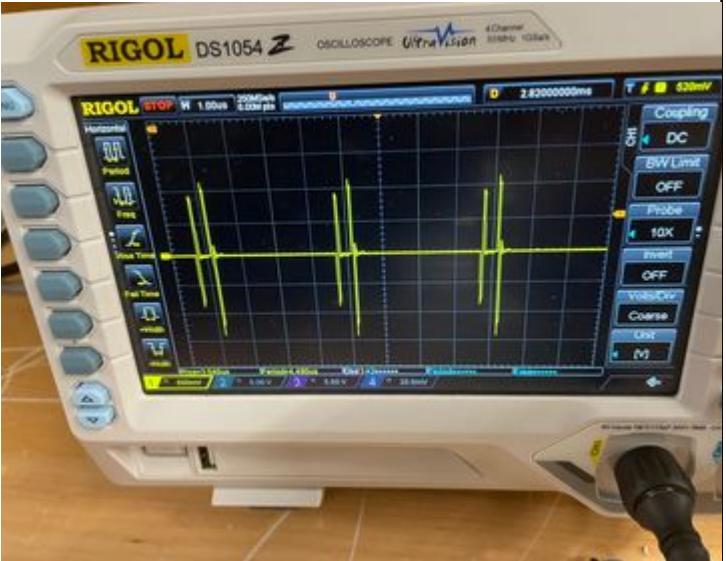
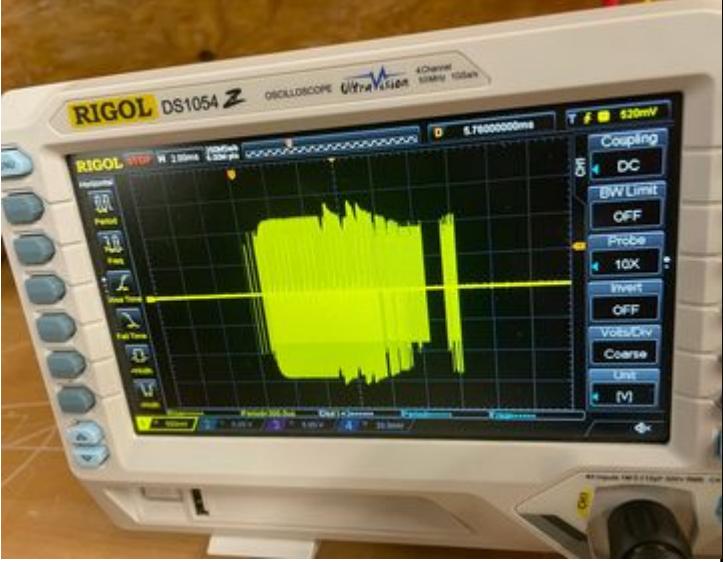
Testing Notes

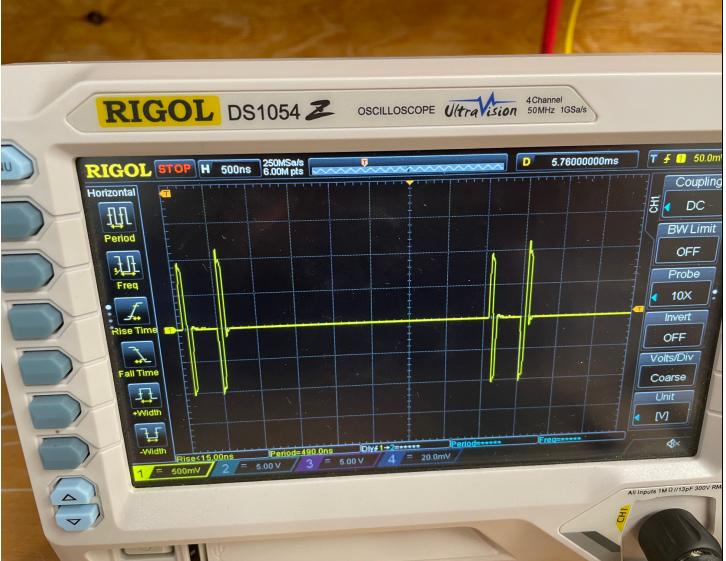
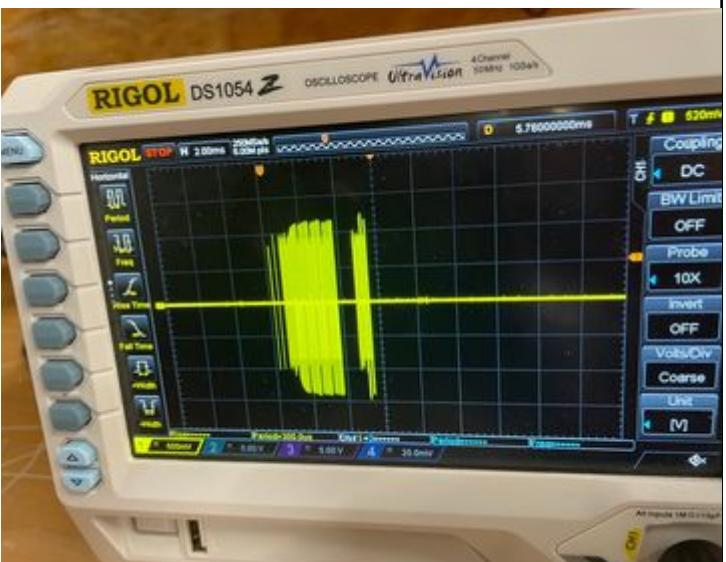
This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
(H+A)S	Soldered wires onto the board Connected positive to BT23,negative to BT24, ground to BT12. Checking voltages resulted in a PEC Error	<pre>bns - menu> 10 Conversion completed in:0.0ms IC 1: C1:6.5535, C2:6.5535, C3:6.5535, C4:6.5535, C5:6.5535, C6:6.5535, C7:6.5535, C8:6.5535, C9:6.5535, C10:6.5535, C11:6.5535 IC 2: C1:6.5535, C2:6.5535, C3:6.5535, C4:6.5535, C5:6.5535, C6:6.5535, C7:6.5535, C8:6.5535, C9:6.5535, C10:6.5535, C11:6.5535 A PEC error was detected in the received data IC 1= 0005101.07000, IC 2= 0005101.07000,</pre>
	Probed T2 input	

		
	Probed T3 input	
	T3 OUTPUT	

	FL2 U4 SIDE	
	FL2 Transformer Side	
	Probed r29 and r6	190 ohms -> should be 50 ohms We think that this might be a common mode choke issue
	While trying to take off FL2 two of the pads came off	We think we should be able to wire the missing pad, as one of the two is still routed but hanging.
	Probed c30	There is charging 5V

	Check the SPI lines	SPI Lines were flipped
	Not getting consistent readings	<pre>bms - menu> 10 Conversion completed in:1.8ms IC 1: C1:1.3904, C2:1.3466, C3:1.6488, C4:2.1747, C5:0.8473, C6:5.2460, C7:6.5535 IC 2: C1:0.0000, C2:0.0025, C3:0.0033, C4:0.0000, C5:0.0594, C6:0.5188, C7:6.5535 A PEC error was detected in the received data IC 1: SOC:131.0700, IC 2: SOC:131.0700. bms - menu> 10 Conversion completed in:2.1ms IC 1: C1:1.4545, C2:6.5343, C3:6.5535, C4:6.5535, C5:6.5535, C6:6.5535, C7:6.5535 IC 2: C1:0.0000, C2:0.0024, C3:0.0035, C4:6.5535, C5:6.5535, C6:6.5535, C7:6.5535 IC 1: SOC:25.0360, IC 2: SOC:15.6340,</pre>
	Probing when working (semi working)	 

	Probing when not working	 
	Both sides of FL2 are 180 ohms	
	Checked the Drive Pin	<p>Drive Pin U4 is around 6.2V Drive pin U5 is around 5.7V The datasheet specifies that it should be 5.7V</p>
	Chekking the resistance between ground of LTC and the ground of the Power Supply	<p>We chose to probe this resistance because the drive pin on the npn was at ~6.2V. This means that there would have been an extra voltage drop from another resistance where there shouldn't have been. When probing between the LTC ground and the ground tap we measured a resistance of ~7MOhms. There should be a short between these two nodes through the ferrite bead. The ferrite bead footprint was unpopulated and the ~7MOhms was from external circuitry.</p>

Results

Sub-Test A

Images	Notes

Bottom Line

Impact on Future Testing

- Testing of the rest of the board functionality can go ahead

Impact on Future Design Iteration

- None

Test 2: Simulate Assembly Test			
Date Started	8-02-22	Date Finished	29-07-21
Author(s)			

Aim(s)

- To simulate assembling spine board on cells

Hypothesis

Should theoretically be fine as it is proven on the mirrored boards, however there are issues to balancing circuitry lighting up during assembly.

Procedure

Initial Setup

1. Solder single core wires to all voltage taps
2. Set up a 23 resistor voltage divider network with 1k resistors on a breadboard
3. Connect tap wires from bt24 to bt23 in that order one by one with the power supply on
4. Connect the 2 power supplies (most positive of the first supply to tap 23, the negative to tap 12 negative to tap 24)
5. **Connection to masterboard is connected to T2 end of board**
6. Setup software on masterboard (Git hash: 361d7c)

Sub-Test A

8. Write m then 10 to the console to tell the masterboard to request info from the LTC6811-1

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		-

Results

- When Assembling no known issues popped up

Sub-Test A

Images	Notes

Bottom Line

Impact on Future Testing

- Testing of the rest of the board functionality can go ahead

Impact on Future

Test 2: Voltage Reading test			
Date Started	XX-X-XXXX	Date Finished	XX-XX-XXXX
Author(s)			

Aim(s)

- Test whether the masterboard can get voltage readings from the spineboard
- Test if the voltage readings are accurate

Hypothesis

There were no issues that came up when testing the voltage readings on the rev2 board 2, so none are expected here. As such, it is expected that the LTC6811-1 chips will return the correct voltage readings. We need to get around 2V on console

Procedure

Initial Setup

7. Solder single core wires to all voltage taps
8. Set up a 23 resistor voltage divider network with 1k resistors on a breadboard
9. Connect tap wires to resistors in appropriate order (tap 23 to most positive, tap 22 to second most positive, etc. only exception is tap 24 should be connected to the most negative)
10. Connect the 2 power supplies (most positive to tap 23, the mid point should be connected to tap 12, most negative to tap 24)
- 11. Connection to masterboard is connected to T2 end of board**
12. Setup software on masterboard (Git hash: 361d7c)

--	--

Figure 3: Picture of setup for voltage sensing and temperature sensing

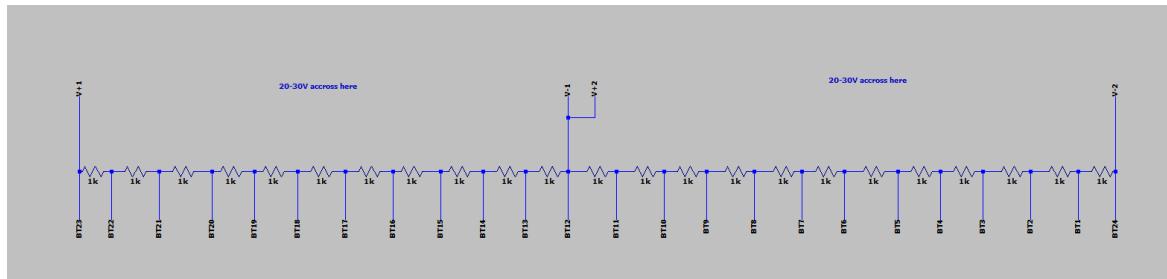


Figure 4: Schematic for testing voltage readings - larger version on drive (link below)
<https://drive.google.com/file/d/1K5q2yD45PjHS5yqdb3-MyiLbu6IKIB/view?usp=sharing>

13. Write m then select the appropriate option from the menu to tell the masterboard to request voltages from the LTC6811-1 (list of all options will be displayed on screen when m is entered)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
Akheel	<pre>ons - menu> 10 Conversion completed in:2.1ms IC 1: C1:6.5535, C2:6.5535, C3:6.5535, C4:6.5535, C5:6.5535, IC 2: C1:2.0573, C2:2.1020, C3:2.0732, C4:2.0507, C5:2.0837, A PEC error was detected in the received data IC 1: SOC:131.0700, IC 2: SOC:24.9660,</pre>	Remember to connect power supply
	<pre>ons - menu> 31 Conversion completed in:2.1ms 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F</pre>	

Results

It WORKS!!!!!!

Images	Notes

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration

Test 3: Temperature reading test			
Date Started	12-2-2022	Date Finished	12-2-2022
Author(s)	Akheel, Matt		

Aim(s)

- Test that the temperature sensing works

Hypothesis

There were no issues with the unmirrored rev 2 board 1 so it is expected that the spineboard should return the correct temperature readings

Procedure

Initial Setup

1. Solder wires to BT23, BT12 and BT24 (here we've soldered wires to all the voltage taps as we were testing voltage readings at the same time but that isn't necessary to test temperature readings. If the tester wants to validate both at the same time, please refer to voltage readings test initial setup)
2. Connect power supply to 1 to BT23 (positive) and BT12 (ground) and power supply 2 to BT12 (positive) and BT24 (ground)
3. Solder thermistors to all the temperature taps
4. Connect masterboard to spineboard (connect to T2 end of board, solder wires to through holes with JST crimped to end if required)
5. Setup software on masterboard (Git hash: 361d7c)

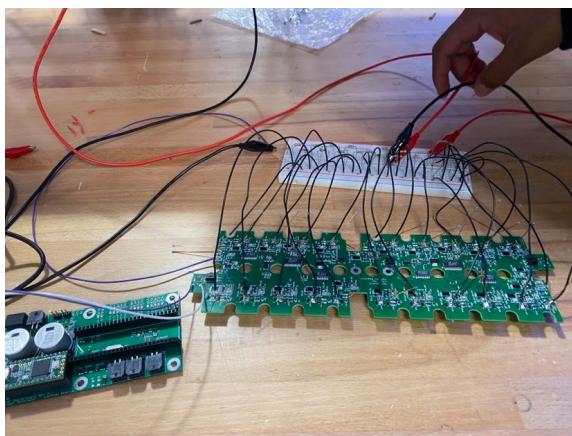


Figure 7: Picture of setup for voltage and temperature testing

Sub-Test A

6. Write m to console and tell it to measure temperatures (list of options will be displayed after entering m)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		•

Results

Temp sensing is working. We checked by heating individual thermistors with our hands, and measuring it with the insulation tester, to check that the temps were correct when not ambient. We did this for two sensors from each IC, where IC1 has temps from RT23 (IC1 sensor 1) to RT12 (IC1 sensor 12?) and IC2 has temps from RT1 (IC2 sensor 1) to RT11 (IC2 sensor 12?).

Images	Notes
	<ul style="list-style-type: none">Initial voltage readings before the temperature check

```
bms - menu> 32
IC 1 Sensor 1 : 1.5842V, 2.2515C
IC 2 Sensor 1 : 1.5897V, 2.2354C

IC 1 Sensor 2 : 1.5790V, 2.2668C
IC 2 Sensor 2 : 1.6008V, 2.2029C

IC 1 Sensor 3 : 1.6031V, 2.1962C
IC 2 Sensor 3 : 1.6009V, 2.2026C

IC 1 Sensor 4 : 1.5744V, 2.2803C
IC 2 Sensor 4 : 1.5903V, 2.2337C

IC 1 Sensor 5 : 1.5938V, 2.2234C
IC 2 Sensor 5 : 1.5817V, 2.2589C

IC 1 Sensor 6 : 1.6052V, 2.1900C
IC 2 Sensor 6 : 1.6033V, 2.1956C

IC 1 Sensor 7 : 1.5801V, 2.2636C
IC 2 Sensor 7 : 1.5984V, 2.2099C

IC 1 Sensor 8 : 1.6012V, 2.2017C
IC 2 Sensor 8 : 1.5804V, 2.2627C

IC 1 Sensor 9 : 1.5931V, 2.2255C
IC 2 Sensor 9 : 1.5839V, 2.2524C

IC 1 Sensor 10 : 1.6054V, 2.1894C
IC 2 Sensor 10 : 1.5999V, 2.2055C

IC 1 Sensor 11 : 1.5807V, 2.2618C
IC 2 Sensor 11 : 1.5923V, 2.2278C

IC 1 Sensor 12 : 1.0303V, 4.0180C
IC 2 Sensor 12 : 1.5841V, 2.2518C
```

- First call to temperatures

```
bms - Menu> 32
IC 1 Sensor 1 : 1.2796V, 3.1747C
IC 2 Sensor 1 : 1.5837V, 2.2530C

IC 1 Sensor 2 : 1.5773V, 2.2718C
IC 2 Sensor 2 : 1.5862V, 2.2457C

IC 1 Sensor 3 : 1.5923V, 2.2278C
IC 2 Sensor 3 : 1.5875V, 2.2419C

IC 1 Sensor 4 : 1.5722V, 2.2867C
IC 2 Sensor 4 : 1.5847V, 2.2501C

IC 1 Sensor 5 : 1.5922V, 2.2281C
IC 2 Sensor 5 : 1.5768V, 2.2732C

IC 1 Sensor 6 : 1.5936V, 2.2240C
IC 2 Sensor 6 : 1.5912V, 2.2310C

IC 1 Sensor 7 : 1.5877V, 2.2413C
IC 2 Sensor 7 : 1.5536V, 2.3414C

IC 1 Sensor 8 : 1.5904V, 2.2334C
IC 2 Sensor 8 : 1.5781V, 2.2694C

IC 1 Sensor 9 : 1.5966V, 2.2152C
IC 2 Sensor 9 : 1.5780V, 2.2697C

IC 1 Sensor 10 : 1.5946V, 2.2211C
IC 2 Sensor 10 : 1.5855V, 2.2477C

IC 1 Sensor 11 : 1.5783V, 2.2688C
IC 2 Sensor 11 : 1.5855V, 2.2477C

IC 1 Sensor 12 : 1.2451V, 3.2851C
IC 2 Sensor 12 : 1.5784V, 2.2685C
```

- Second call while holding thermistor RT23

Bottom Line

Impact on Future Testing

- Temperature readings appear to work so we can continue with the rest of the tests, however the code may need changing to eliminate linearity errors

Impact on Future Design Iteration

Test 4: Cell balancing			
Date Started	12-2-2022	Date Finished	YYYY-MM-DD
Author(s)			

Aim(s)

- Test that the cell balancing circuit works

Hypothesis

The cell balancing was proven to work in the revision 2 unmirrored board 1 without any issues. As such, it is expected that the balancing circuitry will work and the balancing LEDs will turn on when the specific cell is balanced.

Procedure

Initial Setup

1. Set up according to test 2 (voltage readings)
2. Place 3rd power supply across an individual resistor (the one you want to balance for, starting at 23) and set the power supply to 3.7V (nominal cell voltage) - this is to ensure that the voltage across that resistor is a constant voltage which wouldn't be the case if you just connected a power supply to each end.

Figure 10: Picture of setup for cell balancing

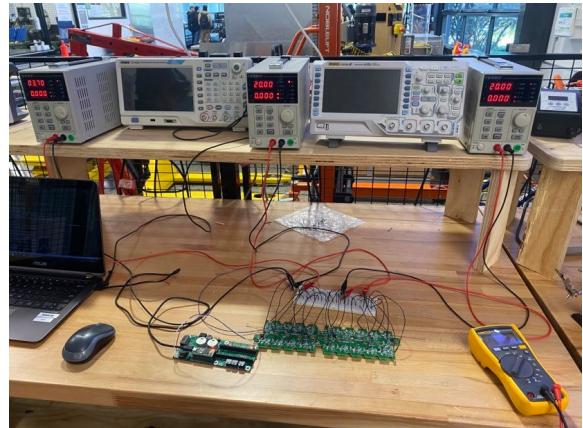


Figure 11: Picture of testing setup with power supplies for cell balancing

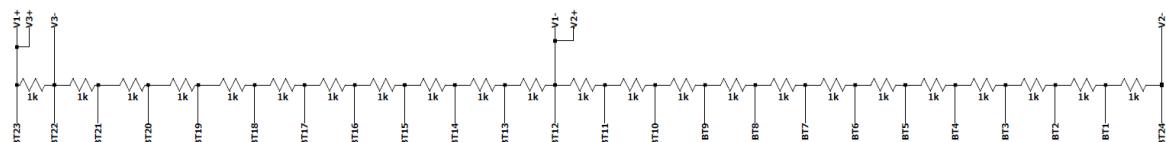


Figure 12: schematic of testing setup for cell balancing. The voltage of power supplies 1 and 2 (denoted by V1 and V2 respectively) should be between 20V and 30V. The voltage across power

supply 3 (denoted by V3)+ should be between 3.7V and 4.2V

Sub-Test A

3. Write 23 to console then enter the s pin you want to enable balancing on (i.e. if you want to balance between cell 12 and 11, enable the 12 s pin. It will enable that s pin on both LTCs, so enter a number between 1 and 12)
4. Confirm that the LED turns on for the target balancing circuit
5. Write 24 to the console to clear the balancing
6. Move the power supply to be across the next resistor
7. Repeat steps 20 to 23 until all balancing circuits have been validated

Sub-Test B

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
	Checked Gating signal	Around - 2.5V
	Check Voltage drop over r24	Around 2.0V
	The diode not soldered on properly (d1_B14)	
	Transistor not on properly	

Results

S pin no.	IC1 LED	IC2 LED
1	<input checked="" type="checkbox"/> BT13 enabled & disabled	<input checked="" type="checkbox"/> BT1 enabled & disabled
2	<input checked="" type="checkbox"/> BT14 enabled & disabled	<input checked="" type="checkbox"/> BT2 enabled & disabled
3	<input checked="" type="checkbox"/> BT15 enabled & disabled	<input checked="" type="checkbox"/> BT3 enabled & disabled
4	<input checked="" type="checkbox"/> BT16 enabled & disabled	<input checked="" type="checkbox"/> BT4 enabled & disabled
5	<input checked="" type="checkbox"/> BT17 enabled & disabled	<input checked="" type="checkbox"/> BT5 enabled & disabled

6	<input checked="" type="checkbox"/> BT18 enabled & disabled	<input checked="" type="checkbox"/> BT6 enabled & disabled
7	<input checked="" type="checkbox"/> BT19 enabled & disabled	<input checked="" type="checkbox"/> BT7 enabled & disabled
8	<input checked="" type="checkbox"/> BT20 enabled & disabled	<input checked="" type="checkbox"/> BT8 enabled & disabled
9	<input checked="" type="checkbox"/> BT21 enabled & disabled	<input checked="" type="checkbox"/> BT9 enabled & disabled
10	<input checked="" type="checkbox"/> BT22 enabled & disabled	<input checked="" type="checkbox"/> BT10 enabled & disabled
11	<input checked="" type="checkbox"/> BT23 enabled & disabled	<input checked="" type="checkbox"/> BT11 enabled & disabled
12	NA	<input checked="" type="checkbox"/> BT12 enabled & disabled

Images	Notes

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration

Bench Testing with 50V over U4 (optional)

Test 1: LTC/Masterboard Communication Test (Rev2)			
Date Started	8-02-22	Date Finished	29-07-21
Author(s)	Akheel, Ananya		

Aim(s)

- Test whether the spineboard can communicate with the masterboard.
- Check that LTC6811-1 chips are working (not dead, shorted, etc.)

Hypothesis

Should be able to return total voltage across each LTC6811-1 chip.

Procedure

Initial Setup

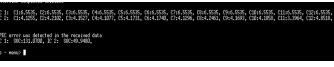
9. Solder wires to voltage tap pads BT12 and BT24
10. Solder wires with JST to through hole pads at T2 end of board
11. Plug teensey on masterboard into laptop using microusb cable
12. Connect assembled spineboard to M19E masterboard
13. Setup software on masterboard (Git hash: 361d7c)
14. Attach the positive of the first power supply to BT12, the negative of the first power supply to the positive of the second power supply and the negative of the second power supply to BT24 (between 25V and 25V for each power supply. 300mA current limit). There is some more context for this provided in the definitions section.

Sub-Test A

15. Write m then 10 to the console to tell the masterboard to request info from the LTC6811-1

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		-

Results

Sub-Test A

Images	Notes

Bottom Line

Impact on Future Testing

- Testing of the rest of the board functionality can go ahead

Impact on Future

Test 2: Simulate Assembly Test			
Date Started	8-02-22	Date Finished	29-07-21
Author(s)			

Aim(s)

- To simulate assembling spine board on cells

Hypothesis

Should theoretically be fine as it is proven on the mirrored boards, however there are issues to balancing circuitry lighting up during assembly.

Procedure

Initial Setup

14. Solder single core wires to all voltage taps
15. Set up a 23 resistor voltage divider network with 1k resistors on a breadboard
16. Connect tap wires from bt24 to bt12 in that order
17. Connect the 1 power supplies (most positive to tap 12, the mid point should be connected to most negative to tap 24)
- 18. Connection to masterboard is connected to T2 end of board**
19. Setup software on masterboard (Git hash: 361d7c)

Sub-Test A

16. Write m then 10 to the console to tell the masterboard to request info from the LTC6811-1

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
	BT11 wire came off after it was properly assembled	<ul style="list-style-type: none"> - This caused R36 to disconnect - There was smoke from the resistor - And the LTC heated up <p>R36 is connected to the npn transistor as the current limiting resistor. This component came off</p>

		
		5V to ground 17.9 ohms
		Bt11 fuse is fined
Removed op amp		1.227k ohms is resistance from 5V to ground
Dead op amp		5v to ground - 18 ohm (this is testing the op amp off the board)
Good op amp		5V to ground - high impedance (this is testing the op amp off the board)
Replaced Op amp		Resistance is 1.227kohms
Removed muxes		Resistastance was 1.7k ohm supposed to be 7.9 Mega Ohms (when compared to the other chip on the other side
Removed NPN		Still 2.3kOhms
Removed r37		It became 4.7kOhms So found that LTC is shorting to gether
Removed LTC		In the Mega ohms

Results

Sub-Test A

Images	Notes

Bottom Line

Impact on Future Testing

- Testing of the rest of the board functionality can go ahead

Impact on Future

Test 3: Voltage Reading test			
Date Started	XX-X-XXXX	Date Finished	XX-XX-XXXX
Author(s)			

Aim(s)

- Test whether the masterboard can get voltage readings from the spineboard
- Test if the voltage readings are accurate

Hypothesis

There were no issues that came up when testing the voltage readings on the rev2 board 2, so none are expected here. As such, it is expected that the LTC6811-1 chips will return the correct voltage readings. We need to get around 4V on console

Procedure

Initial Setup

20. Solder single core wires to all voltage taps
21. Set up a 23 resistor voltage divider network with 1k resistors on a breadboard
22. Connect tap wires to resistors in appropriate order (tap 23 to most positive, tap 22 to second most positive, etc. only exception is tap 24 should be connected to the most negative)
23. Connect the 2 power supplies (most positive to tap 23, the mid point should be connected to tap 12, most negative to tap 24)
- 24. Connection to masterboard is connected to T2 end of board**
25. Setup software on masterboard (Git hash: 361d7c)

Figure 3: Picture of setup for voltage sensing and temperature sensing

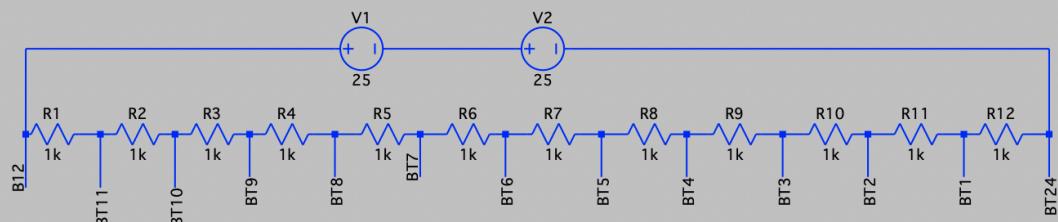


Figure 4: Schematic for testing voltage readings - larger version on drive (link below)
<https://drive.google.com/file/d/1K5g2yD45PJchS5yqdb3-MyIbu6IKIB/view?usp=sharing>

26. Write m then select the appropriate option from the menu to tell the masterboard to request voltages from the LTC6811-1 (list of all options will be displayed on screen when m is entered)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		

Results

Images	Notes

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration

Test 4: Temperature reading test			
Date Started	12-2-2022	Date Finished	12-2-2022
Author(s)	Akheel, Matt		

Aim(s)

- Investigate the how the temperature sensing circuit works on voltages similar to the cell voltage

Hypothesis

- Due to the fact that op amps and multiplexers are not working no

Procedure

Initial Setup

7. Solder wires to BT12 and BT24 (here we've soldered wires to all the voltage taps as we were testing voltage readings at the same time but that isn't necessary to test temperature readings. If the tester wants to validate both at the same time, please refer to voltage readings test initial setup)
8. Connect BT12 (positive) to power supply 1 positive and power supply 1 negative to power supply 2 positive supply and negative of power supply 2 to BT24 (ground)
9. Connect masterboard to spineboard (connect to T2 end of board, solder wires to through holes with JST crimped to end if required)
10. Setup software on masterboard (Git hash: 361d7c)
11. We will be probing all inputs and outputs of the Multiplexor and Op amp

Figure 7: Picture of setup for voltage and temperature testing

Sub-Test A

12. Write m to console and tell it to measure temperatures (list of options will be displayed after entering m)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		•

Results

It should be documenter here

Images	Notes
	<ul style="list-style-type: none"> Initial voltage readings before the temperature check

```
bms - menu> 32
IC 1 Sensor 1 : 6.5535V, 0.0000C
IC 2 Sensor 1 : 1.5801V, 2.2636C

IC 1 Sensor 2 : 6.5535V, 0.0000C
IC 2 Sensor 2 : 1.6082V, 2.1813C

IC 1 Sensor 3 : 6.5535V, 0.0000C
IC 2 Sensor 3 : 1.5935V, 2.2243C

IC 1 Sensor 4 : 6.5535V, 0.0000C
IC 2 Sensor 4 : 1.5970V, 2.2140C

IC 1 Sensor 5 : 6.5535V, 0.0000C
IC 2 Sensor 5 : 1.5674V, 2.3008C

IC 1 Sensor 6 : 6.5535V, 0.0000C
IC 2 Sensor 6 : 1.6113V, 2.1722C

IC 1 Sensor 7 : 6.5535V, 0.0000C
IC 2 Sensor 7 : 1.5948V, 2.2205C

IC 1 Sensor 8 : 6.5535V, 0.0000C
IC 2 Sensor 8 : 1.5808V, 2.2615C

IC 1 Sensor 9 : 6.5535V, 0.0000C
IC 2 Sensor 9 : 1.5922V, 2.2281C

IC 1 Sensor 10 : 6.5535V, 0.0000C
IC 2 Sensor 10 : 1.5876V, 2.2416C

IC 1 Sensor 11 : 6.5535V, 0.0000C
IC 2 Sensor 11 : 1.5850V, 2.2492C

IC 1 Sensor 12 : 6.5535V, 0.0000C
IC 2 Sensor 12 : 1.5844V, 2.2509C
```

- First call to temperatures

Probed drive pin

5.7V (as expected)

Test 5: Cell balancing			
Date Started	12-2-2022	Date Finished	YYYY-MM-DD
Author(s)			

Aim(s)

- Test that the cell balancing circuit works

Hypothesis

Should work the same as with 25 v supply over each LTC chip since there have not been any issues with spineboard on the segment.

Procedure

Initial Setup

8. Set up according to test 2 (voltage readings)
9. Place 3rd power supply across an individual resistor (the one you want to balance for, starting at 23) and set the power supply to 3.7V (nominal cell voltage) - this is to ensure that the voltage across that resistor is a constant voltage which wouldn't be the case if you just connected a power supply to each end.

Figure 10: Picture of setup for cell balancing	Figure 11: Picture of testing setup with power supplies for cell balancing

Figure 12: schematic of testing setup for cell balancing. The voltage of power supplies 1 and 2 (denoted by V1 and V2 respectively) should be between 20V and 30V. The voltage across power supply 3 (denoted by V3)+ should be between 3.7V and 4.2V

Sub-Test A

10. Write 23 to console then enter the s pin you want to enable balancing on (i.e. if you want to balance between cell 12 and 11, enable the 12 s pin. It will enable that s pin on both LTCs, so enter a number between 1 and 12)
11. Confirm that the LED turns on for the target balancing circuit
12. Write 24 to the console to clear the balancing
13. Move the power supply to be across the next resistor
14. Repeat steps 20 to 23 until all balancing circuits have been validated

Sub-Test B

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
	BT11 wire came off after it was properly assembled	<ul style="list-style-type: none"> - This caused R36 to disconnect - There was smoke from the resistor - And the LTC heated up <p>R36 is connected to the npn transistor as the current limiting resistor. This component came off</p>
		C30 - to ground 17.9 ohms
		Bt11 fuse is fined
	Removed op amp	1.227k ohms is resistance from 5V to ground
	Dead op amp	5v to ground - 18 ohm
	Good op amp	5V to ground - high impedance
	Replaced Op amp	Resistance is 1.227kohms
	Removed muxes	Resistastance was 1.7k ohm supposed to be 7.9 Mega Ohms (when compared to the other chip on the other side)
	Removed NPN	Still 2.3kOhms

Results

S pin no.	IC2 LED
1	BT1 enabled & disabled
2	BT2 enabled & disabled
3	BT3 enabled & disabled
4	BT4 enabled & disabled
5	BT5 enabled & disabled
6	BT6 enabled & disabled
7	BT7 enabled & disabled
8	BT8 enabled & disabled
9	BT9 enabled & disabled
10	BT10 enabled & disabled

11	BT11 enabled & disabled
12	BT12 enabled & disabled

Images	Notes

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration

Testing on M19E Cells

Test 1: Cell balancing			
Date Started	12-2-2022	Date Finished	YYYY-MM-DD
Author(s)			

Aim(s)

- Test that the cell balancing circuit works with actual cells

Hypothesis

Testing

Procedure

Initial Setup

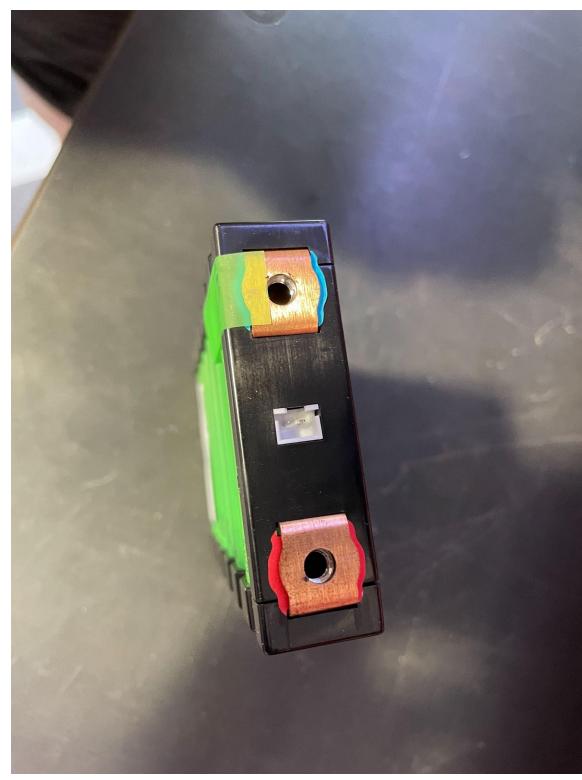
- Set up 12 blocks M19E cells
- Solder ring terminal wire to voltage taps
- Bolt ring terminal to the cell
- According schematic diagram 1 or 2

Schematic 1 (over the U4 IC)	
Schematic 2 (Over the U5 IC) Minimum rating of LTC to be powered is 11V	

M19E Cells (1s5p)



Attach ring terminal from wires
(red positive and blue/green negative)



Sub-Test A

Write 23 to console then enter the s pin you want to enable balancing on (i.e. if you want to balance between cell 12 and 11, enable the 12 s pin. It will enable that s pin on both LTCs, so enter a number between 1 and 12)

15. Confirm that the LED turns on for the target balancing circuit

16. Write 24 to the console to clear the balancing

- 17.Move the power supply to be across the next resistor
- 18.Repeat steps 20 to 23 until all balancing circuits have been validated

Sub-Test B

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes

Results

S pin no.	IC1 LED	IC2 LED
1	BT13 enabled & disabled	BT1 enabled & disabled
2	BT14 enabled & disabled	BT2 enabled & disabled
3	BT15 enabled & disabled	BT3 enabled & disabled
4	BT16 enabled & disabled	BT4 enabled & disabled
5	BT17 enabled & disabled	BT5 enabled & disabled
6	BT18 enabled & disabled	BT6 enabled & disabled
7	BT19 enabled & disabled	BT7 enabled & disabled
8	BT20 enabled & disabled	BT8 enabled & disabled
9	BT21 enabled & disabled	BT9 enabled & disabled
10	BT22 enabled & disabled	BT10 enabled & disabled
11	BT23 enabled & disabled	BT11 enabled & disabled
12	NA	BT12 enabled & disabled

Images	Notes

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration

M21 Segment Testing

Test 1: Voltage reading test			
Date Started	13/04/22	Date Finished	YYYY-MM-DD
Author(s)	Locky, Ananya		

Aim(s)

- Test whether the masterboard can get voltage readings from the spineboard
-

Hypothesis

No issues came up when bench testing the board so it is expected to all work correctly and return the correct voltage across each cell.

Procedure

Initial Setup

1. Set up spineboard and segment according to the segment assembly guide
2. **Connection to masterboard is connected to T2 end of board**
3. Setup software on masterboard (Git hash: 361d7c)

Figure 3: Picture of setup for voltage sensing and temperature sensing	
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Figure 4: Schematic for testing voltage readings - larger version on drive (link below) https://drive.google.com/file/d/1K5g2yD45PJcHS5yqdb3-MyiLbu6lIKIB/view?usp=sharing
--

4. Write m then select the appropriate option (10) from the menu to tell the masterboard to request voltages from the LTC6811-1 (list of all options will be displayed on screen when m is entered)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		○

Results

Getting the voltage readings we expect

Images	Notes
	•

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration

Test 2: Temperature reading test			
Date Started		Date Finished	YYYY-MM-DD
Author(s)			

Aim(s)

- Test that the temperature sensing works

Hypothesis

There were no issues with the unmirrored rev 2 board 1 so it is expected that the spineboard should return the correct temperature readings

Procedure

Initial Setup

1. Set up segment according to the segment assembly guideline
2. Connect masterboard to spineboard (connect to T2 end of board, solder wires to through holes with JST crimped to end if required)
3. Setup software on masterboard (Git hash: 361d7c)

Figure 7: Picture of setup for voltage and temperature testing

Sub-Test A

4. Write m to console and tell it to measure temperatures (32) (list of options will be displayed after entering m)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		○
-		-

Results

Temp sensing is working, although the voltage to temperatures conversion might need reconfiguring

Images	Notes
	-

Test 3: Loaded Segment Test			
Date Started		Date Finished	YYYY-MM-DD
Author(s)			

Aim(s)

Test functionality of the segment under load. The segment voltages should sag when the load is turned on and then return to normal when the load is turned off.

Hypothesis

Procedure

Initial Setup

1. Set up segment according to the segment assembly guideline
2. Connect masterboard to spineboard (connect to T2 end of board, solder wires to through holes with JST crimped to end if required)
3. Setup software on masterboard (Git hash: 361d7c)

Figure 7: Picture of setup for voltage and temperature testing

Sub-Test A

4. Write m to console and tell it to measure temperatures (32) (list of options will be displayed after entering m)

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes
		○
-		-

Results

Images	Notes
	-

Test 4: Cell balancing			
Date Started	29-4-2021	Date Finished	YYYY-MM-DD
Author(s)	Raquib, Matt		

Aim(s)

- Test that the cell balancing circuitry works

Hypothesis

The cell balancing was proven to work in the revision 2 unmirrored board 1 without any issues. As such, it is expected that the balancing circuitry will work and the balancing LEDs will turn on when the specific cell is balanced.

Procedure

Initial Setup

1. Set up spineboard and segment according to the segment assembly guide
2. **Connection to masterboard is connected to T2 end of board**
3. Setup software on masterboard (Git hash: 361d7c)

Figure 10: Picture of setup for cell balancing	Figure 11: Picture of testing setup with power supplies for cell balancing

Sub-Test A

4. Write 23 to console then enter the s pin you want to enable balancing on (i.e. if you want to balance between cell 12 and 11, enable the 12 s pin. It will enable that s pin on both LTCs, so enter a number between 1 and 12)
5. Confirm that the LED turns on for the target balancing circuit
6. Write 24 to the console to clear the balancing
7. Repeat steps 4 to 6 until all balancing circuits have been validated

Sub-Test B

Testing Notes

This section is for notes taken during testing if things don't go as planned, or debugging is required.

Person	Suggestion / Question / Steps Taken	Notes

Results

Cell balancing circuit works

Images	Notes

Bottom Line

Impact on Future Testing

Impact on Future Design Iteration