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METHODOLOGY TO OPTIMIZE THE LOW-DROPOUT
REGULATOR (LDO)

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Abstract

In today's increasingly powerful and complex devices, integrated circuits (ICs) play a pivotal role in supporting a growing array of functionalities. Ensuring the critical functions of these ICs requires stable voltage supplies, alongside energy-efficient strategies to prolong battery life and minimize energy wastage. Consequently, various specialized regulators are employed to provide different voltage levels to multiple parts of ICs. Low-Dropout voltage regulators (LDOs) are key to these supply solutions. Given their frequent use across different design projects, semiconductor technologies, and individual chips, the design of LDOs demands considerable effort.

This thesis focuses on the design and optimization of high-efficiency LDO regulators with low dropout voltage and high power supply rejection ratio (PSRR), implemented in two different technologies 130nm Bipolar-CMOS-DMOS (BCD) technology and 22nm Fully Depleted Silicon On Insulator (FDSOI) technology.

The methodology integrates advanced design automation techniques, utilizing Python-based scripts to initially calculate the widths and lengths ((W/L)) of MOS-FET transistors, bias currents, and compensation values. These initial parameters are then refined using local optimization algorithms in Cadence Virtuoso, ensuring the LDO meets stringent performance criteria.

Key design strategies include the use of a PMOS pass transistor to minimize dropout voltage and a two-stage error amplifier to achieve high DC gain and rail-to-rail output. The frequency compensation is handled through pole-splitting and pole-zero cancellation techniques to maintain stability across varying load conditions.

Simulation results for three different cases demonstrate the effectiveness of the proposed methodology in both 130nm BCD and 22nm FDSOI technologies. Case studies include comprehensive analyses of input-output characteristics, AC analysis for PSRR, and transient response to load variations. Despite challenges such as increased gate capacitance impacting stability and slew rate, the optimized designs show significant improvements in efficiency and performance, validating the design approach across different technology nodes.

This research contributes to the field by providing a structured and automated approach to LDO design, highlighting the balance between theoretical predictions and practical implementations to achieve optimal performance in integrated circuits across multiple technology platforms.

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Abbreviations

CMOS	Complimentary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel Metal Oxide Semiconductor Field Effect Transistor
PMOS	p-channel Metal Oxide Semiconductor Field Effect Transistor
OTA	Operational Transconductance Amplifier
VCCS	Voltage Controlled Current Source
BCD	Bipolar-CMOS-DMOS
CLM	Channel Length Modulation
MHz	Mega-Hertz
LDO	Low Dropout Regulator
PSRR	Power Supply Rejection Ratio
ESR	Equivalent Series Resistance
UGF	Unity Gain Frequency
FDSOI	Fully Depleted Silicon On Insulator
SoC	System on Chip
VDO	Dropout Voltage
Iq	Quiescent Current
Iload	Load Current
W/L	Width over Length Ratio
RESR	Series Resistance of Output Capacitor
kOhm	Kilo Ohms
uV	Micro Volts
KP	Transconductance Parameter

Symbols

V_{DD}	Supply Voltage [V]
I_D	Drain Current [A]
I_B	Bias Current [A]
V_{GS}	Gate to Source Voltage [V]
V_{th}	Threshold Voltage [V]
V_{DS}	Drain to Source Voltage [V]
K_P, K_N	Transconductance Parameters [$\frac{A}{V^2}$]
λ	Channel Length Modulation Parameter [$\frac{1}{V}$]
μ	Mobility of Carriers [$\frac{cm^2}{Vs}$]
C_{GS}	Gate to Source Capacitance [F]
C_{DB}	Drain to Bulk Capacitance [F]
g_m	Transconductance [S]
V_{out}	Output Voltage [V]
V_{in}	Input Voltage [V]
R_L	Load Resistance [Ω]
$R_{DS(on)}$	On-Resistance of the MOSFET [Ω]
C_{out}	Output Capacitance [F]
R_{ESR}	Equivalent Series Resistance [Ω]
f_P	Pole Frequency [Hz]
f_Z	Zero Frequency [Hz]
V_{ref}	Reference Voltage [V]
A_v	Voltage Gain
dB	Decibel
ΔV_{out}	Output Voltage Deviation [V]
W	Width of MOSFET [m]
L	Length of MOSFET [m]

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Chapter 1

Introduction

1.1 Introduction

In the rapidly evolving electronics industry, power management has become increasingly critical, particularly with the push toward a complete System-on-chip (SoC) design. This evolution aims to reduce power and area consumption, thereby decreasing costs and enhancing system reliability. Such advancements are driven by the growing demand for battery-operated mobile devices and handheld gadgets, including smartphones, pagers, personal digital assistants, video cameras, and laptops. These devices rely on efficient power management circuits to optimize performance and extend battery life. Consequently, there is a pressing need to innovate in power supply and conservation to enable portable devices to operate for extended periods without escalating production costs or enlarging power sources.

The prevailing trend is to minimize the number of battery cells to reduce both cost and size while also lowering the quiescent current to prolong battery life. Current efficiency is crucial, particularly at low load conditions where battery life is significantly impacted by high quiescent currents. Conversely, at high load currents, efficiency is generally better as the load current vastly exceeds the quiescent current. In such low-voltage environments, Low-Dropout (LDO) voltage regulators emerge as the ideal linear regulators.

This research endeavors to develop a methodology for designing LDO voltage regulators that function efficiently at low input voltages and quiescent currents without compromising performance. Given the substantial variations in battery voltage, these regulators are indispensable for nearly all battery-powered devices. Moreover, integrating these voltage regulators and other power supply circuits directly onto the chip is essential for maximizing portability and minimizing costs. LDO voltage regulators are thus suitable for a wide array of applications, including automotive, portable, industrial, and medical contexts.

1.2 Motivation

The rapid advancement and complexity of Systems-on-Chip (SoC) design demand robust power management solutions to ensure the stable and efficient operation of modern electronic devices. Among the essential components in these systems, Low-Dropout (LDO) regulators play a crucial role in providing clean and stable power

to noise-sensitive equipment. LDO regulators not only supply direct power rails but also effectively post-regulate other power sources, thereby mitigating noise from switching converters that can disrupt system performance [1].

Despite their effectiveness, LDO regulators face challenges related to power dissipation, which can negatively impact overall system efficiency. As a result, the design of LDO voltage regulators has gained significant attention over the years, particularly due to their scalability and improved performance across a variety of application domains.

The design and optimization of analog integrated circuits (ICs), especially for transistor sizing, present a significant challenge. Circuit designers must meticulously size various components to meet specific design criteria and achieve optimal performance, often requiring numerous iterations. This thesis aims to address these challenges by introducing a Python-based hybrid approach for LDO circuit design.

The proposed methodology involves the optimization of the error amplifier, pass transistor, and feedback network. Initial estimates of key parameters such as (W/L) ratios and compensation values are generated using Python-based techniques. These initial values are then refined using Cadence's inbuilt optimization algorithms to achieve precise and desired system parameters.

By automating and optimizing the design process, this approach aims to streamline the development of high-performance LDO regulators, ensuring they meet the stringent requirements of modern SoC designs while maintaining efficiency and stability [2].

1.3 Thesis Objective

The primary objective of this thesis is to develop and implement a comprehensive methodology for the optimization and automation of the Low-Dropout (LDO) regulator design flow. This methodology aims to overcome existing limitations in accuracy and speed, enabling the efficient design of LDO regulators across various output voltages and load currents. The key specifications considered in this work include Dropout Voltage, Power Supply Rejection Ratio (PSRR), Load Regulation, and Line Regulation.

This research focuses on:

1. Developing a robust methodology to optimize LDO designs for different output voltages and load currents.
2. Ensuring that the LDO regulator meets critical specifications such as Dropout Voltage, PSRR, Load Regulation, and Line Regulation.
3. Designing the error amplifier, pass element transistor, and feedback network integral to the LDO regulator.

The proposed design methodology integrates analytical design calculations with simulation-based assessments to expedite the optimization of the LDO regulator's design parameters. This hybrid approach leverages the predictive speed of analytical methods while ensuring the accuracy and thoroughness of simulation validations.

Automation of the initial sizing process is achieved using Python scripting, which serves as the cornerstone of this methodology. This approach aims to reduce the overall design time, making the design process more efficient and adaptable.

Moreover, this methodology is applied to two different technology nodes, demonstrating the feasibility of technology migration from a higher node to a lower node. For each technology, three different specifications are assumed, and initial reference

values are calculated. These values are then set as initial inputs in the Cadence Virtuoso local optimization algorithms, with final specifications extracted from the optimization process.

The ultimate goal is to streamline the design process, enhance efficiency, and validate the methodology's effectiveness across different technology nodes and specifications.

1.3.1 Structure of the Work

- **Chapter 2: Introduction of an LDO**

This chapter delves into the foundational concepts of LDO regulators. It covers the working principles, various structures, and essential components such as the pass element, error amplifier, feedback network, voltage reference, and output capacitor.

- **Chapter 3: Performance Parameters of an LDO**

This chapter discusses the critical performance parameters of LDOs, including dropout voltage, quiescent current, load regulation, line regulation, power supply rejection ratio (PSRR), and efficiency. It also addresses the transient response and frequency response characteristics.

- **Chapter 4: Design Optimization Methodology**

This chapter introduces the methodology for analog design automation, covering various levels of design from system-level to circuit-level. It discusses the proposed LDO design methodology, including topology selection, frequency compensation, and small signal modeling.

- **Chapter 5: Implementation of Design Optimization Methodology**

This chapter details the practical implementation of the design optimization methodology. It includes procedures for determining W/L ratios, the implementation of the design algorithm, design examples, and optimization processes using Python automation.

- **Chapter 6: LDO Design Methodology in 130nm Technology**

This chapter focuses on the LDO design methodology specifically tailored for 130nm technology. It covers the design flow, pass element design, error amplifier design, and detailed simulation results and analysis for three different cases.

- **Chapter 7: LDO Design Methodology in 22nm FDSOI Technology**

This chapter outlines the LDO design methodology adapted for 22nm FDSOI technology. It includes design considerations specific to 22nm FDSOI and provides simulation results and analysis for three cases similar to the previous chapter.

- **Chapter 8: Conclusion**

This final chapter summarizes the major contributions and findings of the thesis, discussing the implications for state-of-the-art LDO voltage regulator design. It suggests possible future work to extend the research.

Chapter 2

Literature Review Of Low Dropout Regulators

2.1 Introduction of an LDO

Low-Dropout (LDO) voltage regulators are fundamental components in power-management systems, playing a crucial role in ensuring the efficient operation of microprocessors and portable devices. These systems frequently employ multiple LDO regulators to provide a stable supply voltage with minimal ripple, catering to the needs of blocks susceptible to supply noise [3].

The primary role of a voltage regulator is to maintain a consistent output voltage, regardless of the operational state of the circuits powered by the LDO. An LDO acts as a voltage source that keeps a power rail's voltage level stable throughout battery discharge and load changes. The response time of an LDO to load fluctuations is critical — not only does it reduce power consumption, but it also ensures that the device quickly responds to user demands.

2.1.1 Working Principle of LDO

The standard block diagram of an LDO regulator, illustrated in Figure 2.1, encompasses essential components: a pass transistor (M_P), an error amplifier (EA), a feedback network with resistors R_{F1} and R_{F2} , and a load capacitor (C_L). The current source I_L represents the current required by the load. In this diagram, a reference block provides a stable reference voltage, V_{ref} . This setup employs a PMOS transistor as the pass element, extensively discussed in Chapter 4. The EA continuously compares the output voltage (V_{out}) with V_{ref} shown in equation 2.1. The gate of the PMOS pass transistor is controlled by the EA's output, allowing the adjustment of V_{out} to regulate the gate voltage. This feedback loop is vital for maintaining a stable output voltage, ensuring consistency amid variations in load or input.

$$V_{OUT} = \left(1 + \frac{R_{F1}}{R_{F2}}\right) V_{REF} \quad (2.1)$$

A conventional LDO operates within three operating regions based on the input power or supply voltage.

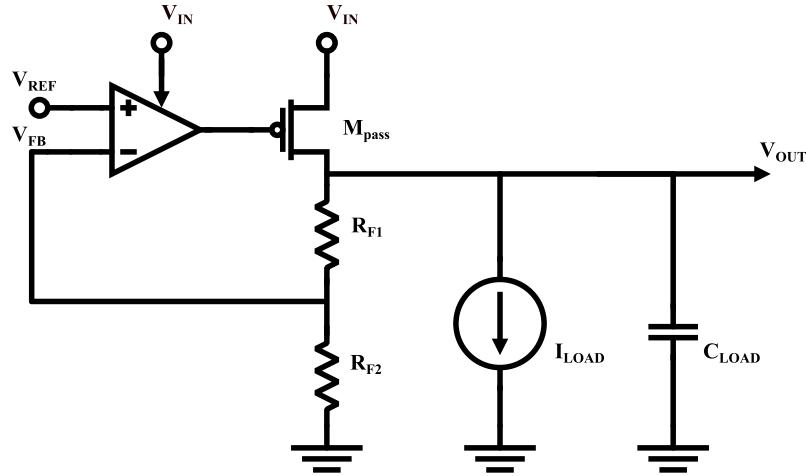


Figure 2.1: LDO regulator

Linear Region: In this region, the output voltage is sufficient for the LDO regulator to operate effectively. It maintains a stable output voltage and supplies the necessary current to the load.

Dropout Region: When the input power diminishes, the control loop's gain decreases, leading to a point where the LDO regulator can no longer maintain regulation. This occurs as one or more transistors enter the triode region.

OFF Region: At this stage, the supply voltage drops too low to keep the transistors in the ON state, resulting in the circuit being in a cut-off state.

The figure depicts the LDO regulator operating regions.

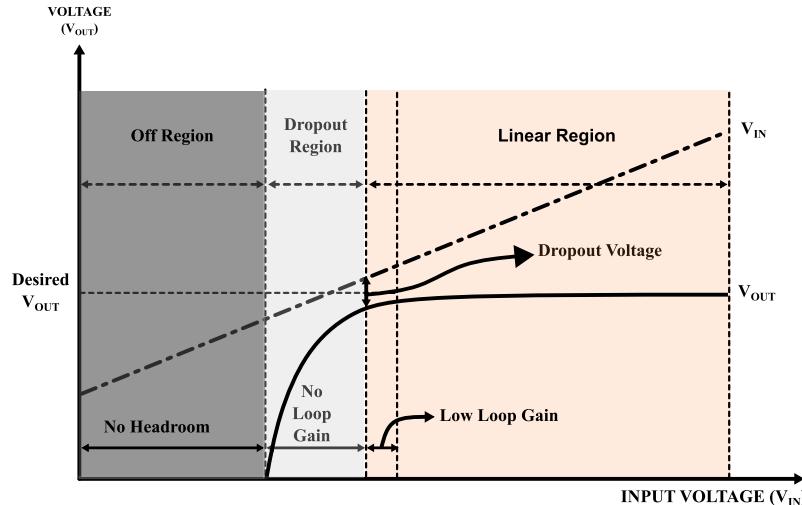


Figure 2.2: LDO input-output voltage behavior [4]

2.1.2 LDO Structures

An LDO regulator primarily consists of five critical blocks, each playing a pivotal role in its functionality.

1. Pass Element
2. Error Amplifier

3. Feedback Network
4. Voltage Reference
5. Output Capacitor

2.1.3 Pass Element

The output stage of linear regulators can be designed using various configurations, which are chosen based on the desired circuit performance and power efficiency. A critical factor in selecting the pass device is the dropout voltage, which is the minimum difference between the input and output voltages at which the regulator can still maintain the desired output voltage.

Figure 2.3 illustrates pass device topologies employed in CMOS linear regulators, including the NMOS source follower, and the PMOS common source configurations. Each topology has its unique characteristics and is chosen based on specific requirements related to performance and efficiency in the LDO's application.

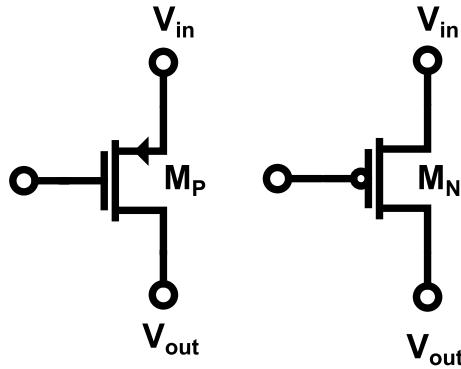


Figure 2.3: Pass Transistors PMOS (a), NMOS (b)

Generally, NMOS transistors, of the same size, exhibit superior current conduction capabilities due to higher electron mobility. However, PMOS transistors are often preferred for achieving low dropout voltage, despite their lower current conduction ability, because their gate voltage is always below the supply voltage.

In contrast, NMOS transistors can have a gate voltage higher than the supply voltage when designed for low dropout operation, requiring additional circuitry and increasing design complexity. Nonetheless, NMOS devices occupy less area for a given maximum current and offer better dynamic performance in large signal conditions, as the source node is directly connected to the output of the regulator. This direct connection facilitates rapid response to changes in load current, such as a shift from $I_{L_{\min}}$ to $I_{L_{\max}}$, causing V_{out} to decrease and V_{gs} to increase quickly, thus enabling the pass device to accommodate $I_{L_{\max}}$.

On the other hand, PMOS transistors require only a minimal dropout voltage, V_{dsat} , to be fully saturated, whereas NMOS transistors need at least $V_{sat} + V_{gs}$ for saturation, unless the process includes NMOS transistors with zero threshold voltage, known as native or zero-V_t transistors.

The pass device architecture also impacts the DC gain. With PMOS acting as a common-source stage, the overall gain is increased, enhancing steady-state regulation, as will be elaborated later in this chapter. In the case of NMOS, acting

as a common-drain (source follower), the DC gain is ideally unaffected, making the regulator easier to stabilize due to significantly lower output resistance [5].

Table 2.1 distinguishes between NMOS and PMOS pass elements used in LDOs. NMOS stands out for its low on-resistance and efficiency, important for power management. However, complexities in its gate drive make it less ideal in some scenarios. PMOS, after significant development, now exceeds many other devices in performance and is simpler to integrate into LDOs, making it a preferred choice in modern applications.

Table 2.1: Comparison of NMOS and PMOS Pass Element Structures [6]

Parameter	NMOS	PMOS
$I_{o,\max}$	Medium	Medium
I_q	Low	Low
$\Delta V_{\text{dropout}}$	$V_{\text{sat}} + V_{gs}$	$V_{DS}(\text{sat})$
Speed	Medium	Medium

2.1.4 Error Amplifier

The error amplifier's architecture must be straightforward, ensuring minimal quiescent current without sacrificing performance. A low output impedance is critical for system stability, while a high DC gain is pivotal for loop gain consistency under varying loads. The Gain Bandwidth Product (GBW) is crucial and must be designed with the understanding that it is limited by the Unity Gain Frequency (UGF), which plays a role in the Power Supply Rejection Ratio (PSRR). This detail will be expounded upon in Chapter 3. In operation, the error amplifier regulates the voltage by adjusting the reference voltage with the output feedback and modulating the pass device's gate to maintain the desired voltage level. The design must consider the pass device's requirements and the broader system specifications, prioritizing a substantial output voltage range to accommodate all current loads and input voltage conditions. The selection of the amplifier's topology directly affects the regulator's power supply rejection, underlining the necessity of a strategic balance between quiescent current and performance.

2.1.5 Feedback Network

The feedback network in an LDO can be designed using either a series of diode-connected transistors or a resistive divider network. Utilizing a resistive divider, as depicted in Figure 2.4A, offers enhanced precision and stability. Larger resistors are preferable as they exhibit fewer production variances and demonstrate minimal temperature-dependent changes. However, a significant drawback of resistive networks is their substantial area consumption, which becomes a critical factor when aiming to minimize current usage.

Conversely, employing a diode-connected transistor network for feedback, illustrated in Figure 2.4B, contributes to a reduction in the circuit's physical size. In this configuration, each transistor's body is linked to its source, ensuring uniform biasing

conditions [7]. With an equal current passing through these transistors, setting the feedback voltage V_{fb} becomes easy. For instance, if the transistors are of the same size, each one will incur an identical voltage drop V_{ds} or V_{gs} , given that $ID_1 = ID_2$. Consequently, the feedback voltage V_{fb} will be proportionally divided, instantiate by $V_{fb} = \frac{V_{OUT}}{2}$.

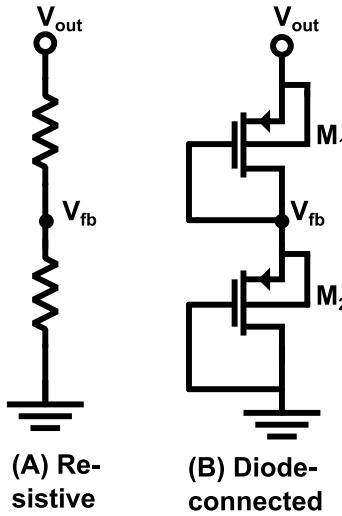


Figure 2.4: Feedback Network

2.1.6 Voltage Reference

The voltage reference establishes the operating point for the error amplifier, serving as the starting point of all regulators. Commonly, this voltage reference is derived from a band-gap circuit due to its capability to function at low supply voltages and its satisfactory accuracy and stability across a range of temperatures, which are crucial for linear regulator designs [8]. Key aspects of the voltage reference include its output noise and its impact on the overall Power Supply Rejection Ratio (PSRR) of the error amplifier. These effects can be mitigated by integrating passive filtering components, such as RC filters, into the design.

2.1.7 Output Capacitor

The output capacitor plays a crucial role in ensuring that during load transients, current is swiftly supplied to the load while the error amplifier adjusts to the new conditions. Additionally, it is vital for the system's stability, as it introduces a low-frequency pole and a zero at higher frequencies in the system's response.

The zero introduced by the output capacitor is associated with its Equivalent Series Resistance (ESR), which can be conceptualized as a resistor in series with the capacitor. A lower ESR is beneficial for reducing overshoots during load transients because a higher ESR limits the rate at which the capacitor can supply current to the load. Conversely, a higher ESR can contribute to enhanced system stability, illustrating the trade-offs involved in selecting the appropriate ESR value for a given application.

2.2 Performance Parameters of an LDO

Design specifications are essential for assessing the LDO's performance during both steady-state and transient conditions. The subsequent sections will explore these parameters in detail.

2.2.1 Dropout Voltage

The dropout voltage is defined as the minimum voltage difference between V_{IN} and V_{OUT} required to maintain specified voltage regulation. A linear regulator capable of functioning with low dropout voltage is typically referred to as a Low-Dropout regulator (LDO). According to [4], an LDO in the context of battery-powered applications is identified by a dropout voltage of less than 600 mV.

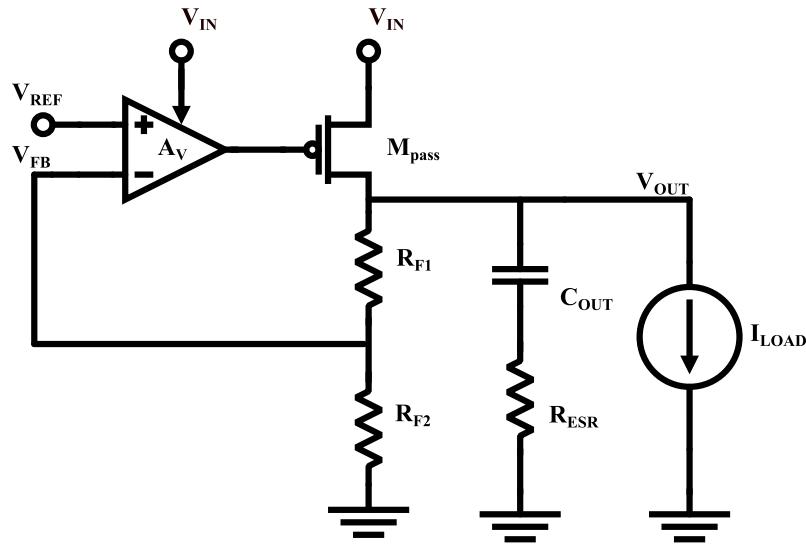


Figure 2.5: Conventional PMOS LDO Schematic

The analysis starts from the PMOS LDO shown in Figure 2.5. The differential voltage, V_{drop} , is calculated by subtracting V_{OUT} from V_{IN} and is represented by 2.2

$$V_{drop} = V_{IN} - V_{OUT} \quad (2.2)$$

When V_{drop} is minimal, the pass transistor functions similarly to a switch with significantly reduced loop gain, which complicates the regulation of V_{OUT} . Additionally, V_{drop} is affected by the maximum load current, I_{load} , and the on-resistance of the pass transistor, R_{ON} . This relationship is given by 2.3

$$V_{drop} = I_{load} \times R_{ON} \quad (2.3)$$

2.2.2 Quiescent Current

Quiescent current I_q , also referred to as ground current, is the current consumed by the regulator when no load is attached. It is the difference between the input and output currents. Achieving a minimal quiescent current is crucial for optimizing current efficiency. The quiescent current, denoted as 2.4

$$I_q = I_i - I_o \quad (2.4)$$

The quiescent current, which is the sum of the bias currents for components such as the band-gap reference, sampling resistor, and error amplifier, along with the drive current for the pass element, doesn't contribute to the output power. Typically, the value of the quiescent current is governed by the pass element, the chosen circuit topologies, and the surrounding environmental temperature [6]. The drain-source current for MOS transistors denoted as I_{ds} , is determined by the equation 2.5.

$$I_{ds} = \beta_1(V_{gs} - V_t)^2 \quad (2.5)$$

Here, β_1 signifies the MOS transistor gain factor, V_{gs} is the gate-to-source voltage, and V_t represents the threshold voltage of the device.

2.2.3 Load Regulation

Load regulation quantifies a circuit's ability to maintain a constant output voltage across different loading conditions. It is expressed as the ratio of the change in output voltage to the change in output current and is given by equation 2.6.

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (\text{V/A}) \quad (2.6)$$

Voltage variation (ΔV_{OUT}) in response to changes in static load current (ΔI_{OUT}) is a key factor in load regulation. PMOS load regulation analysis, as shown in Figure 2.5, utilizes a small-signal methodology. In this context, A_v symbolizes the open-loop gain of the error amplifier, g_{mp} the transconductance of the PMOS, I_{load} the current passing through the load, and C_{OUT} the output capacitor (assuming R_{ESR} is negligible). The relationship between the output voltage variation and load current is expressed by the following equations:

$$I_{OUT} + \frac{V_{sd}}{r_{ds} \parallel (R_{F1} + R_{F2})} + g_{mp} V_{sg} = 0 \quad (2.7)$$

In Equation 2.7, I_{OUT} is the total output load current calculated by applying Kirchhoff's Current Law (KCL) at the output node. Here, V_{sd} is the source-to-drain voltage of the pass transistor, r_{ds} is the drain-source resistance of the pass transistor, g_{mp} is the gain factor of the pass transistor, and V_{sg} is the source-to-gate voltage of the pass transistor.

$$I_{OUT} + \frac{(-V_{OUT})}{r_{ds} \parallel (R_{F1} + R_{F2})} + g_{mp}(-\beta A_E V_{OUT}) = 0 \quad (2.8)$$

In Equation 2.8, β represents the feedback factor $\frac{R_{F2}}{R_{F1} + R_{F2}}$, and A_E denotes the gain of the error amplifier.

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} \approx -\frac{1}{g_{mp} \beta A_E} \quad (2.9)$$

From Equation 2.9, it is evident that the load regulation capability is dictated by both the error amplifier's open-loop gain A_v and the transconductance g_{mp} of the PMOS. Figure 2.6 depicts the load regulation characteristics of an LDO, illustrating the behavior from minimum to maximum load under steady-state DC conditions.

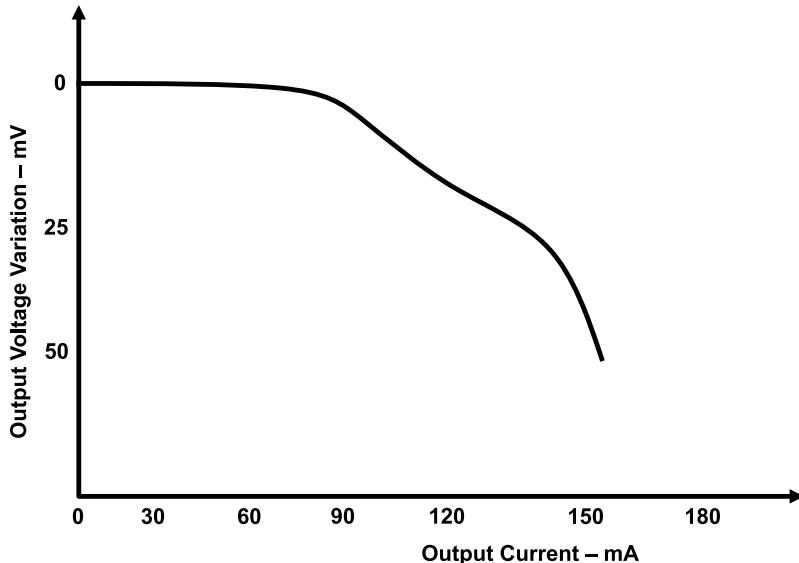


Figure 2.6: Load Regulation @DC [6]

2.2.4 Line Regulation

Line regulation also measures the output voltage variation that occurs when there is a change in the input voltage, with the measurement taken after the output voltage has reached a steady state. The line regulation is represented by the equation 2.10.

$$\text{Line regulation} = \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} \quad (2.10)$$

The regulated voltage is expected to remain constant until the regulator's effectiveness begins to drop. Nevertheless, due to the limited loop gain, the actual output voltage tends to vary close to the supply voltage. Although line regulation is categorized as a DC parameter, analyzing it in the small-signal domain can be easier. Consider the PMOS regulator depicted in Figure 2.5, where g_{mp} denotes the transconductance of MPASS, r_{dsp} is the output resistance, and A_v the open-loop gain of the error amplifier. With a minor change at the V_{IN} node by ΔV_{IN} , there should be a corresponding change at the V_{OUT} node by ΔV_{OUT} . The relationship can be described by the equation 2.11.

$$(\Delta V_{\text{IN}} - \Delta V_{\text{OUT}} \frac{R_{F2}}{R_{F1} + R_{F2}} A_v) g_{\text{mp}} [(R_{F1} + R_{F2}) || r_{\text{dsp}}] = \Delta V_{\text{OUT}} \quad (2.11)$$

Generally, the value $g_{\text{mp}} [(R_{F1} + R_{F2}) || r_{\text{dsp}}]$ is significantly greater than 1, allowing the Equation 2.11 to be simplified to equation 2.12.

$$\frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{IN}}} = \frac{g_{\text{mp}} [(R_{F1} + R_{F2}) || r_{\text{dsp}}]}{1 + g_{\text{mp}} [(R_{F1} + R_{F2}) || r_{\text{dsp}}] A_v} \frac{R_{F2}}{R_{F1} + R_{F2}} \approx \frac{1}{A_v \beta} \quad (2.12)$$

Here, β represents the feedback factor $\frac{R_{F2}}{R_{F1} + R_{F2}}$. This simplification shows that the line regulation is inversely proportional to the product of the open-loop gain A_v and the feedback factor β .

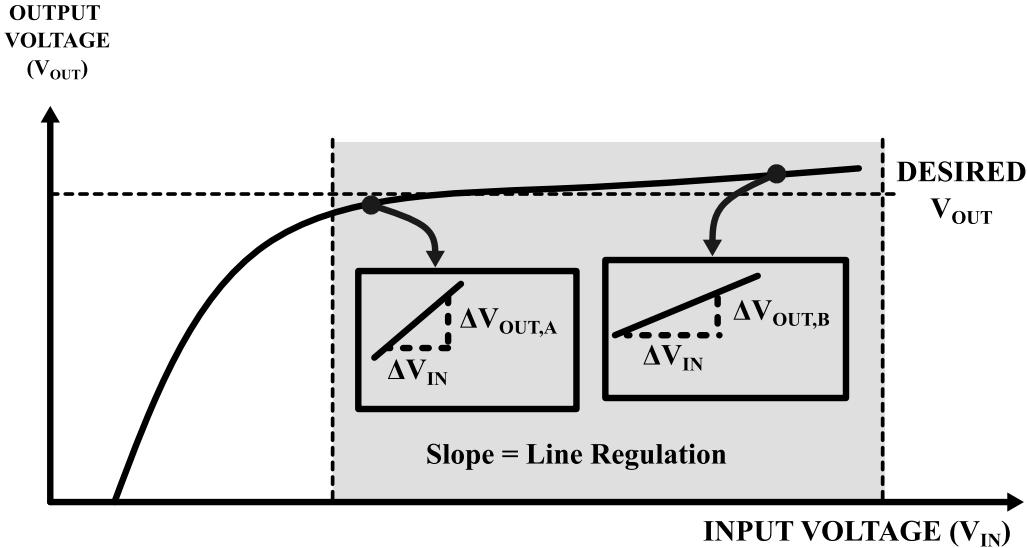


Figure 2.7: Line Regulation [9]

Figure 2.7 illustrates the line regulation characteristics of the LDO, where point A denotes the minimum input voltage ($V_{IN,A}$) and point B represents the maximum input voltage ($V_{IN,B}$) of the LDO. At point A, the output voltage $V_{OUT,A}$ is nearly equal to the desired output voltage (V_{OUT}), and similarly at point B, $V_{OUT,B}$ is also nearly equal to V_{OUT} . The line regulation of the LDO is determined by the slope of the output voltage curve, calculated as the ratio of the change in output voltage to the change in input voltage.

$$\text{Line regulation} = \frac{V_{OUT,B} - V_{OUT,A}}{V_{IN,B} - V_{IN,A}}$$

2.2.5 Power Supply Rejection Ration

The power supply rejection ratio (PSRR) of a linear regulator is characterized by its ability to maintain a constant output voltage (V_{OUT}) despite fluctuations or noise present in the input voltage (V_{IN}) [10]. As depicted in Figure 2.8(a), a linear regulator diminishes the influence of supply noise at its regulated output. Unlike line regulation, which is a DC specification, PSRR pertains to the AC domain and is therefore assessed using small signal analysis. The PSRR is mathematically expressed as:

$$\text{PSRR} = |20 \log_{10} \left(\frac{V_{OUT}}{V_{IN}} \right)|$$

Figure 2.8 illustrates a linear regulator reducing the supply noise at its regulated output. Where $V_{INRIPPLE}$ represents the ripple present on the input voltage (V_{IN}) of the LDO, while $V_{OUTRIPPLE}$ denotes the ripple on the output voltage (V_{OUT}) of the LDO. These parameters are critical for assessing the performance of the LDO in filtering out input voltage fluctuations and maintaining a stable output voltage. The Bode plot of PSRR, as shown in Figure 2.9, illustrates that at lower frequencies, the supply variation is treated as a DC component, corresponding with the line regulation discussed in 2.2.4. In this low-frequency region, extending from DC to a few

kHz, the LDO demonstrates a high PSRR by effectively attenuating input voltage ripple[11]. As frequencies increase into the mid-frequency range, from a few kHz to 100 kHz, the PSRR starts to drop, indicating a decrease in the regulator's ability to suppress variations in the supply voltage. This reduction is primarily due to the reduced feedback loop gain and the influence of capacitors in the linear regulator that create AC signal paths between the supply and output. The trend continues into the high-frequency region, above 100 kHz, where the PSRR further declines, showcasing the LDO's constrained capacity to mitigate high-frequency input voltage noise or ripple.

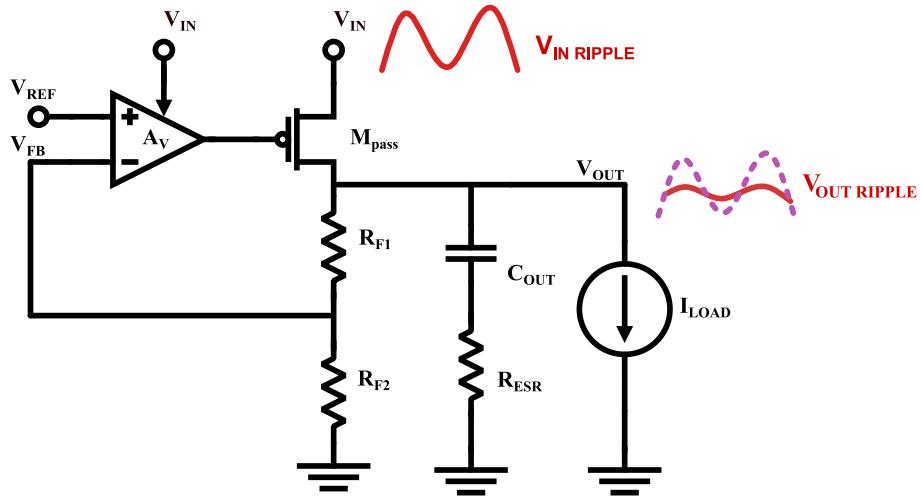


Figure 2.8: PSRR of PMOS LDO

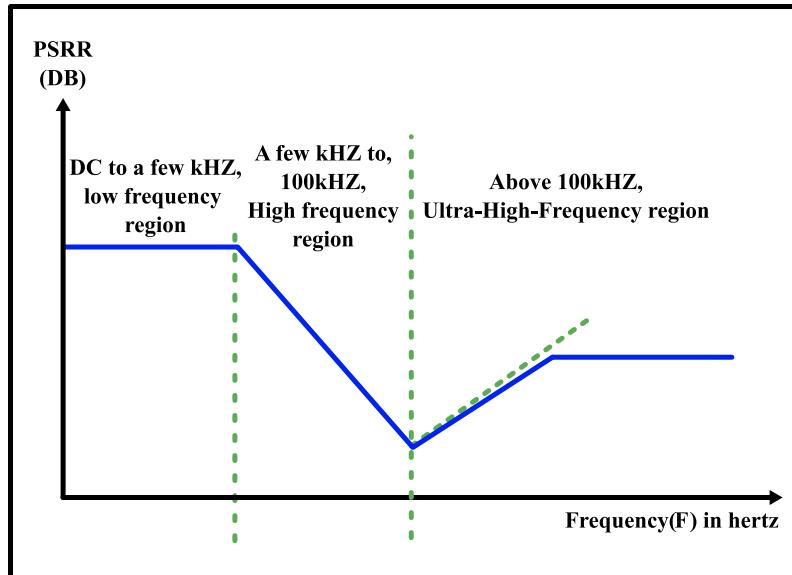


Figure 2.9: PSRR curve of an LDO [11]

For PMOS linear regulators, noise from the power supply is directly reflected at the PMOS power transistor's source. Achieving high PSRR performance involves ensuring that the gate node's variations mirror those at the source node, thereby maintaining a constant V_{SG} (voltage between the source and the gate). This sta-

bility is crucial for minimizing the impact of supply noise on the regulator's output, enhancing the overall performance of the linear regulator.

2.2.6 Efficiency

The efficiency of an LDO (Low-Dropout) regulator is inherently constrained by its quiescent current as well as the ratio between its input and output voltages. The efficiency equation for an LDO regulator is given by the equation 2.13.

$$\text{Efficiency} = \frac{I_O V_O}{(I_O + I_q)V_I} \times 100 \quad (2.13)$$

To achieve a high-efficiency LDO regulator, it's imperative to reduce both the dropout voltage and the quiescent current. Furthermore, the voltage differential between input and output should be as small as possible because the power dissipation in LDO regulators, which is calculated as $(V_I - V_O) \times I_O$, directly impacts the overall efficiency. This input-to-output voltage difference is a fundamental factor affecting efficiency, irrespective of the load conditions.

2.3 Transient Response of LDO

Two key dynamic state specifications for linear regulators are their reactions to transients in supply voltage and load current. The accuracy of the regulator's output can be compromised by ripples in output voltage and the time taken for recovery, which in turn can degrade the quality of the voltage delivered to the load. Ensuring a robust transient response is critical; minimal fluctuations, including overshoots and undershoots, are essential to avoid unintentional power-offs or resets of the load device. Spikes in the output voltage occur within the large signal domain, where slew rates are high and behavior is non-linear, making it challenging to precisely determine spike amplitude and recovery duration[12].

In this section, the transient behavior is dissected into distinct time intervals for better qualitative analysis. A comparative study of linear regulators with infinite versus finite bandwidth is conducted with reference to Figure 2.10. The response to transients is typically classified into two categories Load Transient and Line Transient.

2.3.1 Load Transient

Load transient refers to the variation in the output voltage that results from an abrupt change in the load current (I_{load}). In an LDO, a sudden increase from minimum to maximum load current can cause undershoots, while a decrease from maximum to minimum load can lead to overshoots in the output voltage shown in Figure 2.11. Typically, the magnitude of output voltage overshoot is constrained by the supply voltage, whereas undershoot has the potential to reach down to the ground potential.

The regulator's ability to react to these rapid load transitions is influenced by the load current magnitude, the output capacitor, and the LDO's response time. The output voltage fluctuation can be quantified by Equation 2.14.

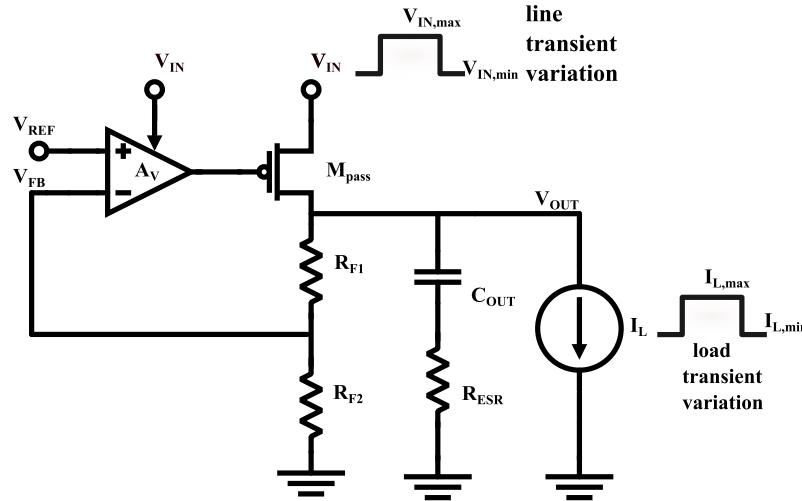


Figure 2.10: Transient response of PMOS regulator [12]

$$\Delta V_{OUT} = \frac{I_{MAX}\Delta t_r}{C_{OUT}} \quad (2.14)$$

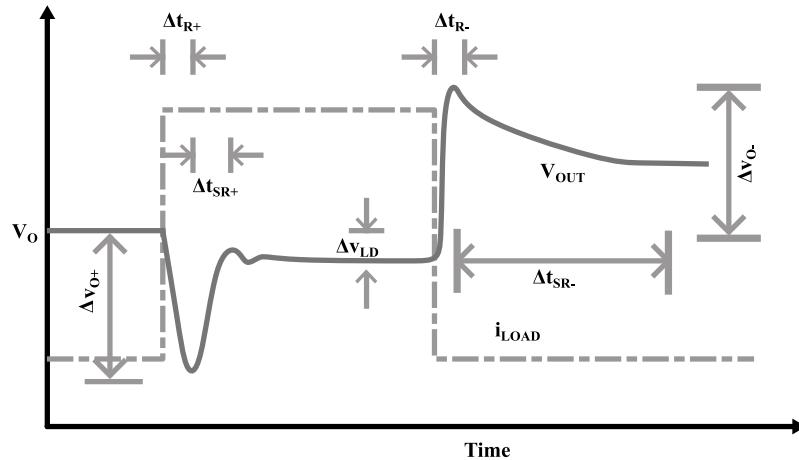


Figure 2.11: Typical transient response to abrupt load current changes [4]

Where I_{MAX} refers to the maximum output current, C_{OUT} is the output capacitor, and Δt_r represents the response time of the regulator. It is evident that ΔV_{OUT} , the variation in output voltage, is inversely related to C_{OUT} . Typically, LDO designs incorporate a sizable output capacitor in parallel with the load to serve as a reservoir of charge during rapid load current shifts, which enhances the regulation of output voltage and contributes to AC stability. As a result, such configurations exhibit superior load regulation compared to LDOs without output capacitors.

The regulator's response time, Δt_r (Δt_{R+} , Δt_{R-}), is affected by the closed-loop bandwidth and internal slew rate, due to parasitic capacitors that induce slewing effects, thus disrupt the load response of the regulator. The response time is computed as follows 2.15.

$$\Delta t_r = t_{BW} + t_{SR} = \frac{2.2}{BW} + \frac{C_{pass}\Delta V_{pass}}{I_{SR}} \quad (2.15)$$

Here, t_{SR} is the slew rate time, $\frac{2.2}{BW}$ is the delay from bandwidth, C_{pass} is the gate parasitic capacitance, and I_{SR} is the current that drives C_{pass} . The value of C_{pass} is primarily from the gate capacitance of the large pass transistor.

The derivation of the expression for bandwidth (BW) involves defining the rise time as the duration for the output voltage to ascend from 10% to 90% of its step change. Based on the standard step response, the times for 10% ($t_{10\%}$) and 90% ($t_{90\%}$) can be described as following equations.

$$V(t) = V_{OUT} \left(1 - e^{-\frac{t}{\tau}} \right) \quad (2.16)$$

$$0.1 = 1 - e^{-\frac{t_{10\%}}{\tau}} \quad (2.17)$$

$$0.9 = 1 - e^{-\frac{t_{90\%}}{\tau}} \quad (2.18)$$

The rise time (t_{rise}) is then:

$$t_{rise} = t_{90\%} - t_{10\%} = 2.2\tau \quad (2.19)$$

For the output voltage to reach 90% of its final value, the time equivalent to 2.2 time constants ($R_{OUT}C_{OUT}$) must pass elapse 2.20.

$$t_{BW} = 2.2RC = \frac{2.2}{2\pi f_{-3dB}} \quad (2.20)$$

2.3.2 Line Transient

The line transient response is a key dynamic characteristic of a system. It refers to the system's ability to maintain a stable output voltage when there are sudden changes in the input voltage. For instance, if the input voltage rises rapidly from zero to its maximum value, the output voltage should stabilize within a specific time. Additionally, if there's a sudden shift in the line voltage from, say, 2 V to 2.2 V, the output voltage is likely to experience an overshoot as a result of the rapid increase in the output current. Conversely, a sudden decrease in the line voltage will cause an immediate drop in the output voltage, which corresponds to a decrease in the load current (I_{load}).

2.4 Frequency Response of LDO

Nearly all Low-Dropout voltage regulators (LDOs) employ a negative feedback loop to maintain a consistent output voltage regardless of the load connected to the system's output. The high gain of the feedback loop determines the positioning of poles and zeros (critical components of the system's transfer function). For a comprehensive stability analysis, it's essential to consider the potential range of loads and variations within loop components. Each pole and zero introduces a phase shift of ± 90 degrees and a gain change of ± 20 dB/decade. The phase margin at the Unity Gain Frequency (UGF), or 0 dB point, is used to assess system stability. The UGF represents the frequency where the system's gain equals one (0 dB on a logarithmic scale) and indicates the maximum usable frequency for the regulator.

Stability analysis for an LDO requires a comprehensive examination of all system components, including the error amplifier, pass device, output capacitor, Equivalent Series Resistance (R_{ESR}), and the feedback network. As depicted in Figure 2.12, the pass device operates in a common-source configuration with a negative voltage gain. The feedback signal is fed into the positive input of the error amplifier to establish a negative feedback loop. When utilizing an amplifier with two inverting stages, the pass device functions as a third stage of gain, inverting the signal to ensure the feedback loop remains negative, essential for stable operation.

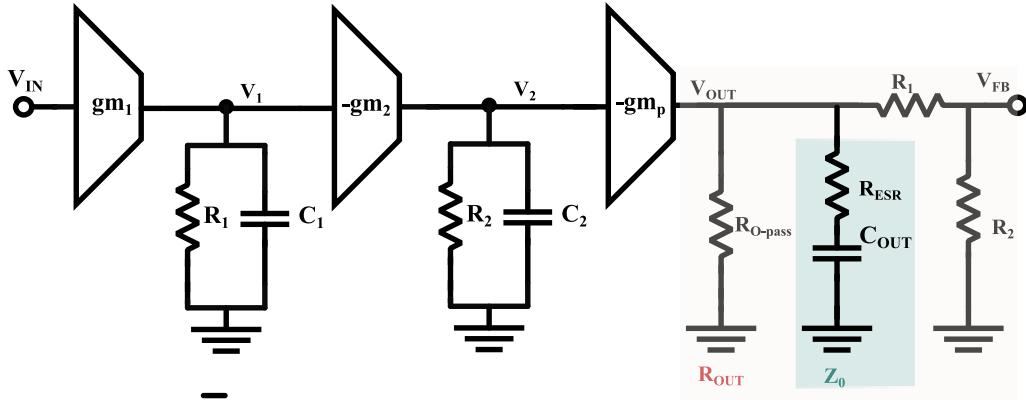


Figure 2.12: Small signal model of LDO

Upon examining the fundamental topology of an LDO, as depicted in Figure 2.12, one can discern two poles and a single zero. If the voltage scaled by the feedback network (V_{fb}) and the voltage at the positive terminal of the amplifier (V_{In}) are considered as the output and input voltages respectively, the open-loop transfer function (A_v) can be articulated as shown in equation 2.21.

$$|A_v| = \frac{V_{fb}}{V_{In}} = g_{m1}g_{m2} \cdot \frac{R_1}{1 + sC_1R_1} \cdot \frac{R_2}{1 + sC_2R_2} \cdot g_{mp} \cdot Z_{out} \cdot \frac{R_1}{R_1 + R_2} \quad (2.21)$$

Here, g_{m1} and g_{m2} represent the transconductance of the error amplifier's first and second stages, while g_{mp} is the transconductance of the pass device. R_1 and R_2 denote the output resistances of the first and second stages of the amplifier, respectively. C_1 is the parasitic capacitance associated with the second stage, and C_2 is the parasitic capacitance related to the pass device. Z_{out} signifies the output impedance, delineated by the equation 2.24.

$$Z_o = \frac{1 + sC_{out}R_{ESR}}{sC_{out}} \quad (2.22)$$

$$R_{out} = R_{opass} \parallel (R_1 + R_2) \quad (2.23)$$

$$Z_{out} = R_{out} \parallel Z_{co} \quad (2.24)$$

Where C_{out} and R_{ESR} correspond to the capacitance and equivalent series resistance (ESR) of the output capacitor, respectively. R_{out} is the system's output resistance, combining R_{opass} , the pass device's output resistance, and the resistances

R_1 and R_2 . Consequently, Equation 2.21 can be expanded to incorporate these elements, leading to a revised representation of the open-loop transfer function in equation 2.25.

$$|A_v| = g_{m1} \cdot g_{m2} \cdot \frac{R_1}{1 + sC_1 R_1} \cdot \frac{R_2}{1 + sC_2 R_2} \cdot g_{mp} \cdot \frac{R_{out}(1 + sC_{out}R_{ESR})}{1 + sC_{out}(R_{out} + R_{ESR})} \cdot \frac{R_2}{R_1 + R_2} \quad (2.25)$$

The locations of the poles and the zero in the system are estimated through the following equations:

For the first pole (f_{P1}):

$$f_{P1} = \frac{1}{2\pi \cdot C_{out}(R_{out} + R_{ESR})} \approx \frac{1}{2\pi \cdot C_{out}(R_{o-pass} || (R_1 + R_2))} \quad (2.26)$$

For the second pole (f_{P2}):

$$f_{P2} = \frac{1}{2\pi \cdot C_1 R_1} \quad (2.27)$$

For the third pole (f_{P3}):

$$f_{P3} = \frac{1}{2\pi \cdot C_2 R_2} \quad (2.28)$$

And for the zero (f_{Z1}):

$$f_{Z1} = \frac{1}{2\pi \cdot C_{out}R_{ESR}} \quad (2.29)$$

Contributions from other poles due to input stage parasitic capacitors are considered negligible because they occur at high frequencies, which are lower than the loop's Unity Gain Frequency (UGF). As indicated by Equations 2.26 and 2.29, the pole and zero are dependent on the output capacitor C_{out} .

The DC open-loop gain $|A_v|$ is described by Equation 2.30 and is proportional to the output resistance, which is augmented by the factor $g_{mp}R_2$. Consequently, as this factor increases, so does the gain. It is also noted that the factor $g_{mp}R_2$ diminishes with the square root of the increasing current for a PMOS pass device, inversely proportional to the square root of the load current.

$$|A_v| = \frac{g_{m1} \cdot g_{m2} \cdot g_{mp} \cdot R_{o1} \cdot R_{o2} \cdot R_{out} \cdot R_2}{R_1 + R_2} \quad (2.30)$$

Figure 2.13 reveals a system with three poles and a zero. Notably, the zero is present at a lower frequency than the Unity Gain Frequency (UGF). This configuration of two poles and one zero below the UGF produces a stable system [13]. For enhancing the phase margin and ensuring the stability of the system, it is crucial for designers to adhere to two primary conditions[14].

The zero should be positioned beneath the system's UGF to effectively maintain stability. Poles at higher frequencies should be set at a distance, ideally over three times the UGF.

To ensure LDO performance prediction, this work analyzes the real performance of the error amplifier, rather than using ideal models. A two-stage operational

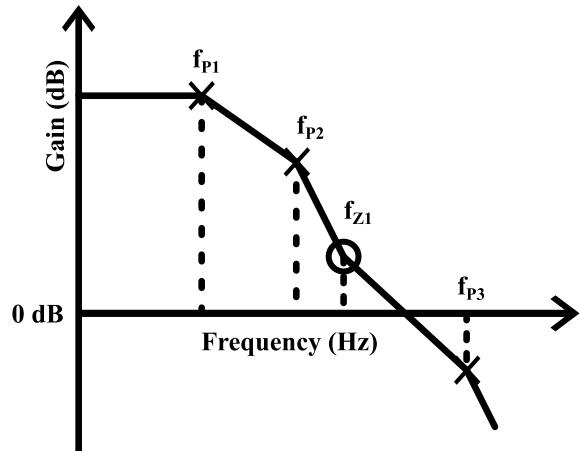


Figure 2.13: LDO open-loop response

transconductance amplifier (OTA) serves as the error amplifier in our design. The proposed optimization process simultaneously takes into account all capacitors, resistors, and the error amplifier within the LDO circuit. This holistic approach guarantees the performance of the final LDO design while controlling overall costs, including the error amplifier. The next chapter will delve into the design optimization methodology used to design the error amplifier for the LDO and model the LDO's behavior.

Chapter 3

Design Optimization Methodology

3.1 Introduction to Analog Design Automation

Rising demand for integrated circuits highlights the urgent need for rapid design methods to shorten development time. While digital circuit design benefits from mature, automated workflows, analog design remains less supported. Unlike digital circuits, which follow standardized Electronic Design Automation (EDA) tools, analog circuits rely heavily on manual effort and lack comprehensive automation across design stages.

In the pre-layout stage, analog design can be framed as an optimization problem shown in figure 3.1 where the goal is to find the transistor dimensions to achieve target specifications like gain and bandwidth. This optimization task presents significant challenges. This optimization problem presents significant challenges. It necessitates searching for optimal parameters across a vast design space, encompassing diverse devices. The problem's complexity increases exponentially as the number of design variables and desired specifications grows [15].

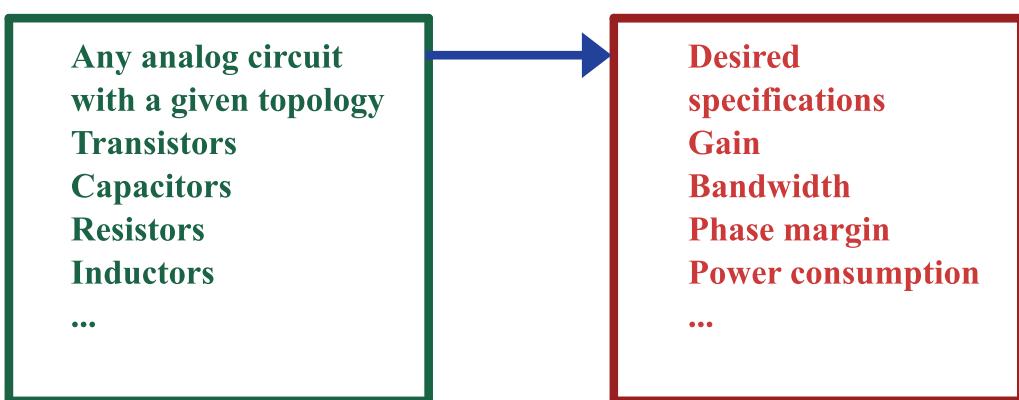


Figure 3.1: LDO open-loop response [16]

Analog and mixed-signal design relies heavily on specific rules and techniques to meet performance targets. However, design methodologies and CAD tools in this domain lag behind their digital counterparts, making complex analog design flows difficult. Analog circuits are more susceptible to fabrication variations than

digital circuits, impacting parameters like power consumption, gain, bandwidth, phase margin, slew rate, noise, power, and area. This sensitivity makes reusing analog IP (intellectual property) expensive and complex. Additionally, second and third-order effects, often negligible in digital design, become highly significant in analog circuits [17].

3.1.1 Analog IC Design Flow

Analog system design can be approached in two ways: flat or hierarchical. The flat approach tackles the entire circuit at once. However, the increasing complexity of analog systems has made this method less popular. The hierarchical approach uses a divide-and-conquer strategy and consists of two flows: top-down design and bottom-up verification [17] [18]. Each flow involves multiple steps with specific design tasks [19]. Due to its ability to manage complexity, the hierarchical approach is broadly preferred for modern analog and mixed-signal integrated circuits. Figure 3.2 illustrates a typical design flow, briefly describing each step below.

3.1.2 System-Level

The system-level stage is the initial phase in designing analog/mixed-signal systems. Here, the focus is on the technology process, goals, and overall system specifications. The system architecture is created and divided into high-level functional blocks to guide subsequent design steps. System-level specifications are translated into intermediate parameters that will define the requirements for lower-level building blocks. High-level behavioral modeling and simulation tools (such as Python, MATLAB, or Verilog AMS) are used to verify these design decisions and specifications.

3.1.3 Block-Level

The block-level stage refines the high-level design into detailed functional blocks that achieve the desired system behavior. Each functional block is described independently using a hardware description language (HDL) like VHDL or VHDL-AMS. To ensure they meet the specified requirements, these blocks undergo behavioral simulations using tools such as Ultrasim, NcSim, Hsim, or Modelsim.

3.1.4 Circuit-Level

At the circuit level, designers focus on optimizing each analog functional block through a tailored process driven by specifications and the chosen technology. This iterative stage involves selecting the best circuit topology and determining the precise sizing of the circuit's components (transistors, etc.). Designers simulate process variations and device tolerances to make the design resilient against manufacturing variability, aiming for a high-yield product. Finally, the circuit undergoes rigorous testing in a circuit-level simulator, like Cadence Spectre and HSPICE, to verify its performance against the target specifications.

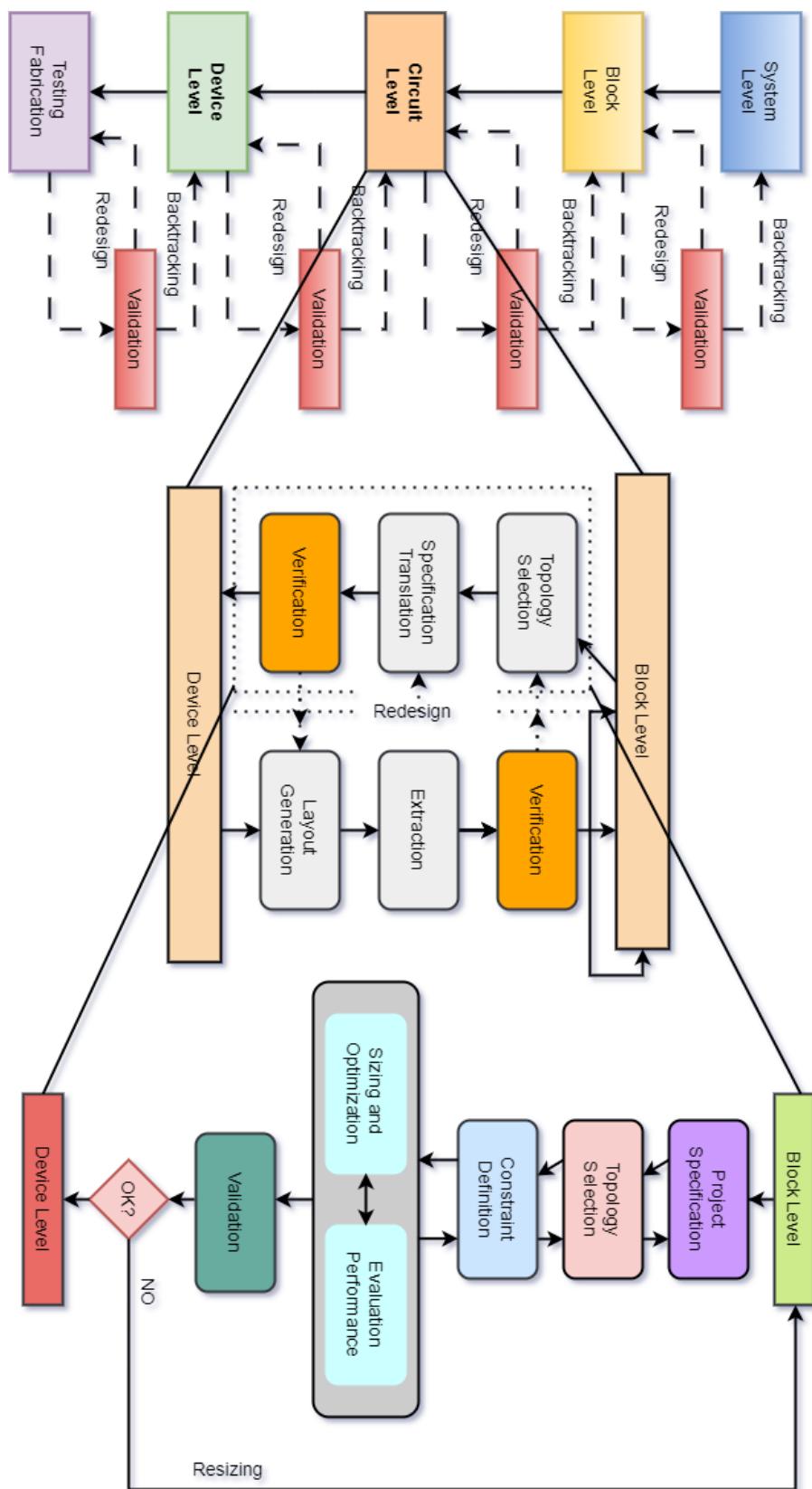


Figure 3.2: Analog Design flow top-down circuit-level design flow [18] [19]

3.1.5 Layout hierarchy

The layout hierarchy stage focuses on transforming the circuit schematic into a physical layout composed of multiple layers. This process uses the optimized building blocks created earlier. The layout itself is a collection of geometric shapes that must adhere to the design rules of the fabrication process. The goal is to minimize the layout area, and this can be achieved through manual or automated design. After design rule verification (DRC), parasitics within the layout are extracted. Circuit simulation then confirms that these parasitics don't significantly degrade the circuit's performance from the original target specifications. Additionally, layout techniques are crucial for managing crosstalk, substrate coupling, and mismatch issues.

3.1.6 Fabrication and Testing

The final phase in creating an integrated circuit is fabrication and testing. This involves producing the IC using a series of mask-generation processes. Throughout the fabrication process, multiple quality control checks are performed to minimize defects in the final chip. A test bench and setup are used to test the circuit and make sure it functions as designed.

These different levels of abstraction (in chip design) can be approached using both top-down and bottom-up methodologies, often combined with design changes or backtracking for optimization [19] as illustrated in Figure 3.2. In this work, the primary emphasis lies on the Circuit-level design methodology within this hierarchy. Therefore, the following discussion centers on top-down and bottom-up flows specifically related to the circuit level.

The Top-down flow encompasses these stages:

(a) Topology Selection - This stage of the design process focuses on selecting the appropriate circuit topology to fulfill the requirements established at the system and block levels. One selection method involves using a database and applying heuristic rules to manually identify suitable topologies. This approach assesses the feasibility of each topology within the database to determine if it can achieve the desired specifications. An alternative technique, known as the optimization-based approach [18], integrates topology selection with the process of determining device sizes.

(b) Specification Translation/Sizing - This step, known as specification translation or sizing, aims to achieve an optimized design that fulfills all the desired specifications using the chosen circuit topology. High-level specifications originating from the upper levels of the design hierarchy are translated and distributed to the individual sub-blocks within the system. Ultimately, these specifications determine the sizing of the transistors within each sub-block. Essentially, at higher levels of the hierarchy, this process involves decomposing the block under design into a subset of specifications that are passed down to each sub-block within the hierarchy, ensuring the overall block meets its intended functionality. At the lowest levels of the hierarchy, where sub-blocks are realized as individual devices (transistors, resistors, etc.), circuit sizing is performed based on performance specifications and the chosen topology received from upper levels. Two primary approaches are used for this process: a knowledge-based approach and an optimization-based approach that leverages various optimization methods.

(c) Synthesis Verification - Following the transistor sizing within each block,

the design undergoes simulation and verification to confirm whether the optimized circuit meets the designated specifications. If the desired performance is achieved, the design process progresses to the sub-blocks at the lower level of the hierarchy. However, suppose the circuit fails to meet specifications. In that case, the entire process might need to be restarted within the same hierarchical level for redesign, or potentially at other hierarchical levels for adjustments (backtracking).

The bottom-up flow layout involves the following stages:

- (a) Layout Generation - The physical layout for each sub-block is created and optimized, taking into account all applicable design constraints.
- (b) Extraction - Upon successful completion of Design Rule Checking (DRC) and Layout Versus Schematic (LVS) verification, the layout undergoes extraction. This process approximates the impact of fabrication effects (known as parasitics) on circuit performance.
- (c) Layout Verification - The extracted layout is then simulated and verified to assess how layout parasitics affect the circuit's overall functionality. If parasitics cause a significant deviation from the results of the schematic simulation, a redesign process might be necessary, potentially involving associated blocks within the same hierarchical level or across different levels.

3.2 Proposed LDO Design Methodology

3.2.1 Introduction to Methodology

In this work, A design methodology specifically intended for implementation at the circuit level within a hierarchical design flow is presented. Building upon this initial sizing, frequently, the initial sizing stage yields a design that is close to optimal, requiring only minor adjustments using a circuit optimization tool. The optimized design then undergoes thorough evaluation using a simulator like SPICE to confirm its performance. If necessary, the synthesis process can be repeated iteratively to achieve a design that closely aligns with the desired specifications [19]. The detailed illustration of this methodology is shown in Figure 3.3.

However, for improved efficiency and to account for real-world complexities, in the realm of analog IC design, optimizing design variables such as transistor sizes, bias currents, and compensation values is a crucial process. Typically, methodologies begin with a fixed circuit topology and aim to automate the determination of these optimal design variables, aligning with a prescribed cost function. Notably, two primary approaches have emerged for evaluating circuit performance: equation-based methods and simulation-based methods.

Equation-based analog optimization tools deploy analytical design equations to model the circuit performances of interest. These tools navigate the broad design space, promptly identifying viable designs by adhering to predefined performance constraints. The usefulness of equation-based methods enables the swift sifting through a large design space to procure an initial workable design. Nonetheless, the precision of such designs is frequently constrained. This limitation often arises from the necessity of simplifying the models to derive explicit performance evaluation equations, during which high-order effects may be neglected. Consequently, designs yielded by these methods generally necessitate further fine-tuning [20].

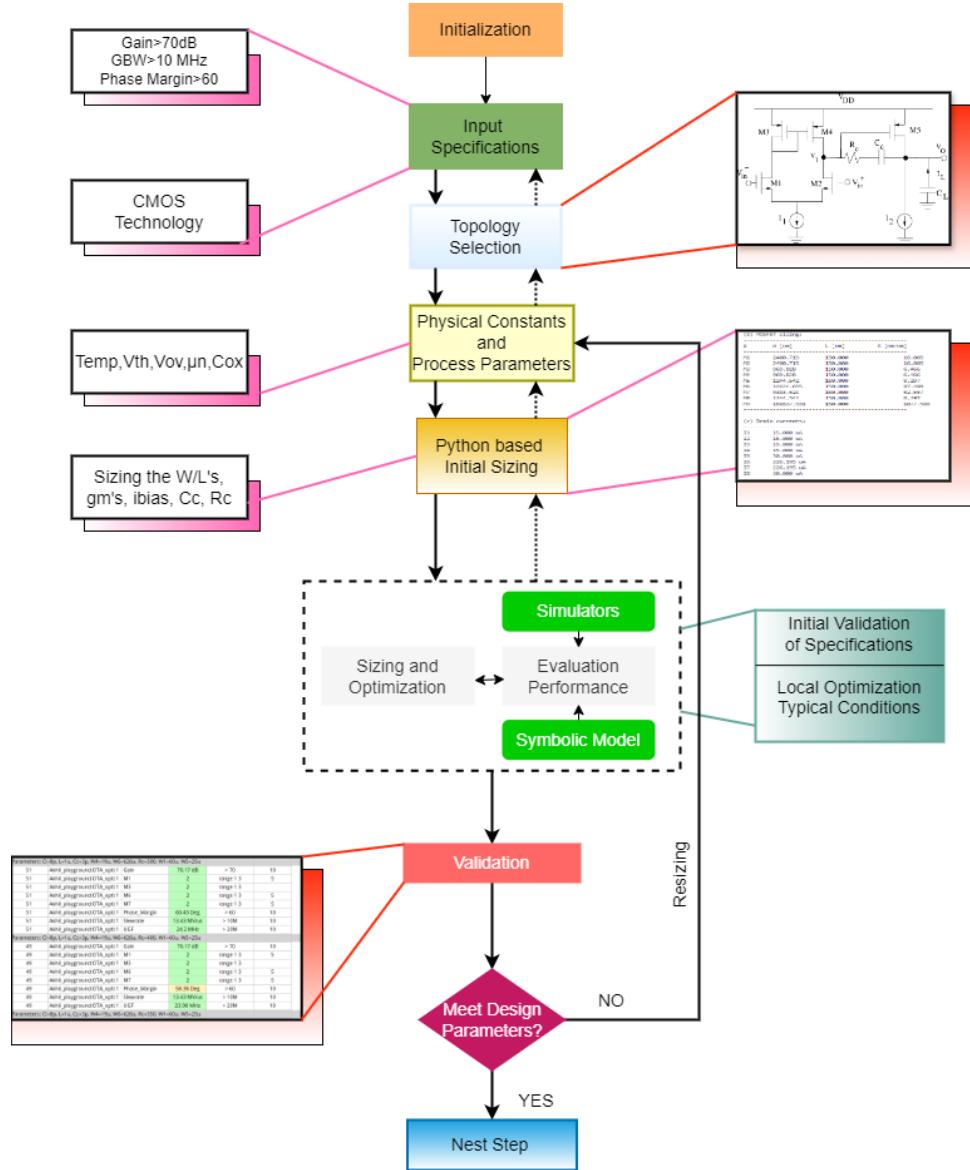


Figure 3.3: Proposed LDO Design methodology flow

To address this limitation and enhance design precision, a hybrid approach combining equation-based and simulation-based techniques appears to be employed in the proposed methodology. The initial sizing of transistors is performed using Python with the equation-based approach. This likely involves the application of square-law equations and other analytical formulas to estimate design variables. This step allows for rapid exploration of the design space and provides a preliminary parameter set.

After the initial sizing phase, simulation-based methods are utilized within the Cadence environment to refine the initial parameters. The simulation-based approach addresses non-idealities and complex interactions potentially overlooked by equation-based models. Through iterative local optimization, the design is fine-tuned until the desired performance is achieved.

By employing both methodologies, the design process benefits from the speed and efficiency provided by equation-based optimization, along with the enhanced accuracy and robustness provided by simulation-based validation and optimization.

This dual approach aims to quickly establish a promising starting point followed by refinement to meet the stringent performance criteria of the final LDO design.

3.2.2 Topology Selection

The process of achieving a high-performance design begins with the crucial step of selecting an appropriate architecture. This decision is guided by the specific design parameters, with the topology being chosen from a predefined library offering a specialized group of circuits with the required functionality. This careful, specification-driven selection lays the foundation for achieving optimal performance.

The proposed LDO architecture based on a two-stage error amplifier is shown in Figure 3.4. This circuit consists of three main components: an error amplifier (EA), a feedback network, and a PMOS pass transistor. The feedback network samples the output voltage V_{out} and feeds it to the positive input of the error amplifier. This amplifier compares the sampled voltage (feedback signal) with a reference voltage (V_{ref} , also denoted as V_{in}).

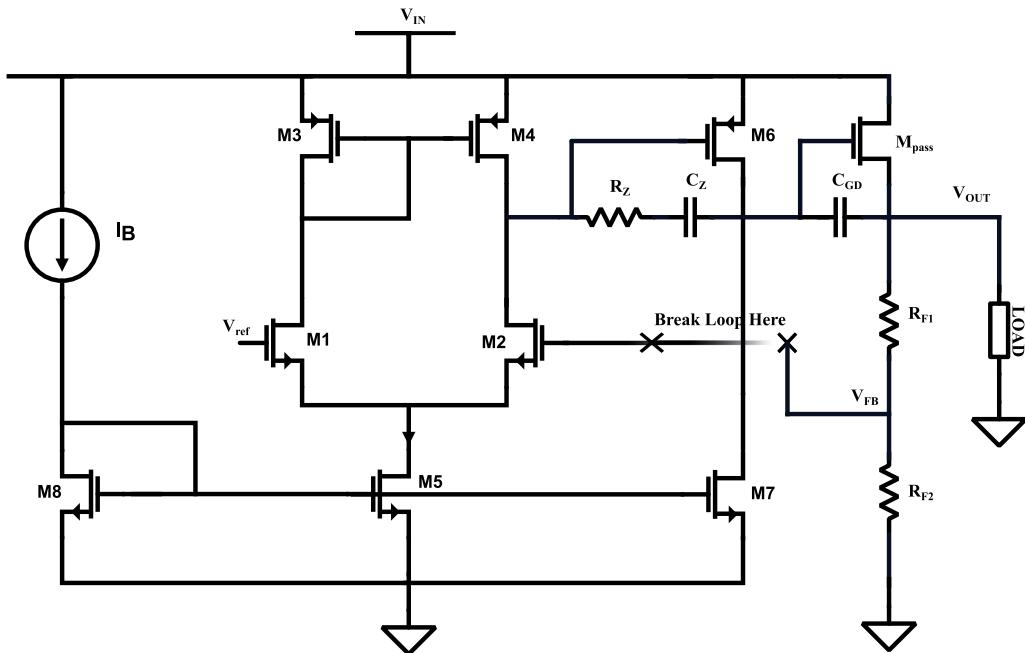


Figure 3.4: LDO Topology

3.2.3 Frequency Compensation

For proper operation, Low-Dropout regulators (LDOs) require compensation circuitry when dealing with circuits that have multiple poles within the unity-gain bandwidth (UGB). A compensation technique is necessary since the proposed LDO circuit possesses two movable poles.

3.2.4 Miller Compensation Technique

The proposed design utilizes Miller compensation, a common approach for LDO stabilization. This method involves introducing a capacitor between the output node

and the gate of the pass transistor. While Miller compensation effectively shifts one pole to a higher frequency and the other to a lower frequency, it also introduces a right-half plane (RHP) zero, potentially compromising circuit stability. A resistor can be incorporated into the compensation network to mitigate the negative impact of the RHP zero. By carefully tuning this resistor value, the zero can be moved to the left-hand side of the s-plane (LHP), restoring stability.

3.2.5 Small Signal Modeling

The feedback loop is disconnected between the node v_{FB} and the gate of transistor M2 as depicted in the LDO schematic. Consider v_S as the differential input voltage between the reference voltage v_{ref} and the feedback voltage v_{FB} . The open-loop small-signal representation from v_S to v_{FB} in our LDO design ensures that the first stage is non-inverting to maintain a non-inverting overall gain from v_{ref} to v_{OUT} [21]. The subsequent sections will articulate the small-signal parameters for our LDO topology. Here the equations for the small-signal parameters of the regulator of Figure 3.5 are given in Table 3.1. This table provides a succinct summary of the small-signal parameters pertinent to the LDO design, including transconductance for the specified MOSFETs and the related capacitances and resistances.

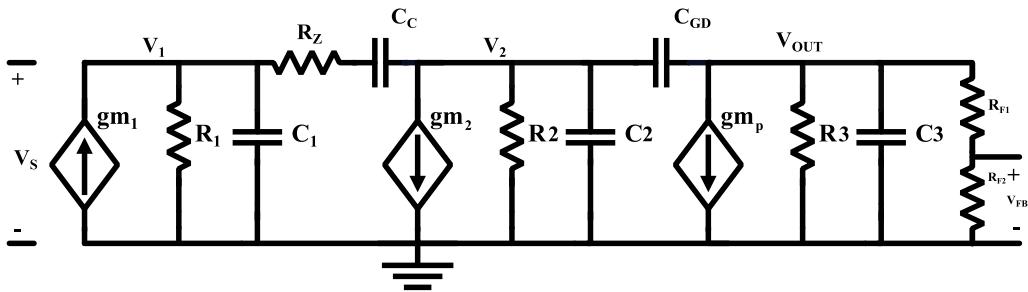


Figure 3.5: small signal model of the proposed LDO regulator

3.2.6 Applying Kirchhoff's Current Law (KCL)

KCL is applied at each node to analyze the circuit in Figure 3.5. The resulting equations are as follows:

$$eq1 = -g_{m1}v_S + \frac{v_1}{R_1} + v_1sC_1 + \frac{(v_1 - v_2)sC_c}{1 + sC_cR_Z} = 0 \quad (3.1)$$

$$eq2 = g_{m2}v_1 + \frac{v_2}{R_2} + \frac{(v_2 - v_1)sC_c}{1 + sC_cR_Z} + v_2sC_2 + (v_2 - v_{out})sC_{gd} = 0 \quad (3.2)$$

$$eq3 = g_{mp}v_2 + \frac{v_{out}}{R_3} + (v_{out} - v_2)sC_{gd} + v_{out}sC_3 + v_{out}sC_{out} = 0 \quad (3.3)$$

$$eq4 = v_{fb} - \frac{v_{out}R_{f2}}{R_{f1} + R_{f2}} = 0 \quad (3.4)$$

Table 3.1: Small-Signal Parameters

Parameter	Description
g_{m1}	Transconductance of M1
R_1	r_{o4}/r_{o2}
C_I	$C_{bd2} + C_{bd4} + C_{gs6} + C_{gd2} + C_{gd4}$
g_{m2}	Transconductance of M6
R_2	r_{o6}/r_{o7}
C_{II}	$C_{bd6} + C_{bd7} + C_{gd6} + C_{gd,pass}$
g_{mP}	Transconductance of M_{pass}
r_{oP}	Output resistance of M_{pass}
R_{OUT}	$r_{opass}/(R_{F1} + R_{F2})$
C_3	$C_{gd,pass} + C_{OUT} \approx C_{OUT}$

The open-loop DC loop gain A_{DC} of the regulator is a critical performance metric that quantifies the amplification within the feedback loop when it's open. A higher A_{DC} typically signifies better error correction and load regulation capability. It is calculated as Equation 3.5 where g_{m1} , g_{m2} , and g_{mP} are the transconductances of the first, second, and pass transistor stages respectively, and R_1 , R_2 , and R_3 are resistances within the circuit topology. Furthermore, the dominant pole ω_P1 , which has the lowest frequency, significantly impacts the regulator's stability and transient response. It is typically located at the output of the LDO's first stage and is determined by Equation 3.6. The second pole is due to the inner loop compensation network at the output of the error amplifier, given by 3.7.

$$|A_{DC}| = \frac{g_{m1} \cdot g_{m2} \cdot g_{mP} \cdot R_{o1} \cdot R_{o2} \cdot R_{out} \cdot R_2}{R_1 + R_2} \quad (3.5)$$

$$P_1 = \frac{1}{g_{m6}R_1R_2C_C + C_{gd}R_2R_3g_{m1} + C_3R_3} \quad (3.6)$$

$$P_2 = \frac{g_{m6}R_1R_2C_C + C_{gd}R_2R_3g_{m1} + C_3R_3}{C_C R_1 R_2 (C_3 R_3 g_{m6} + C_{gd} R_3 g_{m1} + C_1 + C_2)} \quad (3.7)$$

$$P_3 = \frac{C_3 R_3 g_{m1} + C_{gd} R_3 g_{m1} + C_3 R_3 g_{m1} + C_1 + C_2}{R_3 (C_1 C_{gd} R_2 g_{m1} + C_1 C_3 + C_2 C_3 + C_3 g_{m1})} \quad (3.8)$$

The circuit design generates two LHP zeros: one is introduced by the outer loop, the other by the inner loop depicted in equations 3.9, 3.10.

$$Z_1 = \frac{1}{2\pi \cdot C_{out} R_{ESR}} \quad (3.9)$$

$$Z_2 = \frac{1}{C_C \left(\frac{1}{g_{m6}} - R_Z \right)} \quad (3.10)$$

Equations (3.6) and (3.10) reveal that the LHP zero ω_{Z2} effectively cancels the effect of the second pole, ω_{P2} . This cancellation simplifies the transfer function and reduces the system's order. The remaining non-dominant pole, ω_{P3} , occurs at a significantly higher frequency beyond the bandwidth of interest (ω_{GBW}). Therefore, its influence on the regulator's response is negligible as shown in 3.6. For simplicity, the impact of higher-order poles and the right-half plane (RHP) zero arising from $C_{gd,PASS}$ is considered minimal and can be disregarded[21].

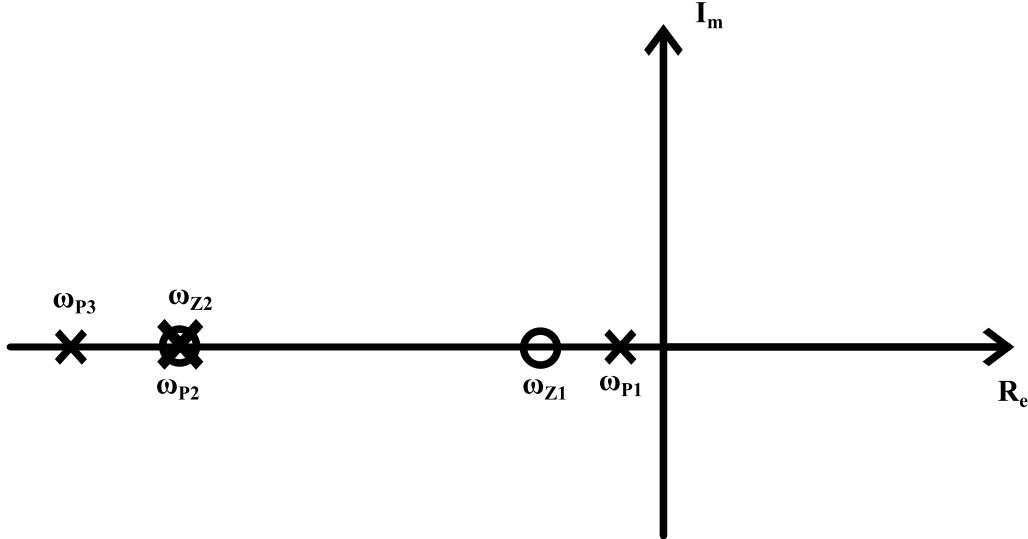


Figure 3.6: Pole Zero Location of the LDO regulator

3.3 Sizing Automation and Performance evaluation

This chapter addresses the challenges of traditional LDO regulator design by introducing a novel sizing automation algorithm. This hybrid approach combines the strengths of equation-based and simulation-based methods, providing a solution that improves both accuracy and efficiency throughout the iterative design process.

3.3.1 Initial Sizing with Python Automation

The foundation of our design algorithm is laid with an analytical sizing process that begins with user inputs and setup within a Python environment. Users specify operational parameters such as supply voltage, slew rate, load capacitance, and gain bandwidth product, which dictate the performance requisites of the LDO. The script then integrates these inputs with fundamental constants, like the Boltzmann constant, and technology-specific parameters, such as NMOS/PMOS threshold voltages, to form the substrate for subsequent sizing calculations. Utilizing the NumPy library, the script deftly executes complex mathematical operations to determine the optimal width-to-length (W/L) ratios of transistors, giving precedence to those nearest the output stage, thereby establishing a conducive starting point for the ensuing optimization process. It further extends into the realm of component selection, determining the required biasing resistors and compensation elements, both vital for the LDO's stability and dynamic performance.

3.3.2 Computation of Component Values and System Analysis

Having determined transistor sizes, the script progresses to calculate values for remaining passive components. The Python libraries play a key role here, allowing manipulation of algebraic expressions that represent these capacitors and resistors, which are crucial for the LDO's transient and frequency response. Furthermore, the script leverages symbolic algebra to establish the LDO's transfer function, enabling the derivation of critical performance metrics like DC loop gain and pole locations. Coupled with a control systems library, the algorithm generates insightful visualizations (e.g., Bode plots, and pole-zero maps) to assess the LDO's frequency response and stability margins.

This computation and analysis phase culminates in a comprehensive output, including transistor dimensions, currents, gain values, and pole locations. This data provides a clear picture of the interplay between design parameters and the targeted performance of the LDO.

3.3.3 Integration with Simulation Tool

Following the initial Python-based sizing, the calculated width-to-length (W/L) ratios and compensation values undergo rigorous evaluation in the Cadence environment. If these initial specifications don't fully satisfy the design criteria, Cadence's sophisticated local optimization algorithms are leveraged for fine-tuning. This optimization phase, explored in detail in the following chapter, refines the design parameters. The final LDO's performance is aligned precisely with the target specifications by strategically employing these optimization tools.

Chapter 4

Implementation Of Design Optimization Methodology

4.1 Introduction

This chapter delves into the implementation of our design optimization methodology. A two-stage Miller operational transconductance amplifier (OTA) is presented as a case study to showcase its effectiveness in identifying optimal solutions.

A critical aspect of our methodology is ensuring transistors operate within the saturation region. Table 4.1 summarizes the design specifications that establish this foundation. Equipped with these specifications, The methodology can be leveraged to achieve the targeted operational characteristics for the OTA design.

Table 4.1: Input Specifications for Design Optimization

Parameter	Description
V_{dd}	Positive supply voltage
V_{ss}	Negative supply voltage
SR	Slew Rate (the speed at which the output can change)
C_L	Load Capacitor (affects stability and transient response)
GBW	Gain Bandwidth Product (determines the frequency response)
ϕ	Phase Margin (ensures stability under varying conditions)

4.1.1 Design Procedure for Determining (W/L) Ratios

The predefined specifications detailed earlier serve as the foundation for calculating the width-to-length (W/L) ratios of the transistors. Referencing the circuit schematic shown in Figure 4.1, the (W/L) ratios for transistors M3 and M4 in the differential amplifier are determined based on the maximum Input Common-Mode Range Plus (ICMR+). For the NMOS transistors M1 and M2, part of the differential amplifier, their sizing is derived from the transconductance of M1 and the system's gain bandwidth.

The slew rate requirement influences the tail current through transistor M5, which also affects the sizing for M5 and M6 by utilizing $ICMR_-$. The compensation capacitance (CC) value is calculated in relation to this tail current, which establishes a bias voltage critical for achieving the desired phase margin[22].

For this two-stage operational amplifier, a minimum transistor length of $L \geq L_{min}$ is maintained to prevent the formation of an irregular gate geometry structure in the MOSFET. In our specific design, A gate length of $L \geq 2L_{min}$ is employed. This substantial gate length is strategically chosen to mitigate channel length modulation effects and reduce the influence of λ (lambda) on the drain and bias currents of M6.

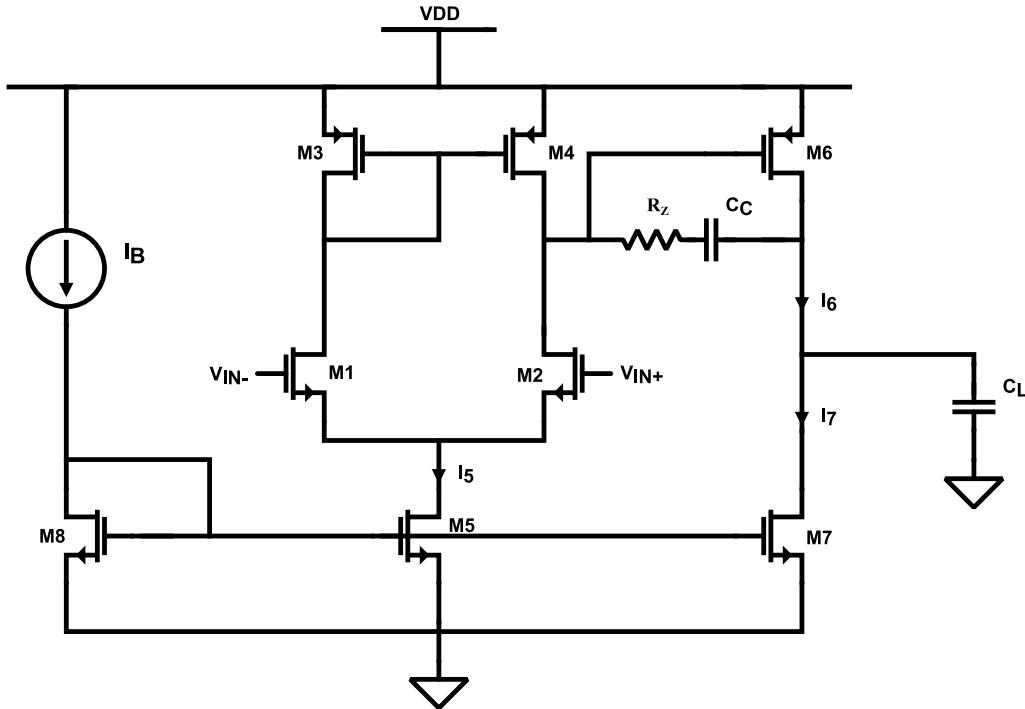


Figure 4.1: Two Stage Miller OTA

4.1.2 Implementation of the Design Algorithm

This subchapter focuses on the step-by-step implementation of the design optimization methodology previously introduced. Building on the specifications detailed in Table 4.1, The practical application of these parameters within our design framework is now addressed.

Design Steps:

Stability Optimization:

Calculation of the compensation capacitor (C_C) to ensure stability within the feedback loop for optimal amplifier performance.

Current and Transconductance Calculations:

Determining initial transconductance (gm_1) and current (I_5) for MOSFET 5, along with calculating the bias current (I_{bias}) and I_8 , ensuring proper current distribution (I_1 through I_4).

MOSFET Sizing:

Establishing form factors (gm_2 , S_1 , S_2) for MOSFETs 1 and 2, and calculating dimensions (L, W) for MOSFETs 3 and 4 based on their electrical behavior requirements.

Refinement with Interpolation:

In this phase, transistor configurations are refined by setting up voltages at each terminal based on the topology and sweeping the gate-source voltages (V_{gs}), ensuring operation in the saturation region. This setup is performed for all four types of transistors, including the input differential pair, where the body effect also plays a role. The approximate values are set at the bulk-source voltage (V_{BS}) terminal, and the drain-source voltage (V_{DS}) is set to half of the output voltage (V_{out}). For PMOS diode-connected pairs, the drain terminal is set to V_{DD} , and the gate-source voltage (V_{GS}) is adjusted to maintain saturation. Similarly, for the load common-source stage, proper biasing conditions are set for PMOS and NMOS transistors.

From these transistor setups, the width-to-length (W/L) ratios are determined according to the stage, with approximate values set at the input and output stages. This allows us to extract operating parameters such as transconductance (gm), output conductance (g_{ds}), drain current (I_d), gate capacitance (C_{gg}), and drain-source voltage (V_{DS}), along with the region of operation. These data are then imported into Python for further analysis.

Interpolating both the g_{ds}/I_d ratios and the gate capacitance (C_{gg}) ratios for key transistors, namely NMOS1, PMOS3, NMOS7, and PMOS6, is crucial. This interpolation allows us to accurately model channel length modulation, which directly affects transistor behavior in the saturation region. Precise interpolation of C_{gg} enables us to approximate node capacitance accurately within our Python simulations.

Unlike traditional approaches that rely solely on approximations, our use of the gm/I_d interpolation technique incorporates real, measured values. This significantly enhances the reliability and accuracy of our circuit models [23].

 V_{dsat} and Transconductance:

Calculating V_{dsat5} and adjusting S_5 and S_8 as necessary, determining gm_6 , S_6 , and I_6 , and setting the form factor and transconductance for MOSFET 7.

Final Performance Parameters:

Computing the compensation resistor R_Z for stability and total power dissipation. Calculating open-loop gains (Av_1 , Av_2) and resistances (R_1 , R_2). Determining pole frequencies and converting them to MHz.

Output and Documentation:

Converting currents, power, and capacitance to standardized units. Documenting all calculated parameters, including component values, MOSFET sizes, currents, gm values, resistances, power, gain, and pole frequencies. Providing comprehensive design data to validate the optimization methodology.

The Flowchart4.1 presented here illustrates the sequential progression of the design optimization algorithm.

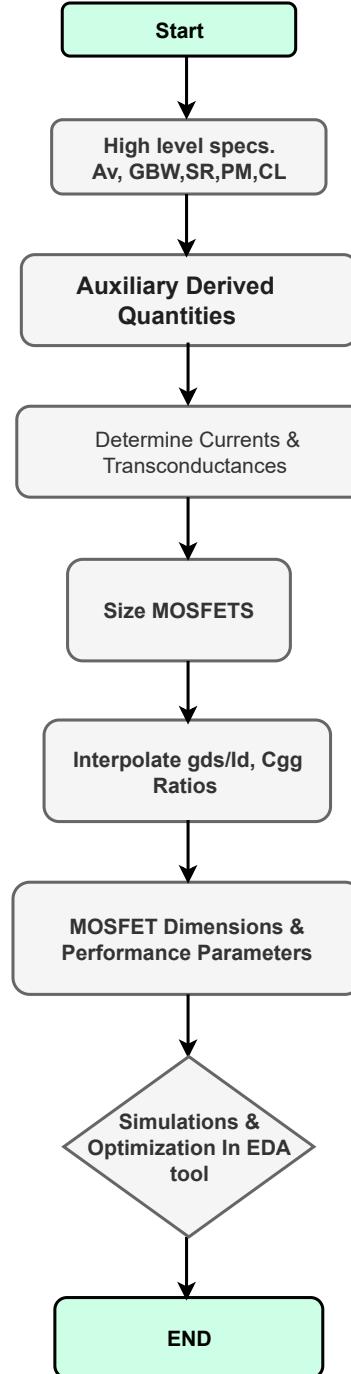


Figure 4.2: Design Steps

4.1.3 Design Example

This section elaborates on the Python-automated sizing and optimization process used in our design of the two-stage Miller Operational Transconductance Amplifier (OTA), which functions as an error amplifier for a Low-Dropout Regulator (LDO). Python scripts are utilized to integrate the predetermined user specifications, as detailed in Table 4.1, with interpolated values, facilitating the precision engineering of the OTA's critical design parameters. This approach underscores the synergy between computational power and human expertise in achieving optimized circuit functionality.

4.1.4 Example Output of Python Automation

In the appendix 8.3, comprehensive results from the Python-based automation process are presented. These results include the initial specifications, interpolated parameters necessary for precise circuit modeling, and final calculated values for various components within the two-stage Miller OTA design. This section aims to provide an exhaustive view of the design process, from initial values through the final implementation stages, underscoring our methodology's robustness and detail-oriented nature.

Initial Specifications: Voltage supplies, slew rate, load capacitance, gain bandwidth product, and phase margin. These parameters are critical as they determine the underlying behavior and functionality of the OTA.

Interpolated Parameters: Transconductance ratios and gate capacitances for critical transistors are crucial for ensuring operation within the saturation region.

Component Sizing and Electrical Characteristics Component values are meticulously calculated to meet design specifications:

MOSFET Sizing: Precise dimensions of width and length for each MOSFET ensure that they operate within the desired electrical parameters.

Drain Currents and Transconductance: Essential for defining the operational characteristics of the amplifier.

Resistances and Capacitances: These passive components are tuned to support the active elements in achieving the desired frequency response and stability.

Simulation Results The final section of the appendix covers the simulation results which validate our theoretical models:

Gain: Key performance indicators that assess the efficiency and amplification capability of the OTA.

Frequency Response: Includes dominant and non-dominant poles and zeros, providing insights into the stability and bandwidth of the amplifier.

These results are a testament to the effectiveness of our Python-based design automation and serve as a benchmark for further optimization and refinement in future design iterations.

4.1.5 Frequency Response Analysis in Python Automation

In the finalization stage of our two-stage Miller Operational Transconductance Amplifier (OTA) design, a comprehensive analysis of its frequency response and stability using control systems theory is paramount. This section presents the key findings

derived from nodal analysis equations and their validation against simulated results. Nodal analysis, represented by equations such as shown in Equations 4.1, 4.2.

$$eq1 = g_{m1} \cdot v_s + \left(\frac{v_1}{R_1} \right) + v_1 \cdot s \cdot C_1 + \left(\frac{v_1 - v_{out}}{1 + s \cdot C_c \cdot R_c} \right) \cdot s \cdot C_c = 0 \quad (4.1)$$

$$eq2 = g_{m6} \cdot v_1 + \left(\frac{v_{out}}{R_2} \right) + \left(\frac{v_{out} - v_1}{1 + s \cdot C_c \cdot R_c} \right) \cdot s \cdot C_c + v_{out} \cdot s \cdot C_2 = 0 \quad (4.2)$$

Frequency Response Analysis:

The frequency response of the OTA, depicted in the Bode plots generated through Python-based control systems analysis Figure 4.3, provides crucial insights into the system's behavior across various frequencies. The magnitude plot exhibits a robust and stable DC gain plateau at approximately 95.14 dB before the onset of gain roll-off, indicating the desired bandwidth of the amplifier.

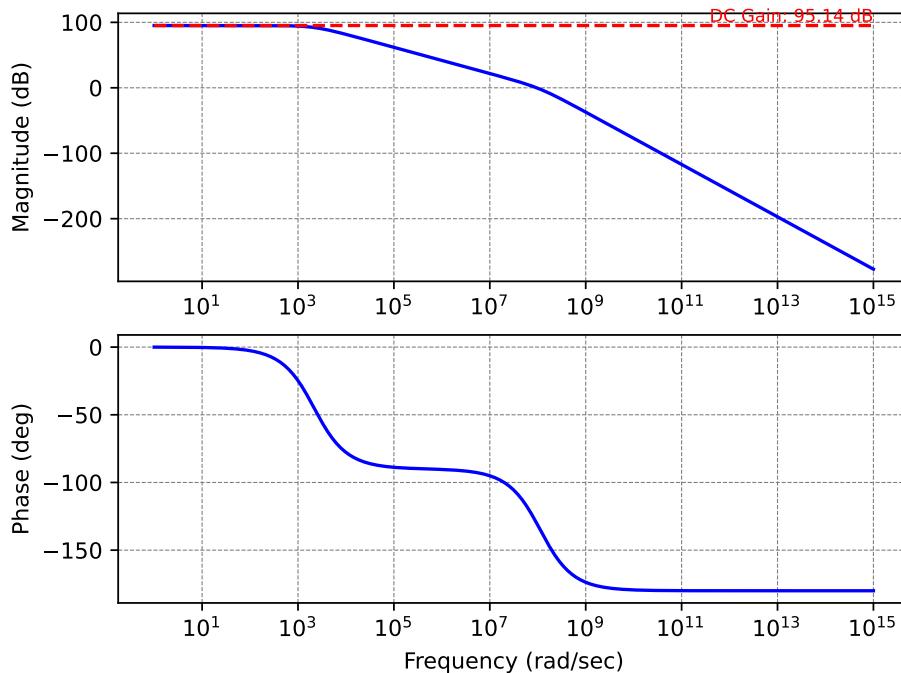


Figure 4.3: Bode Plot Of Two Stage Miller OTA

The phase margin, a significant stability indicator, is approximately 49.94 degrees at the unity gain frequency of about 94.88 MHz (94881761.63 rad/sec). This phase margin suggests a well-behaved system with sufficient buffer against oscillatory tendencies, aligning with our design objectives for a stable operational amplifier.

Further stability metrics were extracted using Python's control systems library:

```

1 # Calculate gain_margin, phase_margin,
2 and crossover_frequencies
3 gain_margin, phase_margin, gain_cross_freq,
4 phase_cross_freq = margin(H)

```

```

5
6 # Print the phase margin
7 print(f"Phase Margin:{phase_margin}
8 degrees at frequency {phase_cross_freq} rad/sec")

```

The unity gain frequency, or phase crossover frequency where the gain margin is measured, empirically validates the system's feedback stability. The design exhibits robustness under various operating conditions with a phase margin well above the often-recommended minimum of 45 degrees.

The phase plot reflects the anticipated phase shift across frequencies, which is crucial for maintaining signal timing integrity within the feedback loop. A gradual descent into a negative phase angle with increasing frequency is typical of such amplifier systems.

Stability Analysis:

The pole-zero map offers a clear visualization of the system's stability landscape. The placement of poles, indicated by 'X', within the left half-plane confirms system stability according to the Nyquist criterion. The absence of zeros, or 'O', in the critical right half-plane further supports this stable configuration Figure 4.4.

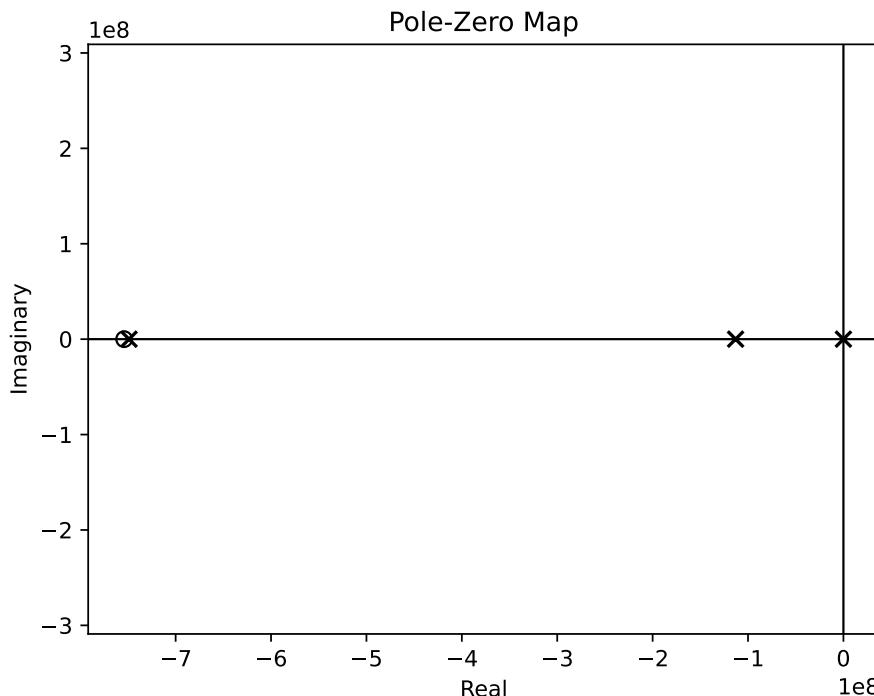


Figure 4.4: Pole Zero Of Two Stage Miller OTA

Preliminary Verification Through Frequency Response Estimation:

The initial validation involves estimating the frequency response, offering an initial insight into the operational characteristics, stability, and parameter precision of our OTA design. This step sets the stage for empirical verification, enabling parameter refinement for subsequent simulation phases.

Empirical Verification Via Cadence Simulations:

Comprehensive simulations using Cadence design tools were conducted to authenticate our theoretical calculations. The simulation outcomes provided empirical

evidence supporting our analytical predictions. The waveform outputs and pole-zero mappings obtained from Cadence simulations strongly aligned with our initial theoretical assessments. The agreement between the Bode plots and pole-zero configurations from both estimations and Cadence simulations validates the fidelity of our design process.

This systematic approach of analytical prediction followed by simulation-based confirmation underscores the reliability of our design. It demonstrates the OTA's ability to meet predefined specifications. The convergence of theoretical and simulation results lays a solid groundwork for detailed discussions on full simulation outcomes, which will be elaborated upon in the following section.

4.1.6 Optimization and Empirical Verification of OTA Design Parameters

The development of our two-stage Miller Operational Transconductance Amplifier (OTA) reaches a critical phase with the Python-based implementation of our sizing technique, as outlined in the Subsection 4.1.2. Here, the calculated width-to-length (W/L) ratios and compensation values are subjected to rigorous evaluation within the Cadence Virtuoso environment.

4.1.7 Initial Design Evaluation and Optimization

Upon reviewing the initial parameters and simulation results of our design, the following observations were made:

- The key parameters of the OTA, including gain, phase margin, and slew rate, were generally within acceptable limits. Specifically, the gain was measured at **71.06 dB**, the phase margin at **93.75 degrees**, and the slew rate at **9.849 MV/us**, all of which met or exceeded the design specifications.
- The unity gain frequency (UGF) was noted at **18.52 MHz**, which was close to the target range, suggesting a need for further optimization to refine the design.
- Transistor sizing parameters such as the width-to-length (W/L) ratios for M1, M3, M5, and M6 showed deviations from their intended values, indicating the necessity for more precise adjustments.

To bridge the gap between theoretical calculations and design objectives, Cadence's sophisticated local optimization algorithms were employed. This phase is crucial for fine-tuning the OTA's parameters to align precisely with our specifications regarding gain, phase margin, slew rate, and unity gain frequency. By introducing a 20% deviation around each parameter, a comprehensive exploration for potential improvements was facilitated. This systematic and iterative optimization ensures that the final design not only meets but surpasses initial operational targets, achieving an optimal balance between performance and stability.

The iterative nature of electronic design, where theoretical values serve as starting points, is highlighted through empirical testing and refinement, which ultimately leads to true design efficiency. This rigorous process aims to produce a reliable and optimized OTA that integrates seamlessly within a complex electronic system.

Output	Nominal	Spec	Weight	Pass/Fail
Gain	71.06 dB	> 70	10	pass
Phase_Margin	93.75 Deg	> 60	10	pass
slew rate	9.849 MV/us	< 11e6	10	pass
UGF	18.52 MHz	> 20e6	10	near
M1	3	range 1 3	5	near
M3	2	range 1 3	5	pass
M5	2	range 1 3	5	pass
M6	2	range 1 3	5	pass
M7	2	range 1 3	5	pass

Table 4.2: Two Stage Miller OTA Initial Verification

4.1.8 Comparison of Calculated and Simulated Values

Building on the optimization efforts, Next, the calculated and simulated values for key performance parameters and (W/L) ratios are compared. This comparison, shown in Table 4.3, is critical for validating the design methodology and ensuring that the OTA operates as intended under real-world conditions.

Parameter	Calculated	Simulated	Percentage Error
Gain	95.14 dB	71.06 dB	25.0%
Phase Margin	60 degrees	93.75 degrees	56.0%
Slew Rate	10 V/us	9.849 V/us	2.0%
UGF	20 MHz	18.52 MHz	7.0%
M1 (region)	2	3	50.0%
M3 (region)	2	2	0%
M5 (region)	2	2	0%
M6 (region)	2	2	0%
M7 (region)	2	2	0%

Table 4.3: Comparison of calculated and simulated values

This detailed analysis provides an initial reference value for evaluating the accuracy of our models and the effectiveness of the optimization algorithms used. The results serve as a foundation for further refinement and development in future design iterations, ensuring continual improvement in the performance and reliability of our OTA designs.

4.2 Selection Of Optimization Algorithm

4.2.1 Introduction to Optimization Algorithms

In modern electronics, analog integrated circuits have become indispensable in interfacing digital signal processing with real-world applications. However, due to the complex and nonlinear relationship between circuit performance and design variables, as well as the interdependence among these variables, manual circuit design relies heavily on the insights and experience of the designer. A successful design often necessitates both intuitive understanding and extensive parameter tuning, which is time-consuming.

To overcome the challenges inherent in manual design, various optimization methodologies have emerged to automate analog circuit design. These methodologies, starting from a fixed circuit topology, aim to identify the optimal design variables, such as transistor dimensions and bias currents, that align with a predefined cost function. Based on how they assess circuit performance, these methodologies can be categorized into equation-based and simulation-based approaches.

Equation-based methods leverage analytical equations or polynomial models to approximate the desired circuit characteristics, enabling a quick search through the design space for a viable solution. However, these approximations often require significant simplifications, which can compromise accuracy, necessitating further refinement through manual tuning.

In contrast, simulation-based methods utilize performance data from SPICE simulations to drive the optimization. Although these simulations provide accurate performance metrics, they are computationally intensive, which can limit the thorough exploration needed for global optimization.

In our methodology, these challenges are tackled by starting with initial parameter estimation using Python. The design then progresses to Cadence for verification through initial simulations based on these results. The design is refined further by employing local optimization within Cadence to achieve the desired parameters. This iterative process allows for fine-tuning and ensures the final design is accurate and optimized according to the specified requirements.

4.2.2 Application of the BFGS Algorithm in OTA Design Optimization

The Broyden-Fletcher-Goldfarb-Shanno (BFGS) algorithm is renowned for its efficacy in solving medium-scale unconstrained optimization problems [24]. This quasi-Newton method is especially favored due to its robust local and global convergence properties and its self-correcting capabilities, making it ideal for our application in optimizing operational transconductance amplifier (OTA) parameters.

Mathematical Foundation and OTA Design Optimization

The mathematical model for the BFGS algorithm involves minimizing a continuously differentiable function $f : \mathbb{R}^n \rightarrow \mathbb{R}$, where the solution process generates a sequence $\{x_k\}$, defined by the following equations [25].

$$x_{k+1} = x_k + \alpha_k d_k, \quad k = 0, 1, 2, \dots$$

Here, α_k represents the step size, and d_k is the search direction, given by:

$$d_k = -H_k g_k$$

where $H_k = B_k^{-1}$ and B_k updates according to:

$$B_{k+1} = B_k - \frac{B_k s_k s_k^T B_k}{s_k^T B_k s_k} + \frac{y_k y_k^T}{y_k^T s_k}$$

with initial conditions $B_0 = I$, $s_k = x_{k+1} - x_k$, and $y_k = \nabla f(x_{k+1}) - \nabla f(x_k)$.

In the context of OTA design, the BFGS algorithm is utilized to optimize critical design variables and performance parameters, enhancing the OTA's operational efficacy. The process involves:

- **Initialization:**

- Start with initial design variables x_0 , which include the (W/L) ratios of transistors (e.g., W_o/L_o), bias current (I_{DC}), compensation capacitor (C_C), and compensation resistor (R_C).
- Set the iteration counter $k = 0$.

- **Objective Function Evaluation:**

- Evaluate the objective function $f(x_k)$, which is derived from the key design parameters such as gain, unity gain frequency (UGF), slew rate, and phase margin.
- Calculate the gradient $\nabla f(x_k)$, representing the rate of change of the objective function with respect to the design variables.

- **Compute Search Direction:**

- Determine the search direction $d_k = -H_k g_k$, where H_k is the inverse Hessian approximation and g_k is the gradient at iteration k .

- **Line Search:**

- Perform a line search to find the optimal step size α_k that minimizes $f(x_k + \alpha_k d_k)$.

- **Update Design Variables:**

- Update the design variables: $x_{k+1} = x_k + \alpha_k d_k$.

- **Update Inverse Hessian:**

- Compute $s_k = x_{k+1} - x_k$ and $y_k = \nabla f(x_{k+1}) - \nabla f(x_k)$.
- Update the inverse Hessian approximation H_{k+1} using:

$$H_{k+1} = H_k - \frac{H_k s_k s_k^T H_k}{s_k^T H_k s_k} + \frac{y_k y_k^T}{y_k^T s_k}$$

- **Check Convergence:**

- If the magnitude of the gradient $\|\nabla f(x_{k+1})\|$ is below a predetermined tolerance, or if the maximum number of iterations is reached, stop the algorithm.
- Otherwise, increment k and return to step 2.

Implementation and Results: Initial guesses for (W/L) ratios, I_{DC} , C_C , and R_C are critical as they significantly influence the OTA's gain, UGF, slew rate, and phase margin.

Objective Function: The objective function encapsulates the OTA's performance metrics. It aims to minimize deviations from the target values of gain, UGF, slew rate, and phase margin.

Gradient Calculation and Search Direction: The gradient $\nabla f(x_k)$ is computed to understand how changes in the design variables affect the performance metrics. The search direction d_k is determined to move towards the optimal values.

Line Search and Variable Update: A line search determines the step size α_k for updating the design variables. This step ensures that each iteration brings the design closer to the desired performance.

Inverse Hessian Update: The inverse Hessian H_k is updated to refine the search direction in subsequent iterations. This self-correcting mechanism enhances the convergence rate.

Convergence Check: The algorithm iterates until the gradient magnitude is sufficiently small, indicating that the optimal design is achieved. The results demonstrate significant improvements in the OTA's key performance metrics.

By employing the BFGS algorithm, the OTA design was efficiently optimized, achieving the desired specifications for gain, UGF, slew rate, and phase margin. The iterative refinement process ensured that the final design met and exceeded the initial performance targets, demonstrating the algorithm's effectiveness in handling complex analog circuit optimization problems.

4.3 BFGS Algorithm Example in OTA Design Optimization

The outcome of the BFGS optimization provides a set of design variables setup, as shown in Appendix 8.3, that yields the best possible performance according to the defined criteria. By systematically adjusting the design parameters through this method, the OTA design is fine-tuned to achieve optimal functionality, demonstrating the benefits of integrating advanced optimization techniques in circuit design.

The use of local optimization highlights the iterative nature of electronic design. Theoretical values offer a starting point, but it's empirical testing and refinement that leads to true design efficiency. Through this rigorous process, the goal is to create a reliable and optimized OTA that seamlessly integrates within a complex electronic system.

The included figure (4.5) demonstrates the parameter analysis and compliance summary obtained using the BFGS optimization algorithm. It provides a detailed overview of the achieved values for critical parameters such as gain, phase margin, slew rate, and unity gain frequency (UGF), along with the corresponding design

Parameter Analysis with Local Optimization Summary

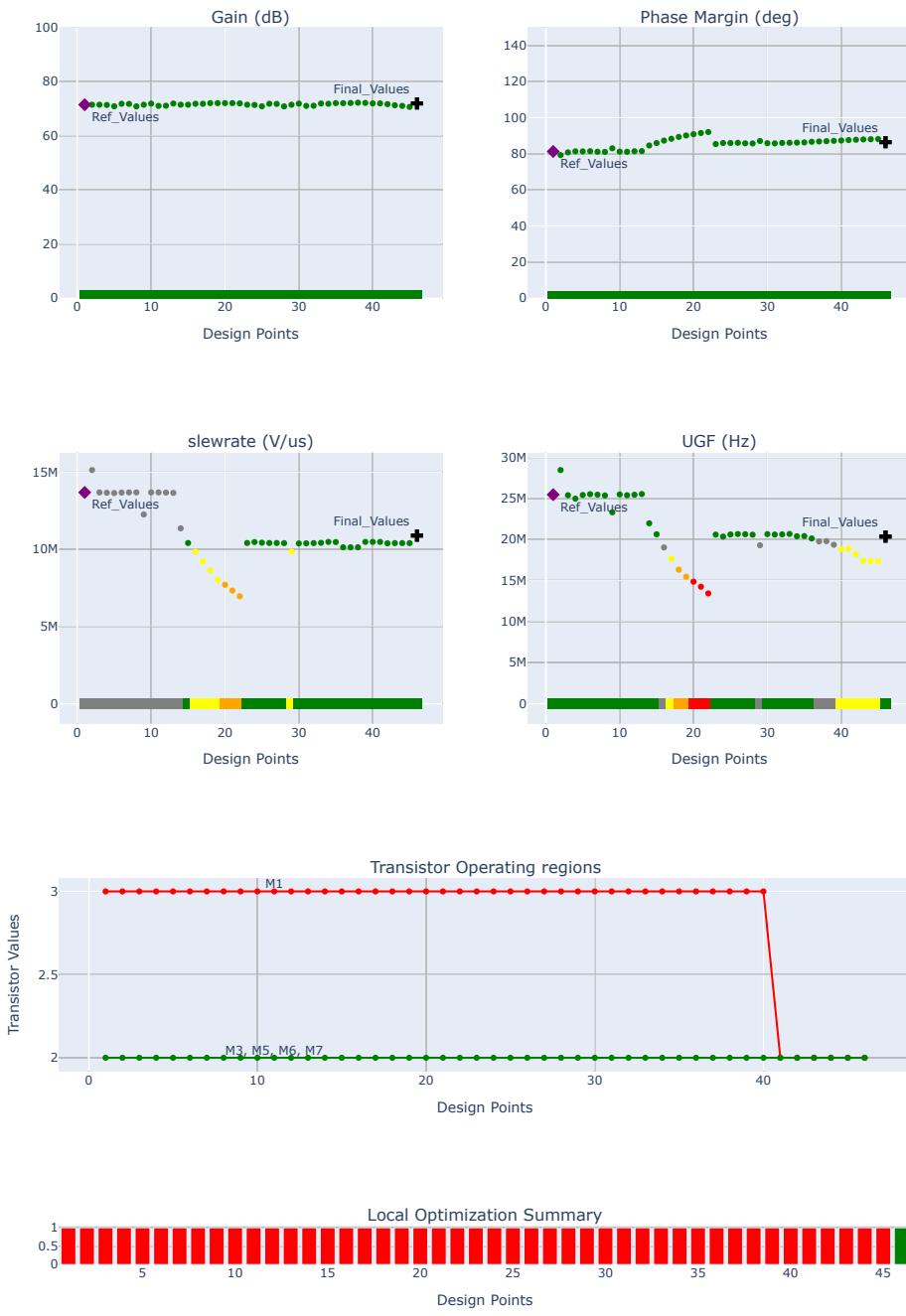


Figure 4.5: Parameter Analysis with Local Optimization Summary

variables. The analysis ensures that all specifications are met, validating the effectiveness of the BFGS algorithm in optimizing the OTA design. This visual representation underscores the successful alignment of theoretical and practical results, highlighting the robust performance and reliability of the optimized design.

This methodical approach to optimization not only streamlines the design process but also ensures that the OTA operates within the desired specifications, effectively enhancing both performance and reliability.

Conclusion

By leveraging the BFGS algorithm, a refined design was achieved faster and more effectively than traditional optimization methods, which often require manual tuning and extensive simulation runs. The algorithm's ability to adaptively update its search direction and step size based on the landscape of the objective function significantly reduced the number of iterations needed to reach the desired accuracy and stability in the OTA's performance.

4.3.1 Application of the Conjugate Gradient Method in OTA Design Optimization

The Conjugate Gradient (CG) method is an iterative algorithm used for solving large-scale systems of linear equations. It is particularly effective for sparse systems and is a popular choice for optimization problems due to its efficient handling of large data sets. In the context of operational transconductance amplifier (OTA) design, the CG method helps optimize the design parameters to meet the desired performance criteria.

Mathematical Foundation and OTA Design Optimization

The CG method aims to minimize a quadratic objective function $f(x)$ defined as:

$$f(x) = \frac{1}{2}x^T Ax - b^T x$$

where A is a symmetric positive-definite matrix, x is the vector of design variables, and b is a constant vector. The iterative process generates a sequence of approximations $\{x_k\}$ that converges to the optimal solution.

The update rule for the CG method is:

$$x_{k+1} = x_k + \alpha_k p_k$$

where α_k is the step size and p_k is the search direction. The search direction is updated as:

$$p_{k+1} = r_{k+1} + \beta_k p_k$$

with the residual $r_k = b - Ax_k$ and β_k calculated as:

$$\beta_k = \frac{r_{k+1}^T r_{k+1}}{r_k^T r_k}$$

In the OTA design, the CG method is applied to optimize critical design variables such as (W/L) ratios, bias currents (I_{DC}), compensation capacitors (C_C), and

resistors (R_C). The goal is to enhance performance parameters like gain, unity gain frequency (UGF), slew rate, and phase margin.

- **Initialization:**

- Start with initial design variables x_0 , including (W/L) ratios (e.g., W_o/L_o), bias current (I_{DC}), compensation capacitor (C_C), and resistor (R_C).
- Set the initial residual $r_0 = b - Ax_0$ and the initial search direction $p_0 = r_0$.

- **Iteration Process:**

- Compute the step size $\alpha_k = \frac{r_k^T r_k}{p_k^T A p_k}$.
- Update the design variables: $x_{k+1} = x_k + \alpha_k p_k$.
- Update the residual: $r_{k+1} = r_k - \alpha_k A p_k$.
- Compute the new search direction: $\beta_k = \frac{r_{k+1}^T r_{k+1}}{r_k^T r_k}$.
- Update the search direction: $p_{k+1} = r_{k+1} + \beta_k p_k$.
- Increment k and repeat until convergence criteria are met.

- **Convergence Check:**

- If $\|r_k\|$ is below a predefined tolerance or the maximum number of iterations is reached, the algorithm stops.
- Otherwise, continue the iteration process.

Implementation and Results

Initialization: Initial estimates for (W/L) ratios, I_{DC} , C_C , and R_C are established. These initial guesses are critical as they influence the OTA's key performance metrics.

Objective Function: The objective function is formulated based on the desired OTA performance metrics, aiming to minimize deviations from target values of gain, UGF, slew rate, and phase margin.

Iteration Process: The CG method iteratively refines the design variables, with each iteration moving closer to the optimal solution by updating the design variables and search directions based on computed residuals.

Convergence Check: The algorithm continues iterating until the residual is sufficiently small, indicating that the design variables have converged to the optimal values. The results show significant improvements in the OTA's performance metrics.

Using the CG method, the OTA design was optimized efficiently, meeting the desired specifications for gain, UGF, slew rate, and phase margin. The iterative process ensured that the final design not only met but exceeded the initial performance targets, demonstrating the effectiveness of the CG method in optimizing complex analog circuit designs.

The included figure (4.6) demonstrates the parameter analysis and local optimization summary obtained using the Conjugate Gradient optimization algorithm. It provides a detailed overview of the achieved values for critical parameters such

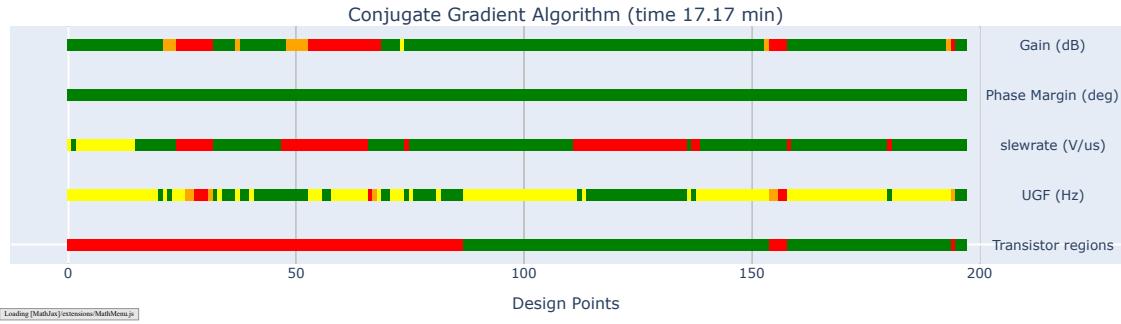


Figure 4.6: Parameter Analysis with Conjugate Gradient Algorithm Summary

as gain, phase margin, slew rate, and unity gain frequency (UGF), along with the corresponding design variables. The analysis ensures that all specifications are met, validating the effectiveness of the Conjugate Gradient algorithm in optimizing the OTA design. This visual representation underscores the successful alignment of theoretical and practical results, highlighting the robust performance and reliability of the optimized design.

Resulting Optimized Design

The outcome of the CG optimization provides a set of design variables that yield the best possible performance according to the defined criteria. By systematically adjusting the design parameters through this method, the OTA design is fine-tuned to achieve optimal functionality, demonstrating the benefits of integrating advanced optimization techniques in circuit design.

Conclusion

Using the CG method, the OTA design was efficiently optimized, meeting the desired specifications for gain, UGF, slew rate, and phase margin. The iterative process ensured that the final design not only met but exceeded the initial performance targets, demonstrating the effectiveness of the CG method in optimizing complex analog circuit designs. By leveraging the CG method, a refined design was achieved faster and more effectively compared to traditional optimization methods, which often require manual tuning and extensive simulation runs.

4.3.2 Application of the Brent-Powell Algorithm in OTA Design Optimization

The Brent-Powell (BP) algorithm is utilized for optimizing the operational transconductance amplifier (OTA) design parameters. This method effectively combines the Brent-Powell conjugate direction method with Brent's line search algorithm to achieve precise minimization of the objective function. The BP algorithm is beneficial for its ability to perform exact line minimization, enhancing the accuracy and efficiency of the optimization process.

Mathematical Foundation and Relevance

Powell's algorithm searches for a local minimum of an objective function for a set of linearly independent direction vectors without calculating the derivatives. It is known as one of the conjugate direction methods. The strategy of Powell's method is summarized as follows:

Given linearly independent vectors d_0, \dots, d_{n-1} and a starting point x_0 for an n -dimensional objective function, the goal is to find the minimum for each direction vector $i = 0, 1, \dots, n-1$ [26]:

$$x_{i+1} = x_i + \alpha_i d_i$$

where α_i can be determined by the line-search algorithm. After finding x_n for direction d_n , the $n+1$ -th direction vector is defined as:

$$d_n = x_n - x_0$$

Then, find x_{n+1} for direction d_n . After discarding d_0 and setting $x_0 = x_{n+1}$, the process is repeated until:

$$\|x_{n+1} - x_0\| = 0$$

Brent-Powell method is employed through two core procedures: bracketing and line-search.

OTA Design Optimization Using the Brent-Powell Algorithm

In the context of OTA design, the BP algorithm optimizes critical design variables such as (W/L) ratios, bias currents (I_{DC}), compensation capacitors (C_C), and compensation resistors (R_C). The goal is to enhance performance parameters like gain, unity gain frequency (UGF), slew rate, and phase margin.

- **Initialization:**

- Start with initial design variables μ_0 , which include (W/L) ratios (e.g., W_o/L_o), bias current (I_{DC}), compensation capacitor (C_C), and compensation resistor (R_C).
- Set the initial directions d_i (for $i = 1, 2, 3, 4$).

- **Line Search Optimization:**

- Perform an exact line search along each direction d_i using Brent's method to find the optimal step size α_i that minimizes the cost function.
- Update the design variables: $\mu_{k+1} = \mu_k + \alpha_i d_i$.

- **Direction Update:**

- Compute the new direction: $d = -\mu_{k+1} + \mu_k$.
- Set the new direction for the next iteration: $d_i = d$ for $i = 2, 3, 4, 5$.

- **Convergence Check:**

- If the Euclidean distance $\|\mu_{k+1} - \mu_k\|$ is less than a predefined threshold ϵ , the algorithm converges and stops.
- Otherwise, repeat the line search optimization and direction update steps.

Implementation and Results

Initialization: Initial estimates for (W/L) ratios, I_{DC} , C_C , and R_C are determined. These initial guesses are critical as they influence the OTA's key performance metrics.

Line Search Optimization: The BP algorithm performs exact line minimization along specified directions to find the optimal step sizes. This ensures that each iteration moves the design variables closer to the optimal solution.

Direction Update: The directions are updated iteratively to maintain orthogonality and improve convergence. The new directions are set based on the difference between the current and previous design variables.

Convergence Check: The algorithm continues iterating until the Euclidean distance between consecutive design variables is sufficiently small, indicating that the design has converged to the optimal solution. The results show significant improvements in the OTA's performance metrics.

Resulting Optimized Design

The outcome of the BP optimization provides a set of design variables that yield the best possible performance according to the defined criteria. By systematically adjusting the design parameters through this method, the OTA design is fine-tuned to achieve optimal functionality, demonstrating the benefits of integrating advanced optimization techniques in circuit design.

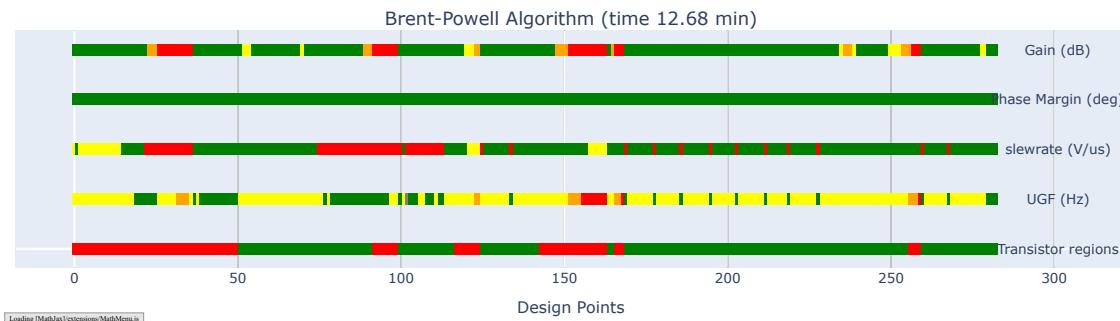


Figure 4.7: Parameter Analysis with Brent-Powell Optimization Summary

The included figure (4.7) demonstrates the parameter analysis and compliance summary obtained using the Brent-Powell optimization algorithm. It provides a detailed overview of the achieved values for critical parameters such as gain, phase margin, slew rate, and unity gain frequency (UGF), along with the corresponding design variables. The analysis ensures that all specifications are met, validating the effectiveness of the Brent-Powell algorithm in optimizing the OTA design. This visual representation underscores the successful alignment of theoretical and practical results, highlighting the robust performance and reliability of the optimized design.

4.3.3 Application of the Hooke-Jeeves Algorithm in OTA Design Optimization

The Hooke-Jeeves algorithm is an iterative method used for optimizing the design parameters of an operational transconductance amplifier (OTA). This algorithm

performs two types of search: exploratory search and pattern search, making it effective in finding local minima without the need for gradient information.

Mathematical Foundation and Relevance

The Hooke-Jeeves algorithm can be summarized as follows:

1. Initialization:

- Choose an initial point x_0 and a step size Δ .
- Set $k = 0$.

2. Exploratory Search:

- Perform a search along each coordinate direction from the current point x_k to find a new point x_{k+1} .
- For each direction d_i , update the point:

$$x_{k+1} = x_k + \Delta d_i$$

- If no improvement is found, reduce the step size Δ and repeat the search.

3. Pattern Search:

- Once an improved point x_{k+1} is found, define the pattern direction as:

$$p_k = x_{k+1} - x_k$$

- Perform a search along the pattern direction to find a new point y :

$$y = x_{k+1} + \lambda p_k$$

where λ is a scalar determined by a line search.

4. Iteration:

- Set $x_{k+2} = y$ and update k .
- Repeat the exploratory and pattern searches until convergence is achieved.
- Convergence is determined when the step size Δ is sufficiently small or no significant improvement is found.

OTA Design Optimization Using the Hooke-Jeeves Algorithm

In the context of OTA design, the Hooke-Jeeves algorithm optimizes critical design variables such as (W/L) ratios, bias currents (I_{DC}), compensation capacitors (C_C), and compensation resistors (R_C). The aim is to enhance performance parameters like gain, unity gain frequency (UGF), slew rate, and phase margin.

- **Initialization:**

- Start with initial design variables x_0 , which include the (W/L) ratios of transistors (e.g., W_o/L_o), bias current (I_{DC}), compensation capacitor (C_C), and compensation resistor (R_C).
- Set the step size Δ and the iteration counter $k = 0$.

- **Exploratory Search:**

- Perform a search along each coordinate direction from the current point x_k to find a new point x_{k+1} .
- Update x_{k+1} as:

$$x_{k+1} = x_k + \Delta d_i$$

- **Pattern Search:**

- Once an improved point x_{k+1} is found, define the pattern direction:

$$p_k = x_{k+1} - x_k$$

- Perform a search along the pattern direction to find a new point y :

$$y = x_{k+1} + \lambda p_k$$

- **Iteration:**

- Set $x_{k+2} = y$ and update k .
- Repeat the exploratory and pattern searches until convergence is achieved.

Implementation and Results

Initialization: Begin with initial guesses for (W/L) ratios, I_{DC} , C_C , and R_C . These values are critical as they influence the OTA's gain, UGF, slew rate, and phase margin.

Objective Function: The objective function encapsulates the OTA's performance metrics. It aims to minimize deviations from the target values of gain, UGF, slew rate, and phase margin.

Exploratory and Pattern Searches: Through these searches, the algorithm iteratively improves the design parameters to achieve optimal performance. The process is repeated until the step size Δ is sufficiently small or no significant improvement is found.

Convergence Check: The algorithm iterates until the convergence criteria are met. The results demonstrate significant improvements in the OTA's key performance metrics.

The Hooke-Jeeves algorithm was employed to efficiently optimize the OTA design, achieving the desired specifications for gain, UGF, slew rate, and phase margin. The iterative refinement process ensured that the final design not only met but exceeded the initial performance targets, demonstrating the algorithm's effectiveness in handling complex analog circuit optimization problems.

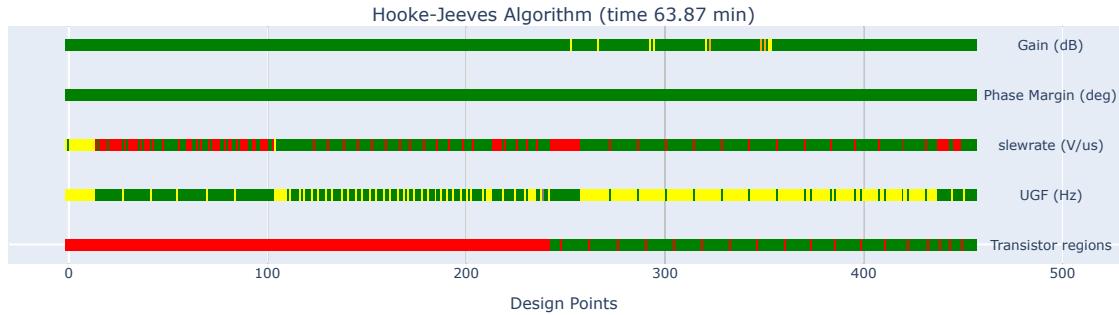


Figure 4.8: Parameter Analysis with Hooke-Jeeves Optimization Summary

4.4 Conclusion

In this chapter, the application of various optimization algorithms for designing operational transconductance amplifiers (OTA) was explored. The algorithms tested included the Broyden-Fletcher-Goldfarb-Shanno (BFGS) algorithm, the Conjugate Gradient (CG) method, the Brent-Powell algorithm, and the Hooke-Jeeves algorithm. These algorithms were applied to three different design cases to optimize key performance parameters of the OTA, such as gain, slew rate (SR), load capacitance (Cl), gain bandwidth (GB), and phase margin (Phi). The specific (W/L) ratios and compensation values used in these designs are detailed in Appendix 8.3 and Table 8.1.

The following table summarizes the specifications for the three design cases:

Parameter	Design 1	Design 2	Design 3
Gain	> 70 dB	> 70 dB	> 70 dB
Slew Rate (SR)	10e6 V/s	30e6 V/s	40e6 V/s
Load Capacitance (Cl)	1p F	5p F	3p F
Gain Bandwidth (GB)	20e5 Hz	50e6 Hz	75e6 Hz
Phase Margin (Phi)	60 deg	> 60 deg	> 55 deg

Table 4.4: Specifications for Design Cases 1, 2, and 3

4.4.1 Comparison of Optimization Algorithms

BFGS Algorithm: The BFGS algorithm demonstrated robust local and global convergence, providing a refined design that met and exceeded the performance targets for gain, UGF, slew rate, and phase margin. The algorithm's self-correcting mechanism and efficient handling of the Hessian matrix updates made it a strong candidate for OTA optimization.

Conjugate Gradient Method: The CG method effectively optimized the OTA design by iteratively refining the design variables. The method was particularly efficient for handling large data sets and sparse systems, making it suitable for OTA design with complex parameter interdependencies.

Brent-Powell Algorithm: The BP algorithm combined Brent's line search with Powell's conjugate direction method to perform precise line minimization. This approach ensured exact minimization along each search direction, resulting in accurate and efficient optimization of the OTA parameters.

Hooke-Jeeves Algorithm: The Hooke-Jeeves algorithm utilized exploratory and pattern searches to optimize the OTA design without requiring gradient information. The algorithm's iterative refinement process proved effective in finding local minima and enhancing the OTA's performance metrics.



Figure 4.9: Parameter Analysis Across Algorithms for Design 2



Figure 4.10: Parameter Analysis Across Algorithms for Design 3

The figures 4.9 and 4.10 included above provide a comparative overview of the parameter analysis across different optimization algorithms for Design Cases 2 and 3. These visualizations further validate the effectiveness of the optimization approaches discussed in this chapter and underscore the potential for applying advanced optimization techniques in analog circuit design.

Based on the comparative analysis of these optimization algorithms, the BFGS algorithm emerged as the most effective method for OTA design optimization due to its robust convergence properties and ability to handle complex design parameter interactions. The inclusion of design case studies highlighted the practical applicability and performance improvements achievable with each algorithm.

In future work, The focus will be on applying the BFGS algorithm to optimize the design methodology of Low-Dropout (LDO) regulators. This will involve leveraging the insights gained from OTA design optimization to enhance the performance and efficiency of LDO designs.

4.4.2 Design Flow

The design methodology for the LDO is outlined in the flowchart shown in Figure 4.11. The process is structured as follows:

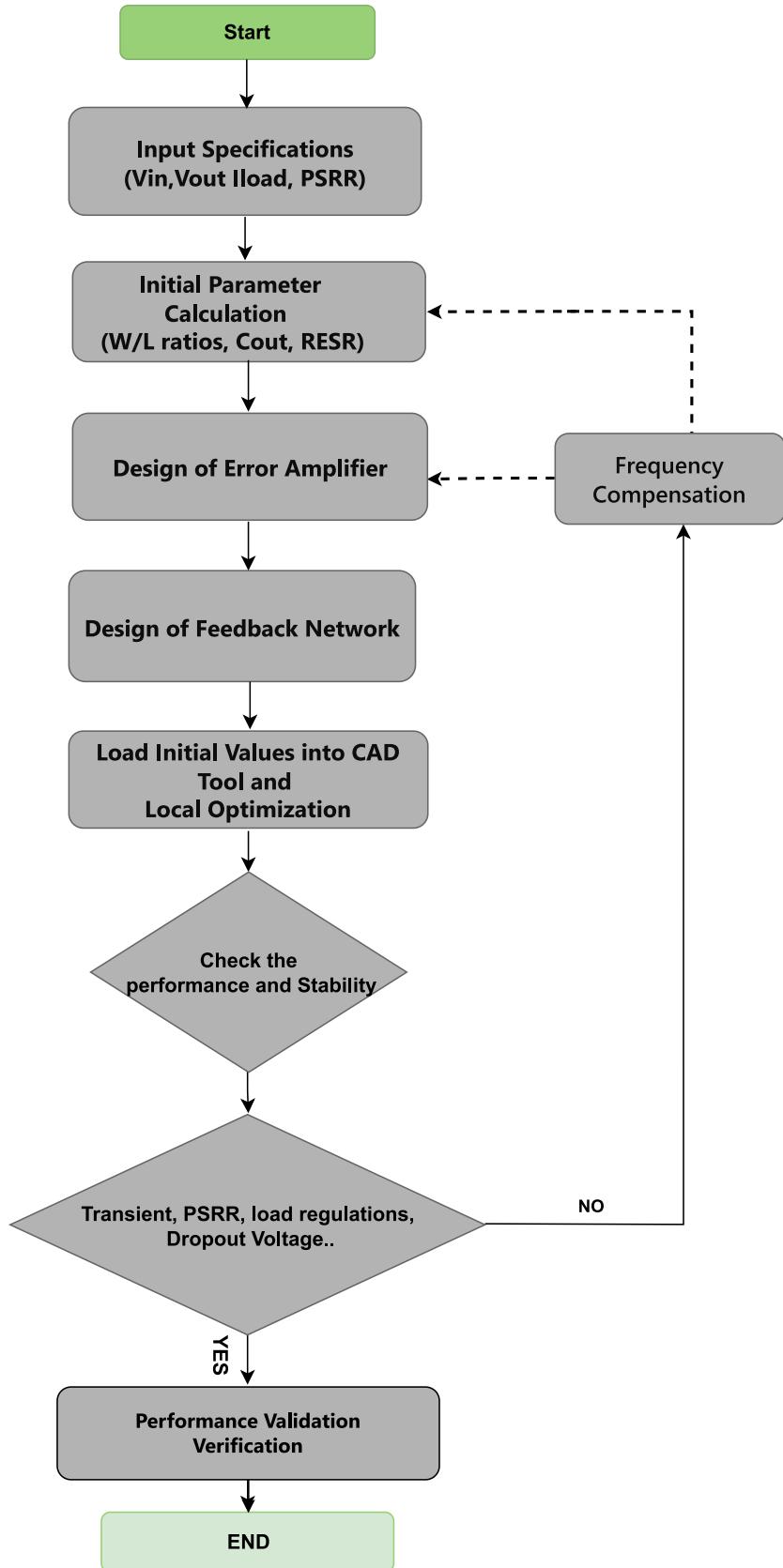


Figure 4.11: LDO Design Methodology Flowchart

4.5 Pass Element Design

The selection of the pass element is crucial for achieving high efficiency and low dropout voltage in Low-Dropout (LDO) regulators. The size of the pass transistor is a critical factor; a larger pass transistor typically lowers the dropout voltage for a given output current. However, as the load current specification increases, the transistor must be correspondingly larger. This increase in size leads to higher gate capacitance, complicating the fulfillment of stability and slew rate requirements. Additionally, a larger transistor size leads to increased quiescent current consumption, which can reduce current efficiency.

In the design discussed here, a PMOS pass transistor in a common-source configuration is utilized, as depicted in Figure 4.12. While a PMOS pass transistor offers certain advantages, it typically lacks high drive capability. Therefore, it must be sufficiently large to satisfy both the load current and dropout voltage specifications, but not so large as to adversely affect the power supply rejection ratio (PSRR) at higher frequencies.

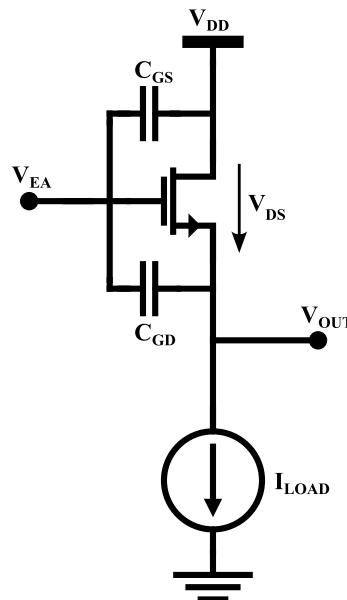


Figure 4.12: PMOS pass transistor

The output impedance of the pass transistor inversely correlates with the current flowing through it, affecting the position of the dominant pole. The dominant pole, primarily determined by the output capacitor and the output impedance of the pass transistor, is described by Equation 4.5:

$$f_{P1} = \frac{1}{2\pi C_{out} R_{o-pass}} \approx \frac{\lambda I_{load}}{2\pi C_{out}}$$

where λ represents the channel length modulation parameter. The position of the dominant pole moves higher with increasing load current, affecting the unity gain frequency (UGF). Conversely, an increase in gate capacitance shifts the location of the parasitic pole to lower frequencies, which can degrade the phase margin and potentially compromise stability. The output current when the transistor is in the

saturation region is modeled by Equation 4.5:

$$I_{sd} \approx \frac{K_P}{2} \left(\frac{W}{L} \right) (V_{sg} - V_{th})^2$$

where K_P and $\frac{W}{L}$ denote the transconductance parameter and the aspect ratio of the PMOS transistor, respectively.

The design of the PMOS pass transistor is guided by the load current specifications, ensuring that the (W/L) ratios are optimized to provide sufficient drive capability while minimizing dropout voltage. This approach enhances the LDO's PSRR and maintains efficiency. The error amplifier, which will be detailed in the further section, is designed to complement the characteristics of the pass transistor, ensuring stability and optimal performance across varying load conditions.

4.6 Error Amplifier Design

The design of the error amplifier is critical for achieving the desired performance characteristics of a Low-Dropout (LDO) regulator. Key specifications for the error amplifier include high DC gain for improved accuracy, excellent load and line regulation, and high rail-to-rail output capabilities to ensure proper control over the PMOS pass transistor. Additionally, the amplifier must position internal poles at frequencies significantly higher than the crossover loop frequency, while maintaining low quiescent current and sufficient output current capacity to swiftly charge the gate capacitance of the power device, thereby reducing both slew rate and settling time[14].

Achieving high DC gain with a single-stage amplifier is challenging, necessitating the adoption of a two-stage amplifier topology shown in Figure 4.13 to meet gain requirements effectively. Ideally, a cascode operational amplifier could maximize bandwidth for a given gain. However, the constraints imposed by a low supply voltage necessitate a simpler approach. Consequently, the chosen circuit design comprises a differential pair followed by a common source stage [27]. This topology eschews cascodes, opting to establish well-defined bias currents for both stages, thus providing a robust and reliable solution. The configuration ensures the error amplifier can deliver the performance needed to control the LDO effectively under varying electrical conditions.

As mentioned in Chapter 4, the detailed process of OTA optimization using different optimization algorithms in Cadence Virtuoso has been thoroughly explained. This includes the application of algorithms such as BFGS, Conjugate Gradient, Brent-Powell, and Hooke-Jeeves to optimize the design parameters of the OTA, ensuring the LDO meets the stringent performance specifications required for modern portable and battery-supplied applications.

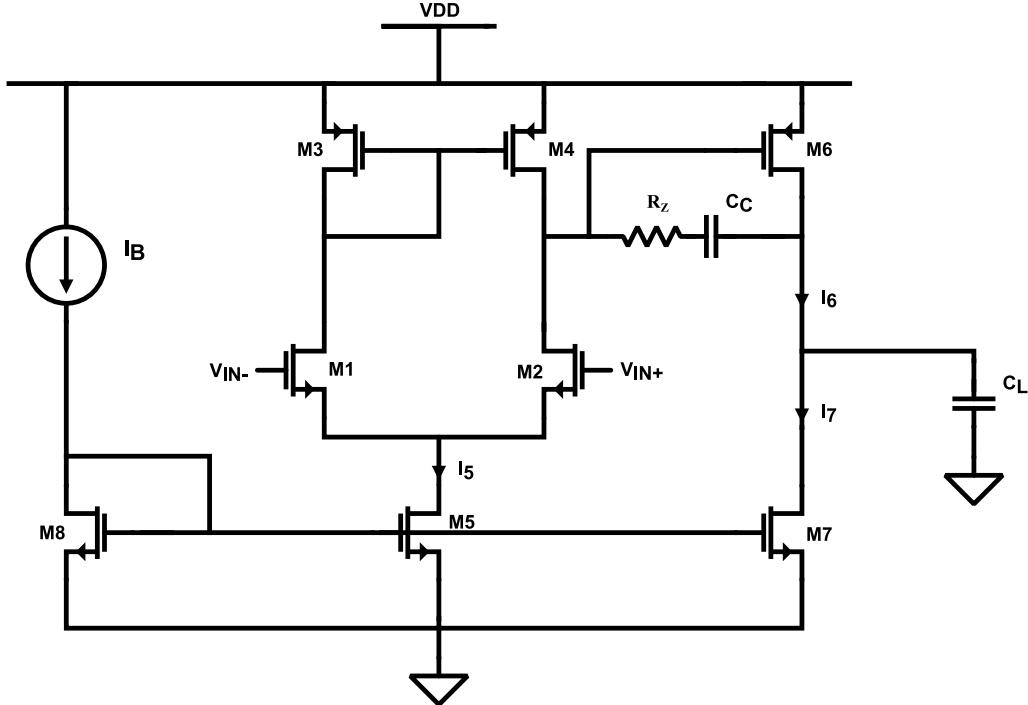


Figure 4.13: Two Stage Miller OTA

4.6.1 LDO Design

The Low-Dropout (LDO) regulator circuit comprises the pass element and error amplifier discussed in the previous sections. Additionally, a resistive feedback network is employed instead of the initially depicted configuration. The output capacitor and equivalent series resistance (ESR) are critical components for analysis and are placed at the output of the circuit, as illustrated in Figure 4.14.

To introduce the load current transient, an active load current mirror is incorporated, as shown in Figure 4.14. The voltage reference V_{ref} should be provided by an ideal voltage source, ensuring that the output voltage V_{out} is determined by the equation:

$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2} \right)$$

Ensuring the stability of the system requires several techniques, as discussed in Chapter 3. Relying on a single technique would not suffice to meet the proposed specifications. Key strategies include using a low ESR value and a large output capacitor, alongside employing a very large PMOS pass transistor.

As previously mentioned, the circuit architecture is based on a three-stage amplifier design that drives a large capacitive load. In such multistage amplifiers, the pole at the output is located at a low frequency and is very close to the dominant pole. Consequently, the LDO must be stabilized by mitigating the effect of the pole at the output. This stabilization can be achieved through pole-splitting using compensation capacitors or pole-zero cancellation using feedforward paths. Notably, the stability of the proposed LDO remains unaffected when the supply voltage increases from the dropout voltage.

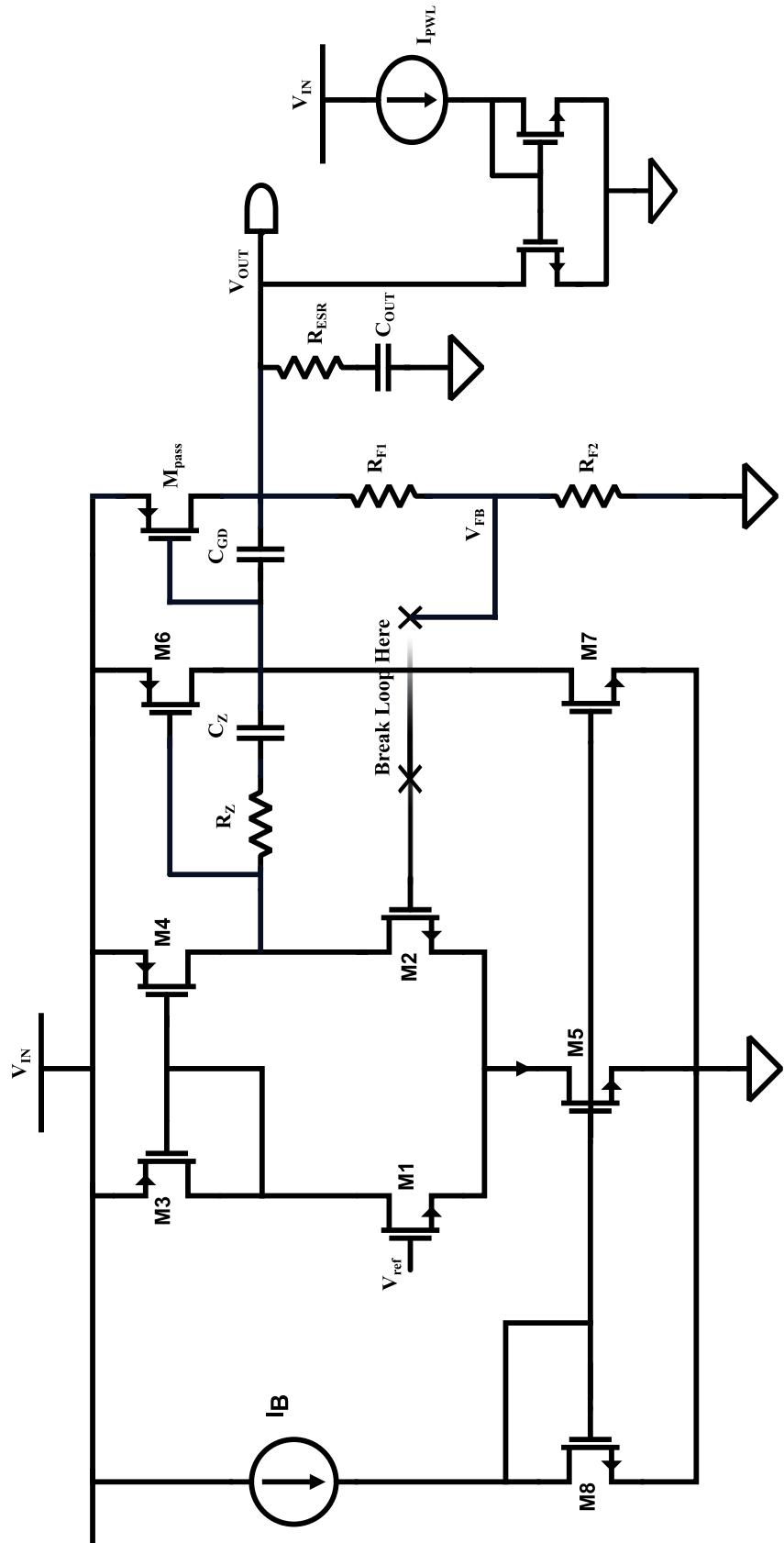


Figure 4.14: LDO Circuit with Output Capacitor and ESR

Chapter 5

LDO Design Methodology In 130nm Technology

5.1 Motivation

This research focuses on developing a Low-Dropout (LDO) voltage regulator characterized by high current efficiency, minimal dropout voltage, and robust power supply rejection ratio (PSRR). These features are critical for battery-powered portable devices such as smartphones and personal digital assistants (PDAs). Incorporating power management circuits within every chip is essential in the modern electronics industry, which is increasingly geared towards system-on-chip (SoC) integration. LDO regulators play a crucial role in converting the higher battery voltages to lower, stable levels necessary for reliable system operation, thereby protecting sensitive components from power supply variations.

High current efficiency is paramount, especially under low load conditions, as it directly impacts battery longevity and system performance. The design process in this work utilizes 130nm BCD technology and begins with a Python-based approach to predefine initial specifications. These include calculating preliminary (W/L) ratios and compensation values, which are then fine-tuned using local optimization algorithms within the Cadence Virtuoso environment. This methodology ensures that the LDO design is not only efficient but also meets the stringent requirements of contemporary electronic applications. Below is a table outlining the initial specifications used in the design process.

This approach emphasizes the significance of LDOs in the broader context of power management solutions, catering to the increasing demand for integrated and efficient power supply circuits.

5.1.1 Specifications Summary

The table below (Table 5.1) presents the specifications for three different LDO design cases, each tailored for various operational requirements and application scenarios. These specifications form the basis for the design objectives guiding the optimization processes described in previous chapters. The goal is to develop LDOs that integrate seamlessly into System-on-Chip (SoC) solutions, thereby improving overall power management efficiency.

Table 5.1: Summary of LDO Parameters Specifications

Specification	Case 1 (1.8 V)	Case 2 (2.5 V)	Case 3 (3.3 V)
Output Voltage	1.8 V	2.5 V	3.3 V
Load Current	20 mA	200 mA	100 mA
Load Capacitor	50 nF	150 nF	100 nF
Input Voltage	5 V	5 V	5 V
Reference Voltage	1.2 V	1.2 V	1.2 V
Dropout Voltage	< 400 mV	< 350 mV	< 250 mV
PSRR	> 95 dB	> 90 dB	> 85 dB
Output Voltage Ripple	< 36mV	< 50mV	< 40mV

The subsequent sections will detail the design methodology, simulation results, and performance evaluations that validate the achievement of these specifications in the developed LDO designs. As discussed in Chapter 3, the frequency stability in an LDO regulator is influenced by the load current, which introduces several critical considerations in its design. This chapter applies the techniques previously described to develop an LDO regulator optimized for high performance. Using established methodologies, the designed LDO achieves low dropout voltage and minimal quiescent current while maintaining a high power supply rejection ratio (PSRR) and meeting other critical specifications.

5.2 Case 1: Simulation Results and Analysis

This chapter presents the detailed simulation results for the Low-Dropout (LDO) regulator designed in 130nm BCD technology. The analysis covers input-output characteristics, AC analysis, PSRR, and transient response. The specifications for the LDO design in Case 1 are summarized in Table 5.2. These specifications include the output voltage, load current, input voltage, reference voltage, dropout voltage, PSRR, and output voltage ripple.

Parameter	Value
Output Voltage V_{out}	1.8 V
Load Current I_{load}	20 mA
Input Voltage V_{in}	2.1 to 5 V
Reference Voltage V_{ref}	1.2 V
Dropout Voltage V_{DO}	< 400 mV
PSRR	> 95 dB
Output Voltage Ripple	< 36 mV

Table 5.2: Specifications for Case 1 (1.8 V Output)

5.2.1 Local Optimization Summary Without Reference Variables

The Cadence local optimization summary for Case 1 is presented below, highlighting the key performance metrics achieved using random variable settings. The optimization results indicate that while the PSRR and output voltage specifications were met, the dropout voltage and phase margin did not meet the desired specifications. The overall time it took to complete the simulation was 59.25 minutes. This provides a foundation for further fine-tuning and optimization.

Parameter	Value	Spec	Pass/Fail
PSRR_LDO_@1KHz	105.3 dB	> 95 dB	pass
LDO_Output_Voltage	1.8 V	tol 1.8%	pass
LDO_DO	504.3 mV	< 400 mV	fail
Vout_Overshoot	31.7 mV	< 36 mV	pass
Vout_Undershoot	19.12 mV	< 36 mV	pass
Phase Margin	18.53°	> 50°	fail

Table 5.3: Case 1: Local Optimization Summary for 1.8V with Random Variables

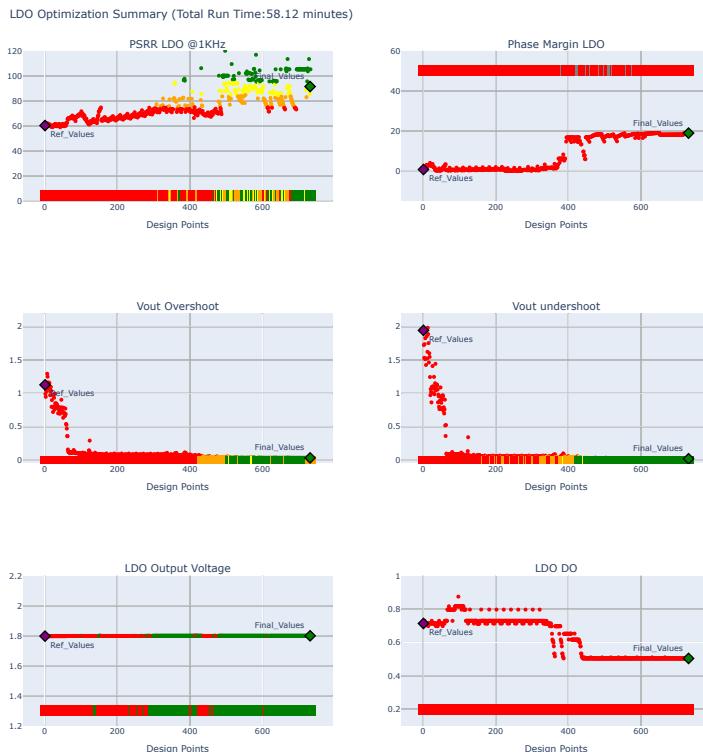


Figure 5.1: LDO Optimization Summary for 1.8V with Random Variables

5.2.2 Local Optimization Summary in Cadence Virtuoso

Before presenting the results of the LDO design, it is essential to summarize the local optimization process carried out in Cadence Virtuoso. This step is crucial to refine the initial design parameters obtained from Python-based initial sizing. The optimization aims to achieve the best possible performance in terms of dropout voltage, phase margin, PSRR, output voltage overshoot, and undershoot.

The BFGS algorithm was used for its robust convergence properties and efficiency in analog design optimization. This process involved iteratively adjusting design variables within specified ranges to minimize deviations from target values.



Figure 5.2: LDO Optimization Summary

The above figure (5.2) illustrates the optimization summary for the LDO design. It includes the final values of critical parameters such as PSRR, phase margin, output voltage overshoot, and undershoot, compared to the initial reference values. The design points are iteratively adjusted to meet the desired specifications effectively.

The Cadence local optimization summary is provided in Table 5.4, demonstrating that all conditions are satisfied after completing the local optimization. Initial conditions such as (W/L) ratios, bias currents, and compensation values are detailed in the table.

Reference Variables			
W7, W4, ESR, W6, W1, Cc, Wpass, W5, Cout, Rca, idc 164 μ , 21 μ , 0.1, 317 μ , 15 μ , 2p, 2.325m, 21 μ , 50nF, 400, 50 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	71.4 dB	> 95 dB	fail
LDO_Output_Voltage	1.8V	tol 1%	pass
LDO_DO	302.5mV	< 400mV	pass
Vout_Overshoot	17.62mV	< 36mV	pass
Vout_Undershoot	11.28mV	< 36mV	pass
Phase Margin	25.03°	> 50°	fail
Final Variables			
W7, W4, ESR, W6, W1, Cc, Wpass, W5, Cout, Rca, idc 162 μ , 18 μ , 0.25, 317 μ , 17 μ , 1.2p, 2.625m, 25 μ , 50nF, 590, 80 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	102.8 dB	> 95 dB	pass
LDO_Output_Voltage	1.8V	tol 1%	pass
LDO_DO	302.9mV	< 400mV	pass
Vout_Overshoot	11.02mV	< 36mV	pass
Vout_Undershoot	6.503mV	< 36mV	pass
Phase Margin	56.88°	> 50°	pass

Table 5.4: Case 1: Local Optimization Summary

Input-output voltage characteristics

The input-output characteristics of the LDO regulator are obtained by sweeping the DC input voltage supply, as shown in Figure 5.3. These characteristics are measured under maximum load current conditions ($I_{load} = 20\text{ mA}$) to verify the dropout voltage value.

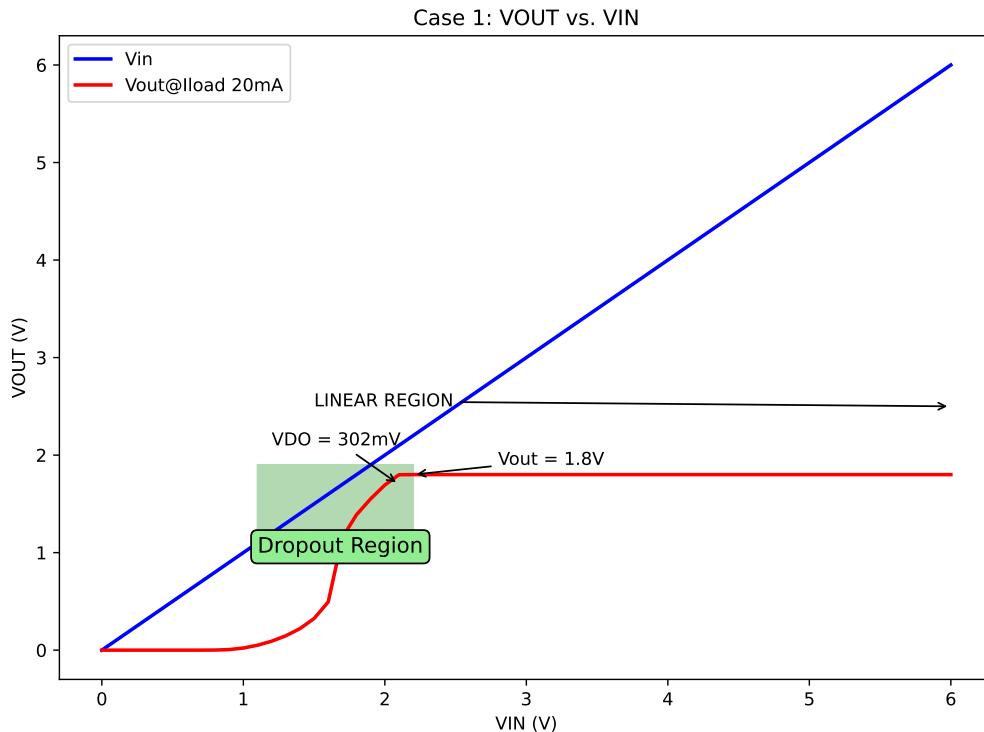


Figure 5.3: Input-output characteristics for Case 1: V_{OUT} vs. V_{IN} at $I_{load} = 20\text{ mA}$

It can be observed from Figure 5.3 that the output voltage remains regulated for an input voltage ranging from 2.1V to 5V when the output is set to 1.8V. The dropout voltage, defined as the minimum difference between V_{IN} and V_{OUT} where regulation is maintained, is determined to be $V_{DO} = 302\text{ mV}$.

This characteristic confirms the regulator's efficiency in maintaining a stable output voltage within the specified input voltage range, ensuring the LDO's ability to manage transitions between the dropout region and the linear region effectively.

5.2.3 Frequency Response

Figure 5.4 shows the LDO regulator's frequency response at an input supply voltage of 5V, load currents of 20mA, and output voltage set to 1.8V. The typical phase margin considered during the local optimization in Cadence is 50 degrees and meets the specification as shown in the figure below 5.4.

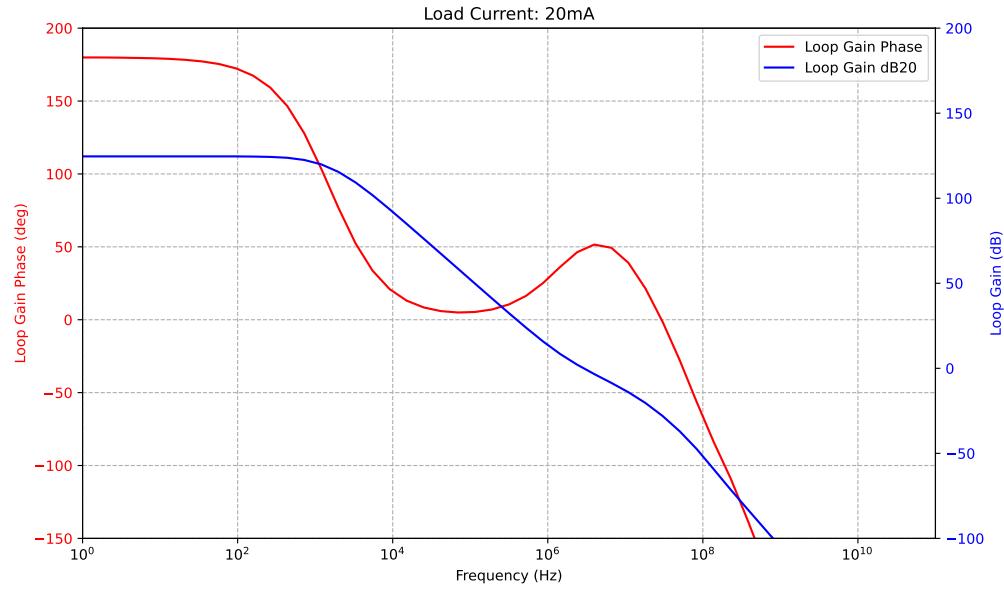


Figure 5.4: Gain and Phase Response for Case 1 at $I_{load} = 20 \text{ mA}$

Power Supply Rejection Ratio (PSRR)

Figure 5.5 illustrates the PSRR of the proposed LDO voltage regulator at $V_{IN} = 5\text{V}$. The PSRR was set to be greater than 95 dB during local optimization, and the design met this specification, as shown in the figure below.

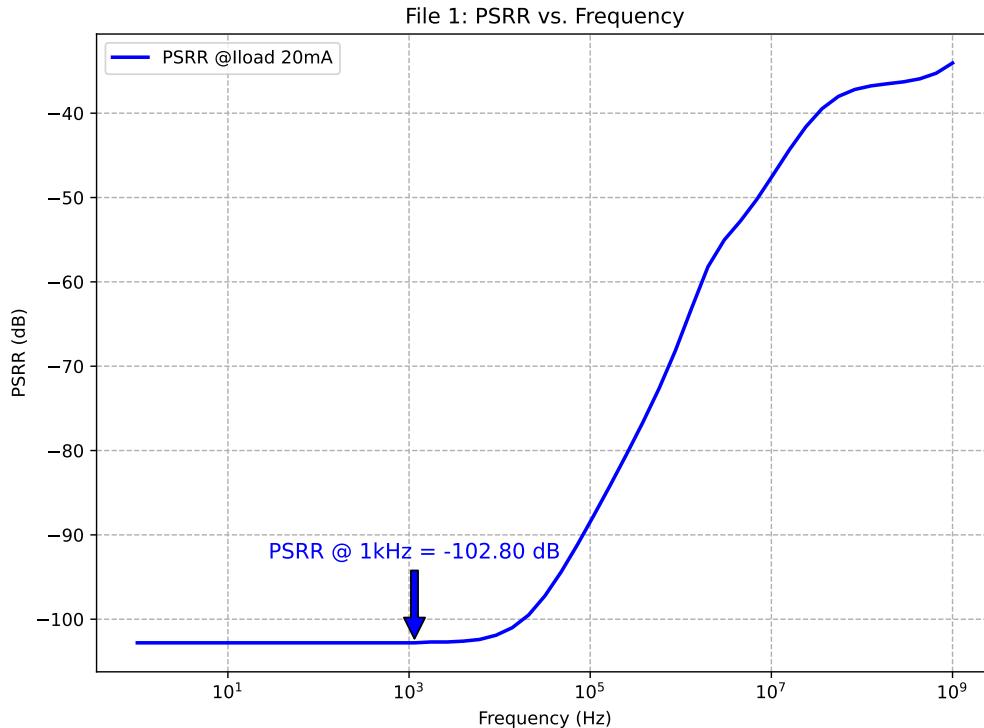


Figure 5.5: PSRR vs. Frequency for Case 1

5.2.4 Transient Analysis

In order to verify the LDO regulator's transient performance, it is necessary to observe how the output voltage settles when the load current changes. Load Transient is a behavior that occurs when there is a sudden change in the load current. In an LDO, a change from minimum to maximum load current results in undershoots, and from maximum to minimum results in overshoots at the output [28].

Figure 5.6 shows the transient response. It can be observed that it exhibits an undershoot value of 11uV and an overshoot of 15uV. The load current changes from 10uA to 20mA, which can be set as preconditions in Cadence local optimization that undershoot and overshoot should be less than 36mV of Vout, satisfying the conditions.

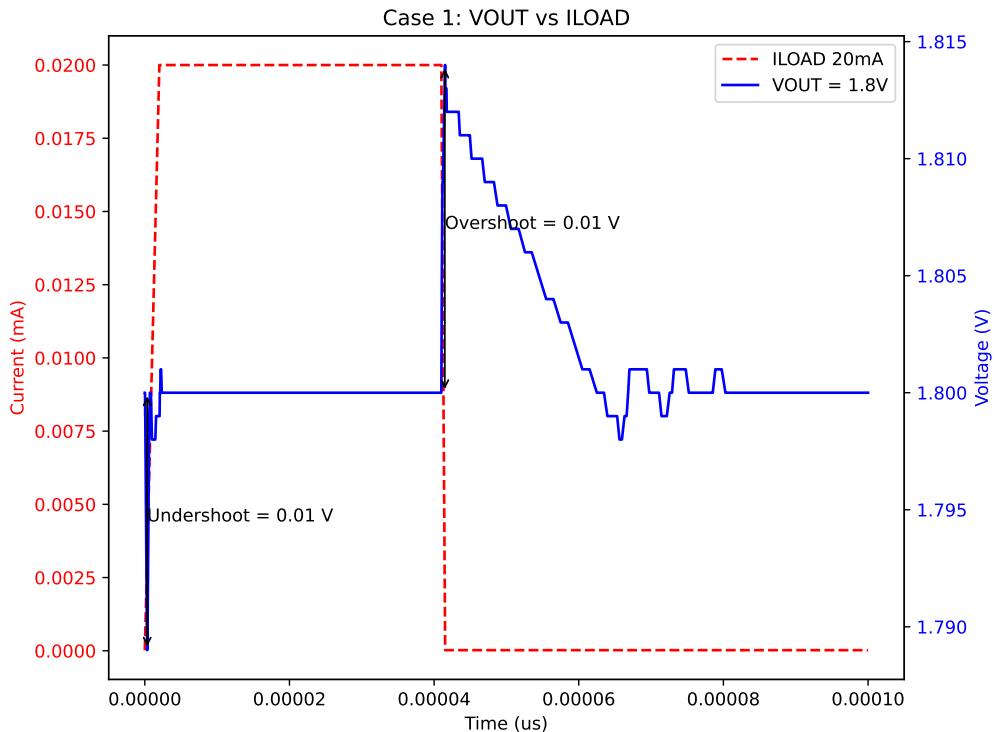


Figure 5.6: Transient Response for Case 1

5.3 Case 2: Simulation Results and Analysis

The specifications for the LDO design in Case 2 are summarized in Table 5.5. These specifications include the output voltage, load current, input voltage, reference voltage, dropout voltage, PSRR, and output voltage ripple.

Parameter	Value
Output Voltage V_{out}	2.5 V
Load Current I_{load}	200 mA
Load Capacitor C_{load}	150 nF
Input Voltage V_{in}	3.1 to 5 V
Reference Voltage V_{ref}	1.2 V
Dropout Voltage V_{DO}	< 350 mV at full load
PSRR	> 90 dB
Output Voltage Ripple	< 50mV

Table 5.5: Case 2: LDO Parameters Specifications

5.3.1 Local Optimization Summary in Cadence Virtuoso

For Case 2, the LDO design specifications are outlined in Table 5.5. In Cadence Virtuoso, local optimization using the BFGS algorithm was essential to refine these performance parameters. This process involved dynamic adjustments of (W/L) ratios, bias currents, and compensation values to achieve optimal PSRR, output voltage stability, and transient response characteristics. The optimization results, depicted in Figure 5.7, demonstrate successful tuning of the LDO, validating the design against initial targets, and proving the efficacy of integrated design and optimization workflows.

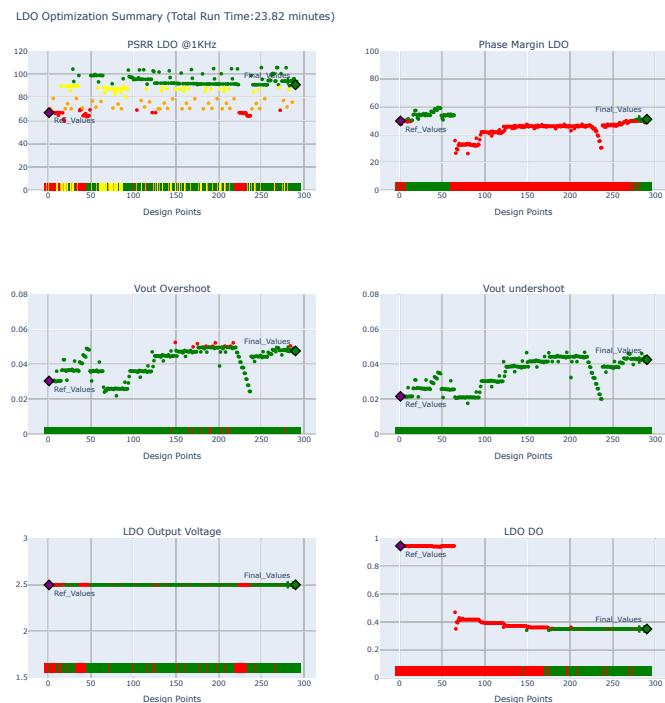


Figure 5.7: LDO Optimization Summary for Case 2

The Cadence local optimization summary for Case 2 is shown in Table 5.6. After optimization, all parameters meet the desired specifications, indicating a successful refinement of the LDO design. Initial conditions such as (W/L) ratios, bias currents, and compensation values are also detailed in Table 5.6.

Reference Variables			
W7, W4, ESR, W6, W1, Cc, Wpass, W5, Cout, Rca, idc 200 μ , 10 μ , 0.1, 240 μ , 40 μ , 1p, 9.24m, 30 μ , 150n, 500, 100 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	66.9 dB	> 90 dB	fail
LDO_Output_Voltage	2.499V	tol 1%	pass
LDO_DO	946mV	< 350mV	fail
Vout_Overshoot	30.46mV	< 50mV	pass
Vout_Undershoot	21.62mV	< 50mV	pass
Phase Margin	49.77°	> 50°	fail
Final Variables			
W7, W4, ESR, W6, W1, Cc, Wpass, W5, Cout, Rca, idc 210 μ , 12 μ , 0.435, 268 μ , 40 μ , 3.7p, 7.3m, 28 μ , 150n, 580, 100 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	94.0 dB	> 90 dB	pass
LDO_Output_Voltage	2.5V	tol 1%	pass
LDO_DO	349.7mV	< 350mV	pass
Vout_Overshoot	48.73mV	< 50mV	pass
Vout_Undershoot	42.45mV	< 50mV	pass
Phase Margin	51.29°	> 50°	pass

Table 5.6: Case 2: Local Optimization Summary

5.3.2 Input-Output Voltage Characteristics

The input-output characteristics of the LDO regulator for Case 2 are obtained by sweeping the DC input voltage supply, as shown in Figure 5.8. The characteristics are measured under maximum load current conditions ($I_{load} = 200\text{ mA}$) to verify the dropout voltage value.

From Figure 5.8, it can be observed that the output voltage remains regulated for an input voltage ranging from 3.1V to 6V, with the output set to 2.5V. During the local optimization for Case 2, the dropout voltage was specified to be less than

350 mV. However, the obtained dropout voltage is 349 mV, meeting the expected specification.

Increasing the size of the pass transistor helps lower the dropout voltage for a specific output current within the milliampere range. However, this increase in size results in a larger gate capacitance, which can make it challenging to meet stability and slew rate requirements. The larger gate capacitance affects the speed at which the pass transistor can respond to changes in the load, impacting the overall performance.

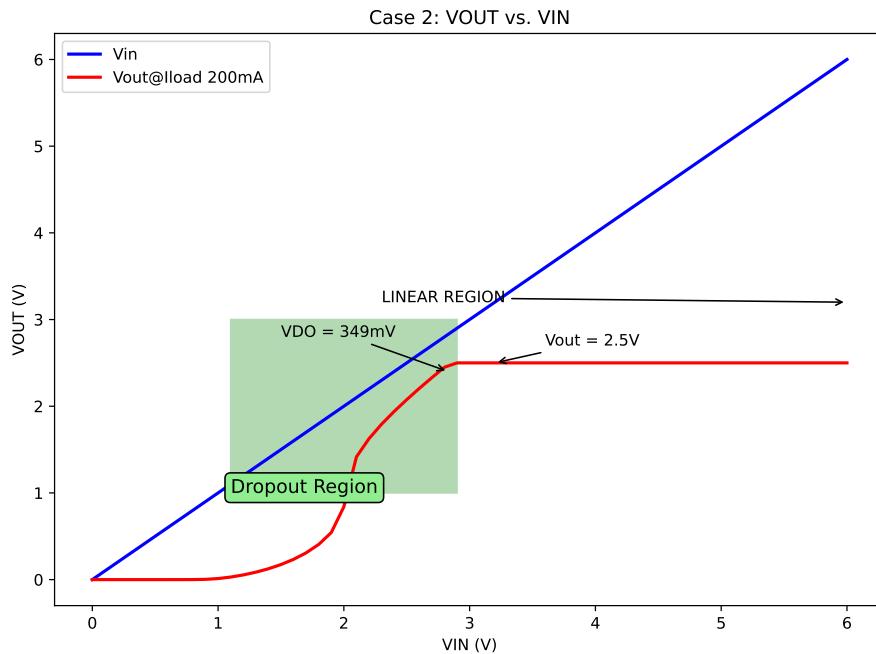


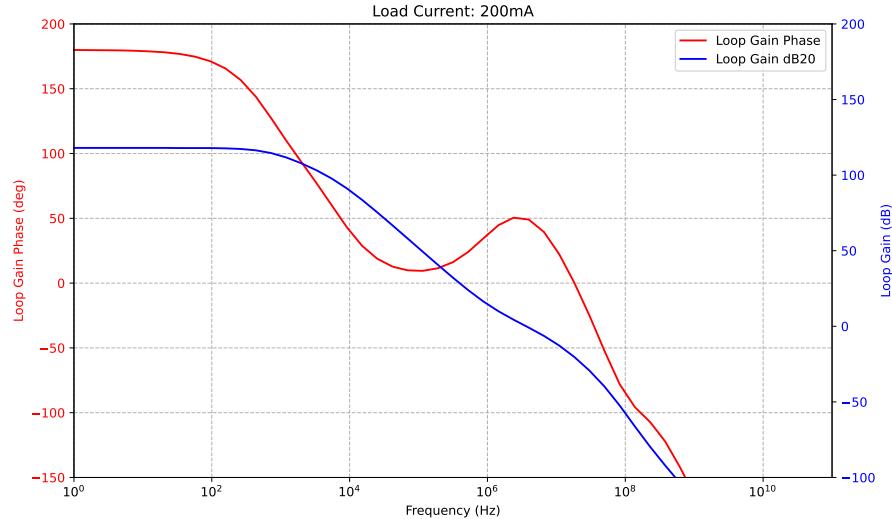
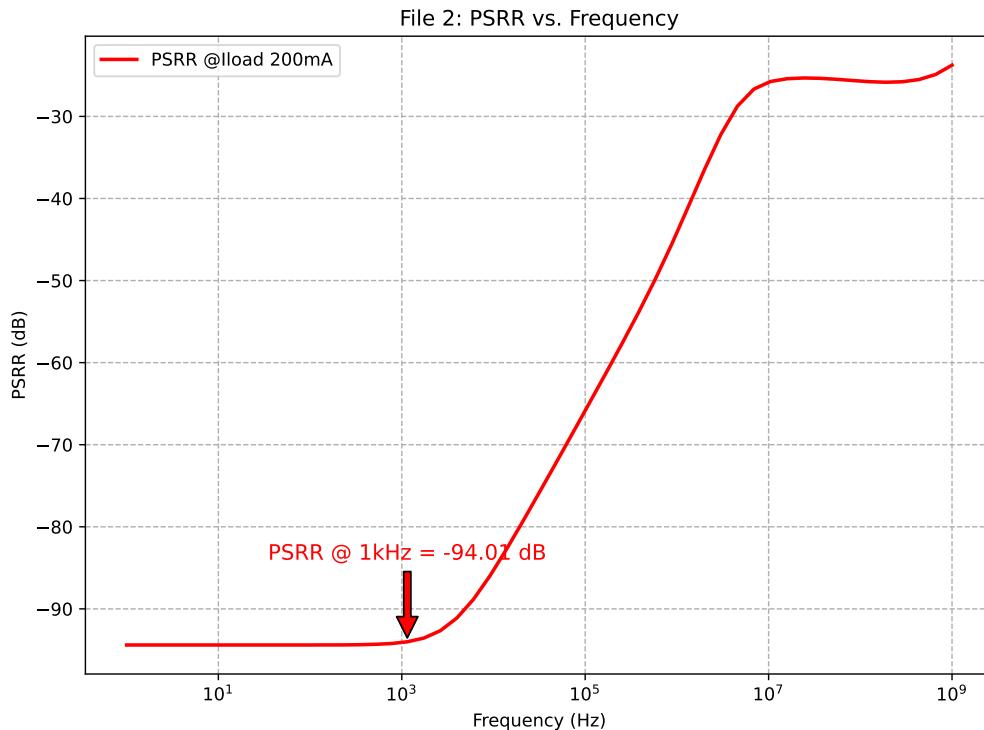
Figure 5.8: Input-output characteristics for Case 2: V_{OUT} vs. V_{IN} at $I_{load} = 200 \text{ mA}$

5.3.3 Frequency Response

The frequency response of the LDO regulator at an input supply voltage of 5V and load currents of 200mA, with the output voltage set to 2.5V. The phase margin > 50 degrees achieved meets the specified criteria, ensuring stability as shown in 5.9 the frequency response plot.

Power Supply Rejection Ratio (PSRR)

The PSRR plot for Case 2, illustrated in Figure 5.10, shows that the measured PSRR at 1 kHz is 94 dB, which exceeds the specified requirement. confirming the design's effectiveness in rejecting power supply variations.


 Figure 5.9: Gain and Phase Response for Case 2 at $I_{load} = 200 \text{ mA}$

 Figure 5.10: Case 2: PSRR Analysis at $V_{in} = 5\text{V}$ and $I_{load} = 200\text{mA}$

5.3.4 Transient Analysis

The transient performance of the LDO regulator for Case 2 is tested by observing the output voltage's response to load current changes. The undershoot and overshoot values are measured during transitions from minimum to maximum load current and vice versa. Figure 5.11 shows the transient response. It can be observed that the transient response exhibits an undershoot value of 42.45 mV and an overshoot of 48.73 mV, as shown in Figure 5.11. The load current changes from 200 μA to 200 mA. Both the undershoot and overshoot requirements were set to be less than 50

mV and were satisfied.

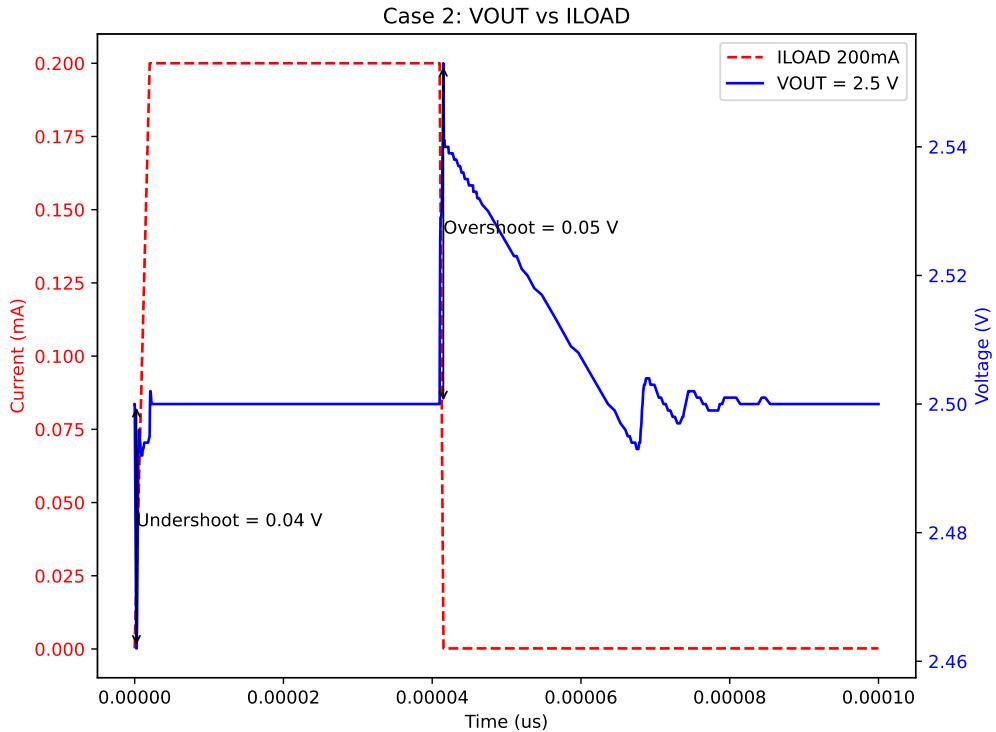


Figure 5.11: Case 2: Transient Response Analysis at $V_{in} = 5V$, I_{load} changing between $200\mu A$ and $200mA$

5.4 Case 3: Results and Analysis

The specifications for the LDO design in Case 3 are summarized in Table 5.7. These specifications include the output voltage, load current, input voltage, reference voltage, dropout voltage, PSRR, and output voltage ripple.

Parameter	Value
Output Voltage V_{out}	3.3 V
Load Current I_{load}	100 mA
Load Capacitor C_{load}	100 nF
Input Voltage V_{in}	3.5 to 6 V
Reference Voltage V_{ref}	1.2 V
Dropout Voltage V_{DO}	< 250 mV at full load
PSRR	> 85 dB
Output Voltage Ripple	< 40mV

Table 5.7: Case 3: LDO Parameters Specifications

5.4.1 Local Optimization Summary in Cadence Virtuoso

For Case 3, local optimization in Cadence Virtuoso was crucial in refining the LDO's performance parameters to ensure they meet or exceed the specified requirements. The optimization, using the BFGS algorithm, focused on the dynamic adjustment of (W/L) ratios, bias currents, compensation values, and other relevant parameters to achieve optimal PSRR, output voltage stability, and transient response characteristics.

Key outcomes of this optimization, as documented in Figure 5.12, reveal successful tuning of the LDO to maintain robust performance across varying conditions.



Figure 5.12: LDO Optimization Summary for Case 3

The Cadence local optimization summary for Case 3 is presented in Table 5.8. Most parameters meet the desired specifications, except for the dropout voltage, which showed a slight deviation but was still within an acceptable range. The overall performance of the LDO in terms of other parameters such as PSRR and phase margin was satisfactory. Initial conditions such as (W/L) ratios, bias currents, and compensation values are detailed in Table 5.8.

Reference Variables			
W7, W4, ESR, W6, W1, Cc, Wpass, W5, Cout, Rca, idc			
160 μ , 10 μ , 0.1, 230 μ , 20 μ , 1p, 2.2m, 30 μ , 50n, 500, 60u			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	68.75 dB	> 85 dB	fail
LDO_Output_Voltage	3.298V	tol 1%	pass
LDO_DO	913.6mV	< 250mV	fail
Vout_Overshoot	25.72mV	< 40mV	pass
Vout_Undershoot	27.64mV	< 40mV	pass
Phase Margin	39.47°	> 50°	fail
Final Variables			
W7, W4, ESR, W6, W1, Cc, Wpass, W5, Cout, Rca, idc			
200 μ , 14 μ , 1.9, 230 μ , 26 μ , 1.6p, 4.2m, 34 μ , 50n, 680, 100u			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	89.4 dB	> 85 dB	pass
LDO_Output_Voltage	3.3V	tol 1%	pass
LDO_DO	309.4mV	< 250mV	fail
Vout_Overshoot	22.68mV	< 40mV	pass
Vout_Undershoot	21.63mV	< 40mV	pass
Phase Margin	51.29°	> 50°	pass

Table 5.8: Case 3: Local Optimization Summary

5.4.2 Input-Output Voltage Characteristics

The input-output characteristics for Case 3 are obtained by sweeping the DC input voltage supply. The characteristics are measured under maximum load current conditions ($I_{load} = 100\text{mA}$) to verify the dropout voltage.

The output voltage remains regulated for an input voltage ranging from 3.5V to 6V when the output is set to 3.3V as shown in Figure 5.13. During the local optimization for Case 3, the dropout voltage was set to be less than 250 mV. However, the obtained dropout voltage was 310 mV, which did not meet the expected specification.

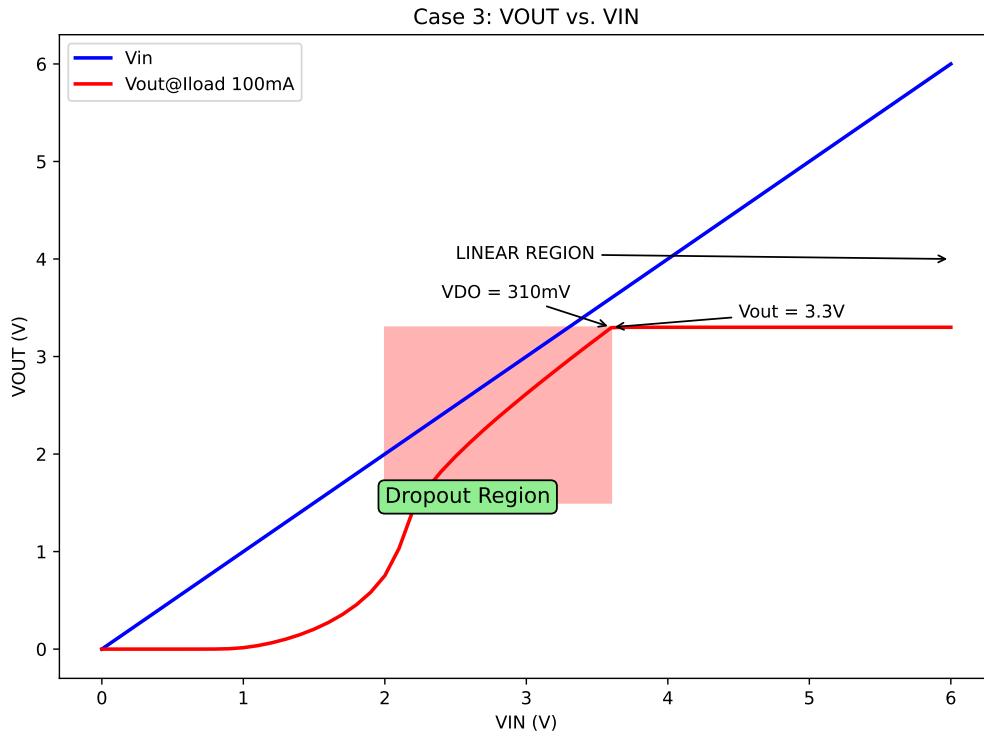


Figure 5.13: Input-output characteristics for Case 3: V_{OUT} vs. V_{IN} at $I_{load} = 100 \text{ mA}$

5.4.3 Frequency Response

The frequency response of the LDO regulator at an input supply voltage of 5V and load currents of 100mA as shown in Figure 5.14, with the output voltage set to 3.3V. The phase margin >50 degrees achieved ensures the stability of the LDO.

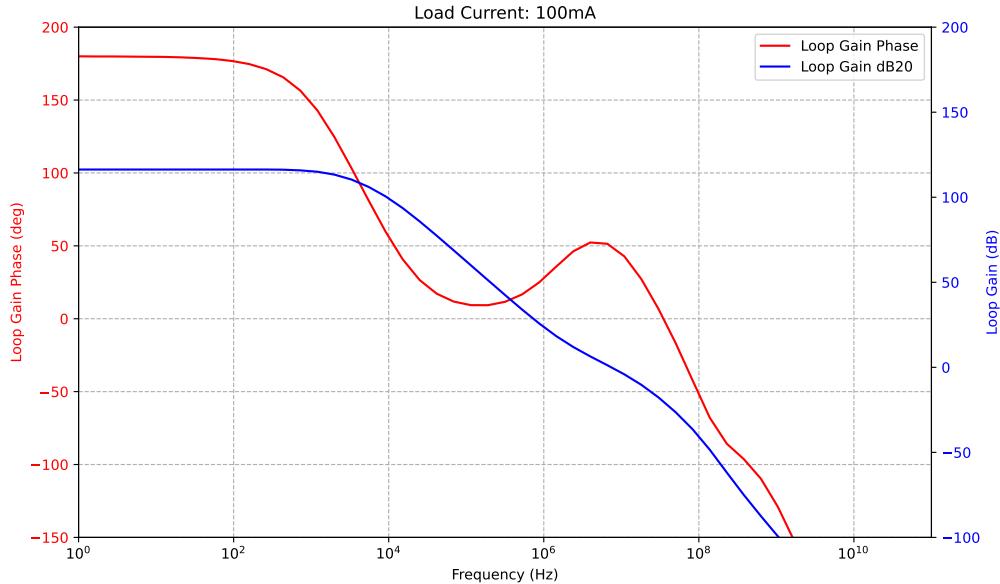


Figure 5.14: Gain and Phase Response for Case 3 at $I_{load} = 100 \text{ mA}$

Power Supply Rejection Ratio (PSRR)

The PSRR for Case 3, shown in Figure 5.15, indicates that the PSRR at 1 kHz is approximately 89.4 dB, which satisfies the design specification of greater than 85 dB. This result demonstrates the effectiveness of the LDO in maintaining a stable output voltage despite variations in the input power supply.

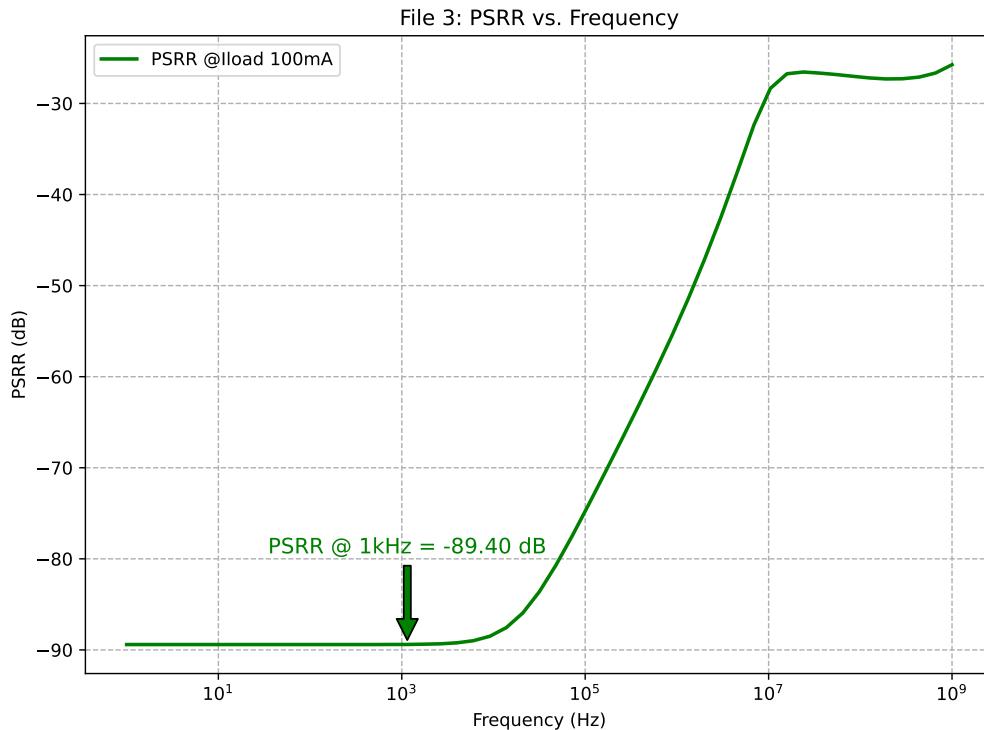


Figure 5.15: Case 3: PSRR Analysis at $V_{out} = 3.3V$ and $I_{load} = 100mA$

5.4.4 Transient Analysis

For Case 3, the transient performance is tested by observing the output voltage's response to load current changes. The undershoot and overshoot values are measured during transitions from minimum to maximum load current and vice versa. The LDO shows satisfactory transient performance with undershoot and overshoot values well within the specified limits, as shown in Figure 5.16.

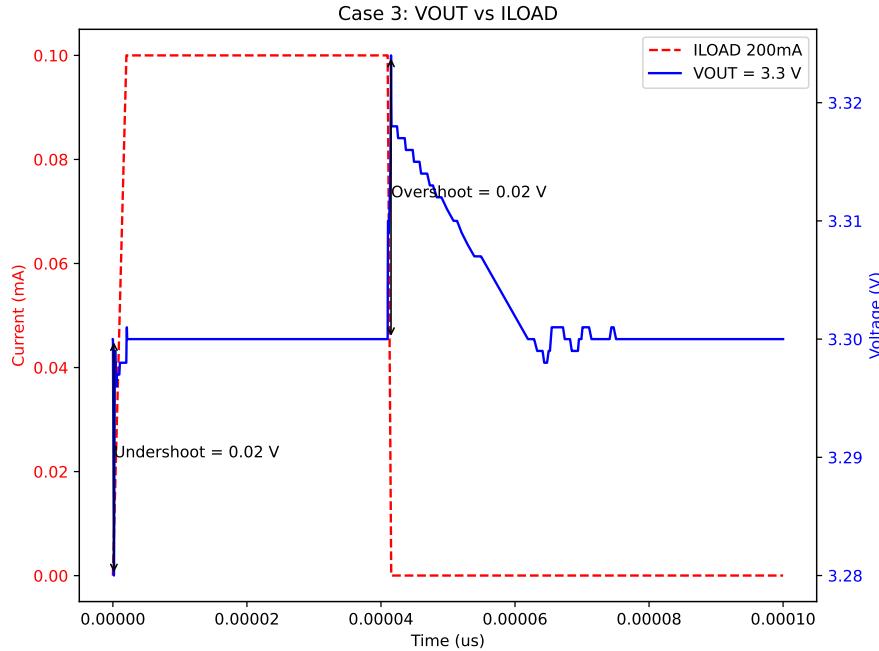


Figure 5.16: Case 3: Transient Response Analysis at $V_{out} = 3.3V$, I_{load} changing between 100uA and 100mA

5.5 Conclusion

In this chapter, detailed simulation results and analyses for three different cases of Low-Dropout (LDO) regulator designs were presented using the Cadence Virtuoso environment. Using the BFGS algorithm for local optimization, it was ensured that most parameters met the desired specifications, although there were minor deviations in some cases. For instance, Case 2 showed a higher-than-expected dropout voltage due to the increased size of the pass transistor, and Case 3 had a slight deviation in the dropout voltage as well. Despite these discrepancies, the overall performance of the LDO regulators was satisfactory, with parameters like PSRR and phase margin meeting the required standards.

In the next chapter, this methodology will be extended to design an LDO in 22nm technology, leveraging the same optimization techniques to explore potential improvements and challenges posed by the advanced technology node.

Chapter 6

LDO Design Methodology IN 22nm FDSOI Technology

6.1 Introduction

Advancements in semiconductor technology, such as GlobalFoundries' proprietary FDX® technology, based on fully depleted silicon-on-insulator (FDSOI), have paved the way for designing highly efficient Low-Dropout (LDO) regulators. The FDX® process technology platform is particularly advantageous for the integration of digital and analog signals on a single chip, offering features like ultra-high speed and ultra-low leakage. These characteristics make it especially suitable for periphery designs like LDOs or low-power bandgaps. This chapter delves into the methodology for designing an LDO regulator in 22nm FDSOI technology, leveraging the optimization techniques and insights discussed in previous chapters [29].

6.2 Motivation

The motivation for adopting 22nm FDSOI technology includes achieving higher integration density, lower power consumption, and improved performance metrics such as enhanced PSRR and reduced dropout voltage. FDSOI technology offers unique benefits, such as minimized short-channel effects and improved electrostatic control, which are crucial for analog and mixed-signal designs. Additionally, the body biasing layer in FDX® technology allows for dynamic threshold voltage adjustments, optimizing for either ultra-low leakage or ultra-high speed, depending on the operating mode. Due to its lower threshold voltage, the 22-nm CMOS technology significantly reduces power consumption and enhances response speed. Additionally, incorporating a three-stage gain-enhanced structure along with adaptive biasing techniques enables this LDO to deliver a rapid transient response and exceptional PSRR performance [30].

6.2.1 Design Considerations in 22nm FDSOI Technology

The proposed LDO is designed in 22nm FDSOI (Fully Depleted Silicon On Insulator) technology. FDSOI technology features two primary modifications compared to CMOS bulk technology. First, there is an ultra-thin layer of insulator, called the

buried oxide (BOX), at the top of the base silicon. Second, a thin silicon film implements the transistor channel, eliminating the need to dope the channel, hence the name fully depleted transistor. This construction results in superior transistor electrostatic characteristics compared to conventional bulk technology.

In fully depleted SOI (FDSOI) devices, most field lines propagate through the buried oxide (BOX) before reaching the channel region, reducing parasitic capacitance between the drain and source terminals. Short-channel effects are mitigated using this thin buried oxide and an underlying ground plane. FDSOI devices also exhibit significantly reduced leakage current and better performance.

Output Impedance Variation with Drain-Source Voltage

In modeling channel-length modulation with a single constant λ , it is assumed that the output impedance of the transistor, r_O , remains constant in the saturation region. In reality, however, r_O varies with V_{DS} . As V_{DS} increases and the pinch-off point moves toward the source, the rate at which the depletion region around the source becomes wider decreases, resulting in a higher incremental output impedance [31].

In this regime, the output impedance can be approximated as:

$$r_O = \frac{2L}{1 - \frac{\delta L}{L}} \cdot \frac{1}{I_D \sqrt{N_B 2\epsilon_{Si} (V_{DS} - V_{DS,sat})}}$$

where $V_{DS,sat}$ is the drain-source voltage at the onset of pinch-off, L is the channel length, I_D is the drain current, N_B is the substrate doping concentration, and ϵ_{Si} is the permittivity of silicon.

In short-channel devices, as V_{DS} increases further, drain-induced barrier lowering (DIBL) becomes significant. This effect reduces the threshold voltage and increases the drain current, further impacting the output impedance. Therefore, the output impedance in short-channel devices is not constant and varies with V_{DS} , especially under higher drain-source voltages [31].

Threshold Voltage

Threshold voltage (V_{th}) is the minimum voltage required to turn on a transistor. It affects both the overdrive and current of the transistor, making it a critical parameter in circuit design. Understanding how V_{th} varies with other parameters is essential for designing robust circuits.

At shorter channel lengths, V_{th} increases due to the reverse short channel effect, which is caused by non-uniform channel doping. Near the drain and source terminals, the channel is more heavily doped, reducing the size of the depletion region near these junctions. When the channel length is short, the doping of the source overlaps with that of the drain, increasing the average channel doping concentration. This overlap leads to an increase in the threshold voltage, as illustrated below.

$$V_{th} \approx V_{th0} + \Delta V_{th(short)}$$

where V_{th0} is the initial threshold voltage and $\Delta V_{th(short)}$ represents the increase in threshold voltage due to the reverse short channel effect. This effect must be

carefully considered in the design of FDSOI devices to ensure proper operation and performance [32].

6.2.2 Body Effect

The threshold voltage (V_{th}) of a transistor changes with the source-to-bulk voltage, as described by the following equation 6.1, a phenomenon known as the body effect:

$$V_{th} = V_{t0} + \gamma \sqrt{|V_{sb} + 2\phi_F|} - \sqrt{|2 \cdot \phi_F|} \quad (6.1)$$

where γ is the junction depletion region coefficient, which depends on the technology used but is not voltage dependent, and ϕ_F is the Fermi potential. The body effect can often be mitigated by connecting the bulk to the source of the transistor, but this is not always feasible due to technology constraints.

FDSOI technology, however, provides an advantage in effectively controlling the threshold voltage. In FDSOI devices, the variation of parameter values and transistor behavior can be controlled through the gate terminal and by applying a voltage to the bulk terminal underneath the buried oxide.

6.2.3 Gain and Speed Trade-offs

For short-channel MOSFETs, increasing the drain current I_D (or equivalently increasing V_{GS}) results in an increase in speed (f_T). However, this comes at the cost of reduced gain, which can be expressed as an equation 6.2 [33].

$$g_m r_o = \sqrt{2K_{Pn} \frac{W}{L} I_D} \cdot \frac{1}{\lambda I_D} = \sqrt{2K_{Pn} \frac{W}{L}} \cdot \frac{1}{\lambda \sqrt{I_D}} \quad (6.2)$$

This shows that the gain decreases with increasing drain current I_D , with the help of another equation 6.3 [33].

$$g_m r_o = \frac{K_{Pn} \frac{W}{L} (V_{GS} - V_{THN})}{\lambda \cdot \frac{K_{Pn} \frac{W}{L} (V_{GS} - V_{THN})^2}{2}} = \frac{2}{\lambda (V_{GS} - V_{THN})} \propto \frac{L}{V_{ovn}} \quad (6.3)$$

This results in a higher gain due to the lower dependence on I_D and a more favorable relationship with (W/L) .

6.3 LDO Design Flow in 22nm FDSOI

In this section, the Low-Dropout (LDO) regulator design follows the same methodology and topology as outlined in the previous chapter for 130nm technology. The design process leverages the advantages of 22nm Fully Depleted Silicon On Insulator (FDSOI) technology to achieve enhanced performance metrics.

The design flow involves:

1. **Input Specifications:** Define the input specifications including input voltage range, output voltage, load current, PSRR, and output voltage ripple.
2. **Initial Parameter Calculation:** Compute the initial values such as (W/L) ratios, compensation capacitor (C_{out}), and Equivalent Series Resistance (RESR).

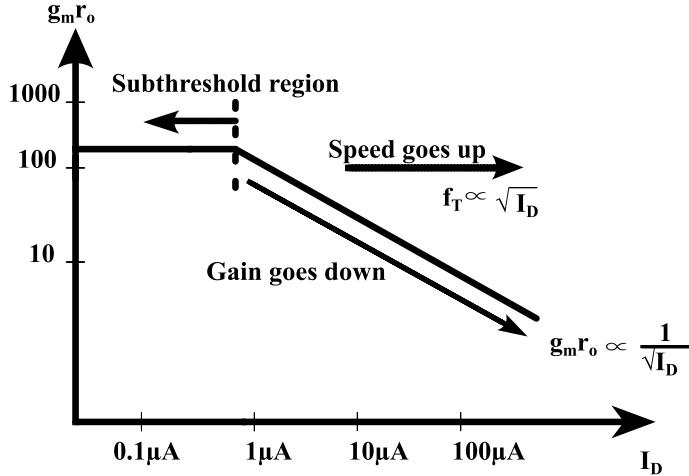


Figure 6.1: Gain falling off with bias current [33]

3. **Design of Error Amplifier:** Utilize a two-stage amplifier topology to meet high gain and stability requirements, ensuring low quiescent current and high output current capabilities.
4. **Design of Feedback Network:** Configure the feedback network to ensure accurate regulation and stability of the output voltage.
5. **Local Optimization:** Implement local optimization techniques in Cadence Virtuoso to fine-tune the design parameters and achieve the desired specifications.
6. **Performance Validation:** Validate the performance through simulations, checking parameters such as transient response, PSRR, load regulation, and dropout voltage.

This approach ensures that the LDO design in 22nm FDSOI technology inherits the robust design principles established for 130nm technology while taking advantage of the improved characteristics of the newer technology node.

The detailed simulation results and analysis for the 22nm FDSOI LDO design will be presented in the subsequent sections, highlighting the improvements and optimizations achieved with this advanced technology.

6.3.1 Specifications Summary

The table (6.1) below outlines the specifications for three distinct LDO design cases in the 22nm FDSOI technology, each tailored for different operational requirements and application scenarios.

Table 6.1: Summary of LDO Parameters Specifications in 22nm FDSOI Technology

Specification	Case 1 (1.0 V)	Case 2 (1.2 V)	Case 3 (1.5 V)
Output Voltage	1.0 V	1.2 V	1.5 V
Load Current	100 mA	20 mA	50 mA
Load Capacitor	150 pF	30 pF	50 pF
Input Voltage	1.8 V	1.8 V	1.8 V
Reference Voltage	0.9 V	0.9 V	0.9 V
Dropout Voltage	< 300 mV	< 200 mV	< 160 mV
PSRR	> 90 dB	> 80 dB	> 75 dB
Output Voltage Ripple	< 6%	< 3%	< 3.5%

6.4 Case 1: Simulation Results and Analysis

This chapter presents the detailed simulation results for the Low-Dropout (LDO) regulator designed in 22nm FDSOI technology. The specifications for the LDO design in Case 1 are summarized in Table 6.2. These specifications include the output voltage, load current, input voltage, reference voltage, dropout voltage, PSRR, and output voltage ripple.

Parameter	Value
Output Voltage V_{out}	1.0 V
Load Current I_{load}	100 mA
Load Capacitor C_{load}	150 pF
Input Voltage V_{in}	1.3 to 2 V
Reference Voltage V_{ref}	0.9 V
Dropout Voltage V_{DO}	< 300 mV
PSRR	> 90 dB
Output Voltage Ripple	< 60mV

Table 6.2: Specifications for Case 1 (1.0 V Output)

6.4.1 Local Optimization Summary in Cadence Virtuoso

For Case 1, the local optimization process in Cadence Virtuoso was crucial for fine-tuning the LDO's performance to meet or exceed specified requirements. Using the BFGS algorithm, the optimization dynamically adjusted parameters such as (W/L) ratios, bias currents, and compensation values to achieve optimal PSRR, output voltage stability, and transient response characteristics. As shown in Figure 6.2, the key outcomes of this optimization process include the successful tuning of the LDO, demonstrating robust performance under varying conditions.



Figure 6.2: LDO Optimization Summary for Case 1

The Cadence local optimization summary is presented in Table 6.3. While the optimization process resulted in several parameters meeting the specified conditions, some parameters, such as dropout voltage and overshoot voltage, did not fully meet the specifications. Despite these discrepancies, the overall performance of the LDO in terms of PSRR and phase margin was satisfactory. The initial conditions, including (W/L) ratios, bias currents, and compensation values, as well as the reference and final values, are shown in the table below 6.3.

Reference Variables			
W1, W3, W5, W6, W7, Wpass, Cc, Cout, Rc, idc			
12.6 μ , 13 μ , 20 μ , 176 μ , 980 μ , 65 μ , 4.5p, 150p, 1.26k, 50 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	77.54 dB	> 85 dB	fail
LDO_Output_Voltage	999.3 mV	tol 1%	pass
LDO_DO	434.3 mV	< 300mV	fail
Vout_Overshoot	71.91 mV	< 60mV	fail
Vout_Undershoot	58.51 mV	< 60mV	pass
Phase Margin	39.47°	> 50°	fail
Final Variables			
W1, W3, W5, W6, W7, Wpass, Cc, Cout, Rc, idc			
13.6 μ , 13 μ , 14 μ , 192 μ , 96 μ , 1.077m, 9.4p, 150p, 1.36k, 60 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	90.35 dB	> 85 dB	pass
LDO_Output_Voltage	999.9 mV	tol 0.5%	pass
LDO_DO	358 mV	< 300mV	fail
Vout_Overshoot	63.89 mV	< 60mV	near
Vout_Undershoot	58.56 mV	< 60mV	pass
Phase Margin	50.01°	> 50°	pass

Table 6.3: Case 1: Local Optimization Summary

Input-output voltage characteristics

The input-output characteristics of the LDO regulator are obtained by sweeping the DC input voltage supply, as shown in Figure 5.3. The characteristics are obtained under maximum load current conditions ($I_{load} = 100\text{ mA}$) to verify the dropout voltage value.

It can be observed from Figure 6.3 that the output voltage remains regulated for an input voltage ranging from 1.8V to 2V when the output is set to 1V. The dropout voltage can also be extracted from Fig. 6.3, providing critical information about the LDO regulator's efficiency.

The dropout voltage values were obtained in both the dropout region and at the beginning of the linear region. Specifically, the dropout voltage in the dropout region is $V_{DO} = 358\text{mV}$ at $V_{OUT} = 1\text{V}$.

During the local optimization for Case 1, the dropout voltage was set to be less

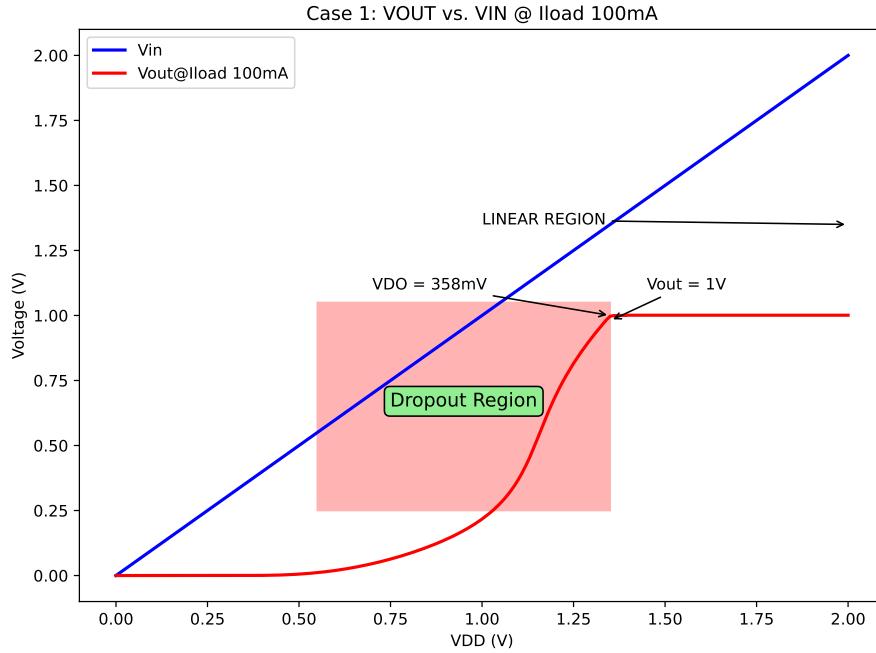


Figure 6.3: Input-output characteristics for Case 1: V_{OUT} vs. V_{IN} at $I_{load} = 100 \text{ mA}$

than 300 mV. However, the obtained dropout voltage was 358 mV, which does not meet the expected specification.

6.4.2 Frequency Response

The frequency response of the LDO regulator at an input supply voltage of 1.8V and load current of 100mA, with the output voltage set to 1V, is shown in Figure 6.4. The phase margin achieved is greater than 50 degrees, meeting the specified criteria and ensuring stability.

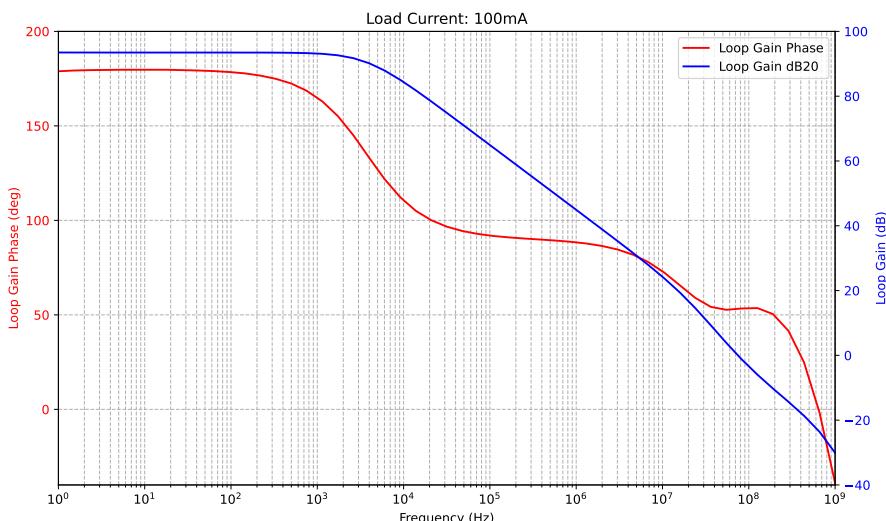


Figure 6.4: Gain and Phase Response for Case 1 at $I_{load} = 100 \text{ mA}$

Power Supply Rejection Ratio (PSRR)

The PSRR plot for Case 1, illustrated in Figure 6.5, shows that the PSRR meets the 90 dB requirement, confirming the design's effectiveness in rejecting power supply variations.

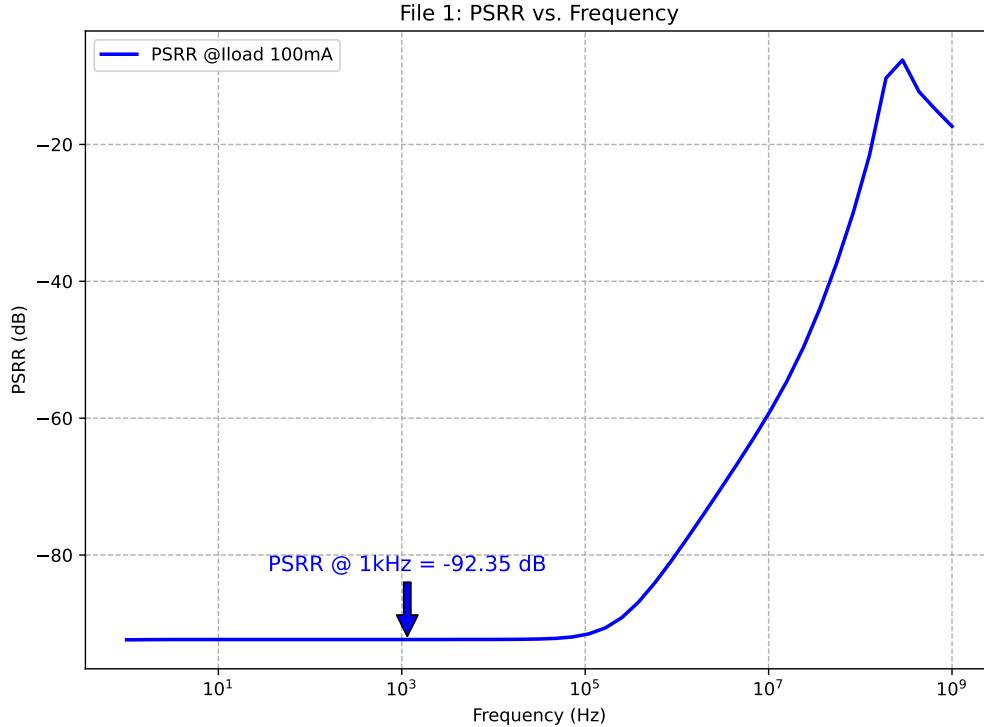


Figure 6.5: Case 1: PSRR Analysis at $V_{in} = 1.8V$ and $I_{load} = 100mA$

6.4.3 Transient Analysis

The transient performance of the LDO regulator for Case 1 is tested by observing the output voltage's response to load current changes. Figure 6.6 shows the transient response. It can be observed that it exhibits an undershoot value of less than 58.6mV and an overshoot of above 64mV shown in the yellow region.

The load current changes from 0 to 100mA. The overshoot requirement was set to be less than 60mV, which was not met. This discrepancy can be caused by the high Equivalent Series Resistance (ESR), which introduces undesirable high overshoots and undershoots during load transient responses. On the other hand, The ESR is useful to maintain system stability as only one of the poles can be canceled by the ESR zero [14].

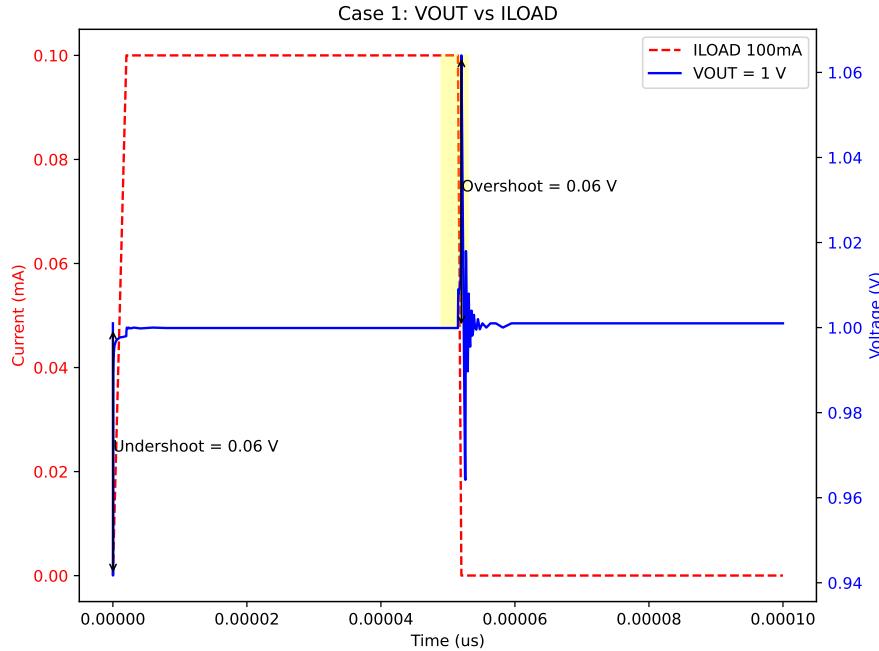


Figure 6.6: Case 1: Transient Response Analysis at $V_{in} = 1.8V$, I_{load} changing between 0 and 100mA

6.4.4 Case 2: Simulation Results and Analysis

The detailed simulation results for the Low-Dropout (LDO) regulator designed in 22nm FDSOI technology for Case 2 are presented in this section. This analysis focuses on key performance metrics such as input-output characteristics, frequency response, PSRR, and transient analysis.

The specifications for the LDO design in Case 2 are summarized in Table 6.4. These specifications include the output voltage, load current, input voltage, reference voltage, dropout voltage, PSRR, and output voltage ripple.

Parameter	Value
Output Voltage V_{out}	1.2 V
Load Current I_{load}	20 mA
Load Capacitor	30 pF
Input Voltage V_{in}	1.25 to 2 V
Reference Voltage V_{ref}	0.9 V
Dropout Voltage V_{DO}	< 200 mV at full load
PSRR	> 80 dB
Output Voltage Ripple	< 3%

Table 6.4: Specifications for Case 2 (1.2 V Output)

Input-output voltage characteristics

The input-output characteristics of the LDO regulator are obtained by sweeping the DC input voltage supply, as shown in Figure 6.7. The characteristics are obtained under maximum load current conditions ($I_{load} = 20\text{ mA}$) to verify the dropout voltage value. It can be observed from Figure 6.7 that the output voltage remains regulated for an input voltage ranging from 1.25V to 1.8V when the output is set to 1.2V. The dropout voltage can also be extracted from Figure 5.8. The dropout voltage in the dropout region is $V_{DO} = 196\text{ mV}$.

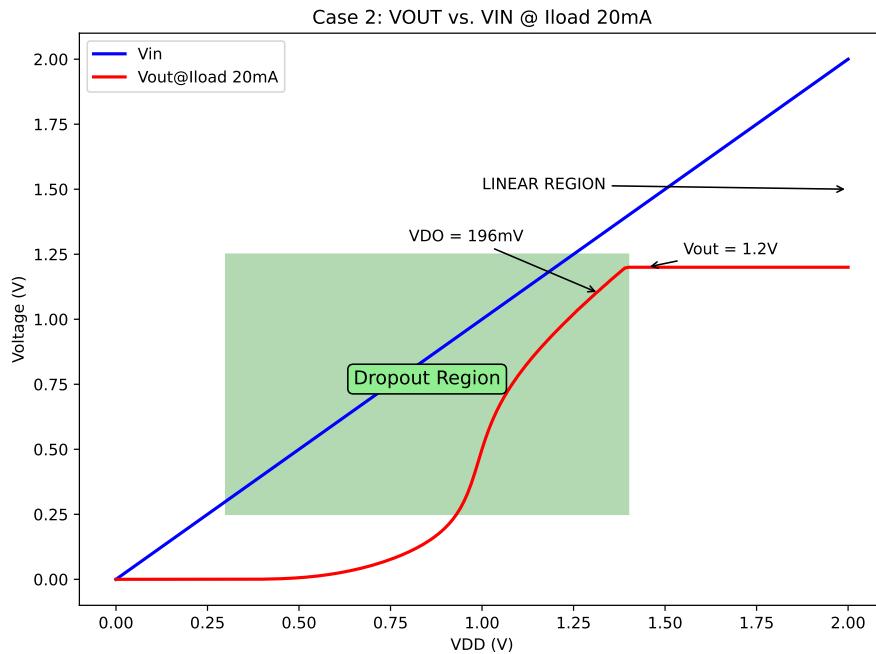


Figure 6.7: Input-output characteristics for Case 2: V_{OUT} vs. V_{IN} at $I_{load} = 20\text{ mA}$

6.4.5 Frequency Response

The frequency response of the LDO regulator at an input supply voltage of 1.8V and load currents of 20mA, with the output voltage set to 1.2V, is shown in Figure 6.8. The phase margin of 53 degrees achieved meets the specified criteria, ensuring stability.

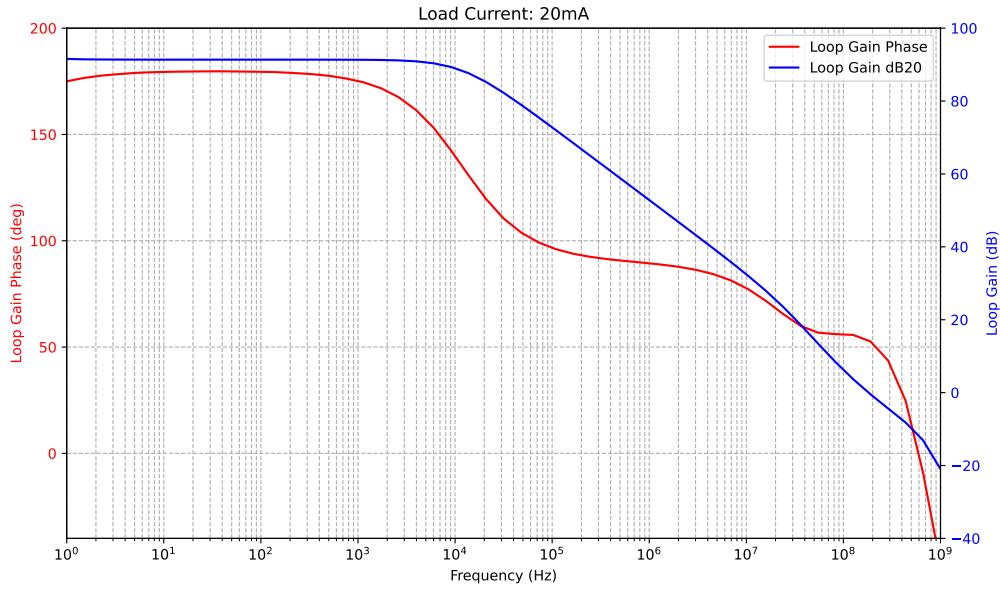


Figure 6.8: Gain and Phase Response for Case 2 at $I_{load} = 20 \text{ mA}$

Power Supply Rejection Ratio (PSRR)

The PSRR plot for Case 2, illustrated in Figure 6.9, shows that the PSRR meets the 80 dB requirement, confirming the design's effectiveness in rejecting power supply variations.

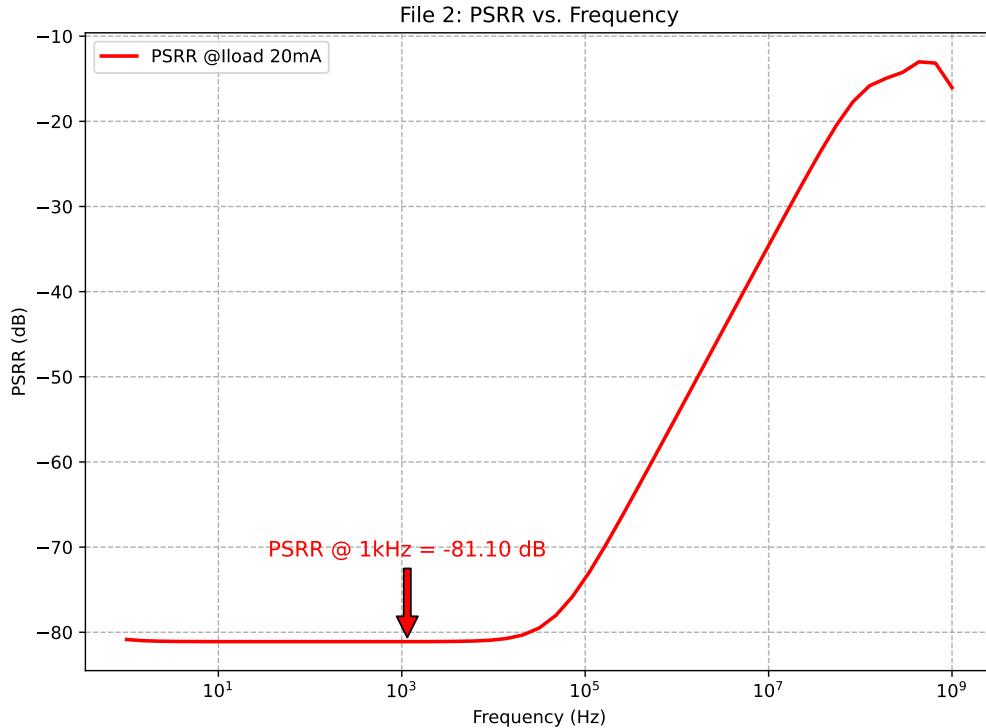


Figure 6.9: Case 2: PSRR Analysis at $V_{in} = 1.8V$ and $I_{load} = 20\text{mA}$

6.4.6 Transient Analysis

The transient performance of the LDO regulator for Case 2 is tested by observing the output voltage's response to load current changes. The undershoot and overshoot values are measured during transitions from minimum to maximum load current and vice versa. Figure 6.10 shows the transient response. It can be observed that it exhibits an undershoot value of below 20mV and an overshoot of below 30mV. The load current changes from 0 to 20mA.

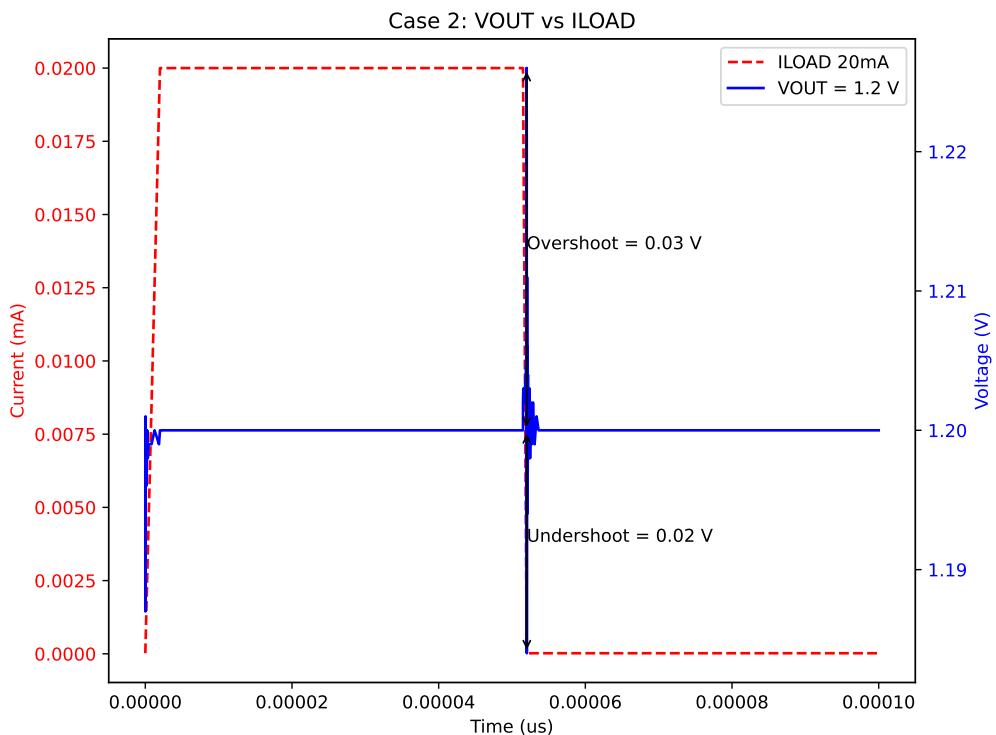


Figure 6.10: Case 2: Transient Response Analysis at $V_{in} = 1.8V$, I_{load} changing between 0 and 20mA

6.4.7 Case 2: Local Optimization Summary

The Cadence local optimization summary is presented in Table 6.5. The optimization process resulted in all parameters meeting the desired specifications, including PSRR, output voltage, and dropout voltage. While there were initial discrepancies in some values, such as the phase margin during the initial setup, these were successfully adjusted during the optimization process. The overall performance of the LDO, particularly in terms of PSRR and phase margin, was satisfactory. The initial conditions, including (W/L) ratios, bias currents, and compensation values, as well as the reference and final values, are shown in the table below 6.5.

Reference Variables			
W1, W3, W5, W6, W7, Cc, Rc, Cout, Wpass, RESR, Idc			
6.2 μ , 16 μ , 20 μ , 122 μ , 76 μ , 1.5p, 800, 30p, 1.2m, 0.1, 50 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	86.64 dB	> 80 dB	pass
LDO_Output_Voltage	1.2V	tol 1%	pass
LDO_DO	41.99mV	< 300mV	pass
Vout_Overshoot	18.22mV	< 30mV	pass
Vout_Undershoot	11.29mV	< 30mV	pass
Phase Margin	15.43°	> 50°	fail
Final Variables			
W1, W3, W5, W6, W7, Cc, Rc, Cout, R1, R2, Wpass, RESR, Idc			
10 μ , 8.6 μ , 9 μ , 112 μ , 70 μ , 3.1p, 2k, 30p, 2.1m, 0.1, 50 μ			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	81.1 dB	> 80 dB	pass
LDO_Output_Voltage	1.2V	tol 1%	pass
LDO_DO	196.2mV	< 300mV	pass
Vout_Overshoot	25.35mV	< 30mV	pass
Vout_Undershoot	15.84mV	< 30mV	pass
Phase Margin	53.24°	> 50°	pass

Table 6.5: Case 2: Local Optimization Summary

6.4.8 Case 3: Simulation Results and Analysis

This section presents the detailed simulation results for the Low-Dropout (LDO) regulator designed in 22nm FDSOI technology for Case 3. The analysis covers various performance metrics such as input-output characteristics, AC analysis, PSRR, and transient response. The specifications for the LDO design in Case 3 are summarized in Table 6.6.

Parameter	Value
Output Voltage V_{out}	1.5 V
Load Current I_{load}	50 mA
Input Voltage V_{in}	1.55 V to 2 V
Reference Voltage V_{ref}	0.9 V
Dropout Voltage V_{DO}	< 160 mV at full load
PSRR	> 75 dB
Output Voltage Ripple	< 50mV

Table 6.6: Specifications for Case 3 (1.5 V Output)

Input-output voltage characteristics

The input-output characteristics of the LDO regulator are obtained by sweeping the DC input voltage supply, as shown in Figure 5.13. The characteristics are obtained under maximum load current conditions ($I_{load} = 50 \text{ mA}$) to verify the dropout voltage value.

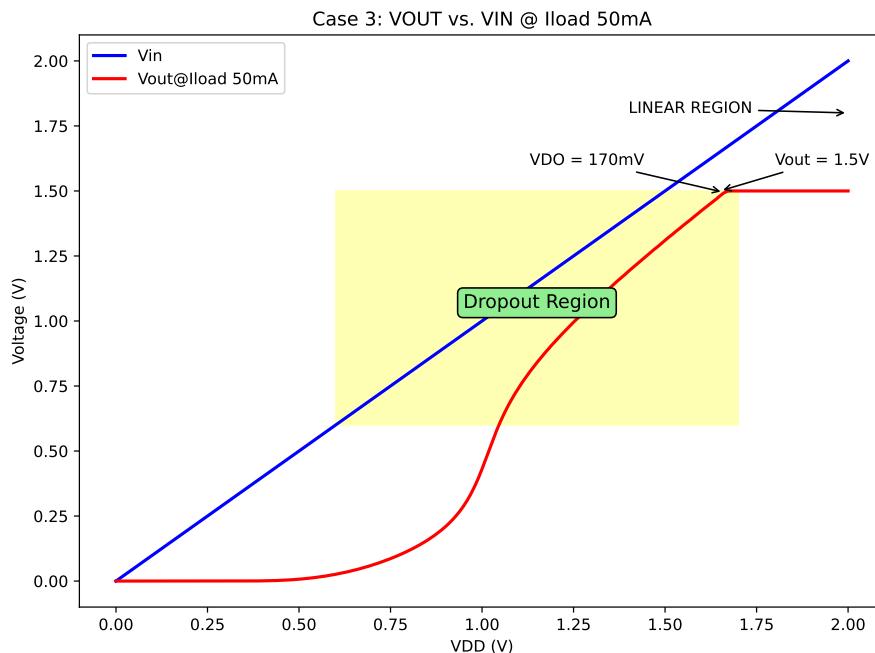


Figure 6.11: Input-output characteristics for Case 3: V_{OUT} vs. V_{IN} at $I_{load} = 50 \text{ mA}$

It can be observed from Figure 5.13 that the output voltage remains regulated for an input voltage ranging from 1.55V to 1.8V when the output is set to 1.5V. The dropout voltage can also be extracted from Figure 6.11, providing critical information about the LDO regulator's efficiency. The dropout voltage value in the dropout region is $V_{DO} = 170 \text{ mV}$ at $V_{OUT} = 1.5 \text{ V}$.

Frequency Response

The frequency response of the LDO regulator at an input supply voltage of 1.8V and load currents of 50mA, with the output voltage set to 1.5V. The phase margin > 50 degrees achieved meets the specified criteria, ensuring stability as shown in Figure 6.12 the frequency response plot.

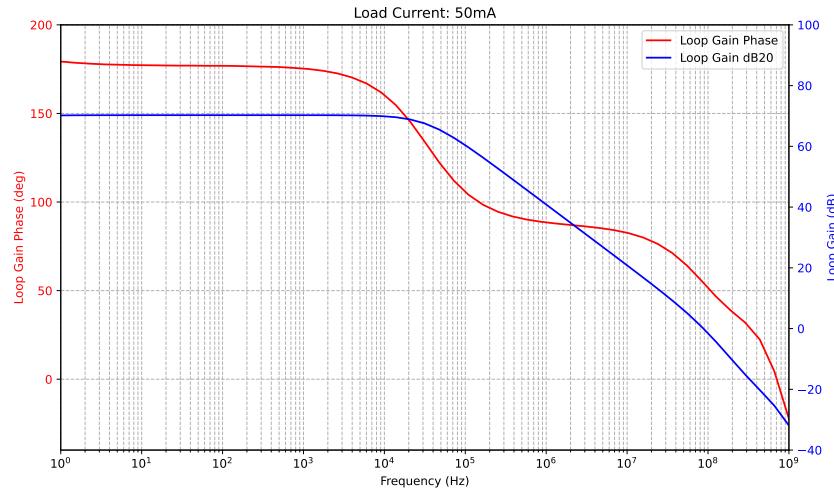


Figure 6.12: Gain and Phase Response for Case 3 at $I_{load} = 50$ mA

Power Supply Rejection Ratio (PSRR)

The PSRR plot for Case 3, illustrated in Figure 6.13, shows that the PSRR meets the 75 dB requirement, confirming the design's effectiveness in rejecting power supply variations.

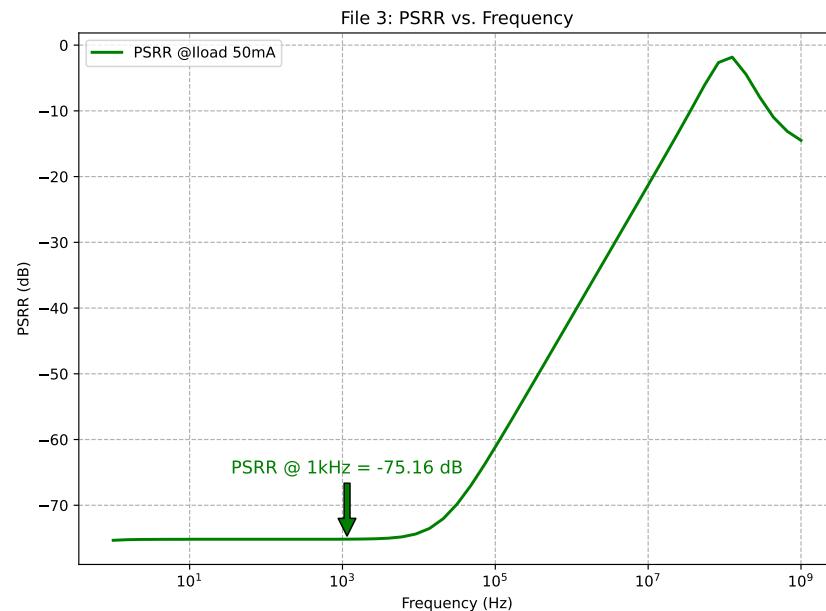


Figure 6.13: Case 3: PSRR Analysis at $V_{in} = 1.8V$ and $I_{load} = 50mA$

Transient Analysis

The transient performance of the LDO regulator for Case 3 is tested by observing the output voltage's response to load current changes. The undershoot and overshoot values are measured during transitions from minimum to maximum load current and vice versa. Figure 6.14 shows the transient response. It can be observed that it exhibits an undershoot value of 8.08mV and an overshoot of 10.92mV. The load current changes from 0 to 50mA. The overshoot requirement was set to be less than 50mV, which was satisfied.

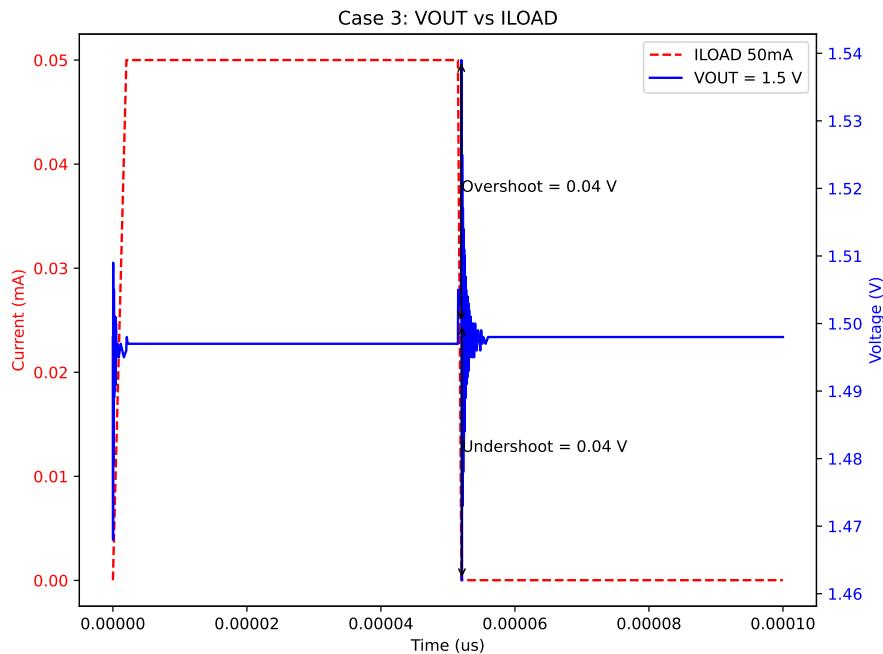


Figure 6.14: Case 3: Transient Response Analysis at $V_{in} = 1.8V$, I_{load} changing between 0 and 50mA

6.4.9 Case 3: Local Optimization Summary

The Cadence local optimization summary is presented in Table 6.7. While most parameters meet the desired specifications, there are some notable exceptions. The initial dropout voltage exceeded the set specification, and the PSRR did not meet the required standards. Despite these discrepancies, the overall performance of the LDO in terms of other parameters, such as the final PSRR and phase margin, was satisfactory after optimization. Initial conditions such as (W/L) ratios, bias currents, and compensation values are detailed, along with reference and final values, as shown in the table below 6.7.

Reference Variables			
M1, W3, W5, W6, W7, Cc, Rc, Cout, Wpass, Idc			
10 μ , 7 μ , 13 μ , 96 μ , 50 μ , 2.5p, 800, 150p, 3.75m, 75u			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	65.16 dB	> 75 dB	fail
LDO_Output_Voltage	1.498V	tol 1.5%	pass
LDO_DO	247.1mV	< 160mV	fail
Vout_Overshoot	88.27mV	< 50mV	fail
Vout_Undershoot	77.1mV	< 50mV	fail
Phase Margin	67.34°	> 50°	pass
Final Variables			
M1, W3, W5, W6, W7, Cc, Rc, Cout, Wpass, Idc			
16 μ , 4.5 μ , 5 μ , 136 μ , 65 μ , 5.1p, 1.22k, 150p, 4.2m, 100u			
Parameter	Final Value	Spec	Pass/Fail
Output Specifications			
PSRR_LDO_@1KHz	75.16 dB	> 75 dB	pass
LDO_Output_Voltage	1.498V	tol 1.5%	pass
LDO_DO	187.1mV	< 160mV	fail
Vout_Overshoot	10.92mV	< 50mV	pass
Vout_Undershoot	8.08mV	< 50mV	pass
Phase Margin	57.34°	> 50°	pass

Table 6.7: Case 3: Local Optimization Summary

6.5 Conclusion

In this chapter, detailed simulation results and analyses for three different cases of Low-Dropout (LDO) regulator designs using 22nm FDSOI technology were presented. Each case was meticulously optimized for specific parameters, including output voltage, load current, input voltage, dropout voltage, PSRR, and output voltage ripple.

Utilizing the BFGS algorithm for local optimization, it was ensured that most parameters met the desired specifications, although there were minor deviations in some cases. For instance, Case 1 showed a higher-than-expected dropout voltage due to the increased size of the pass transistor, and Case 2 had a slight deviation in the overshoot voltage. Despite these discrepancies, the overall performance of the LDO regulators was satisfactory, with parameters like PSRR and phase margin meeting the required standards.

This comprehensive optimization and validation process demonstrates the efficacy of the BFGS algorithm in fine-tuning the LDO designs to achieve optimal performance. Initial conditions, such as (W/L) ratios, bias currents, and compensation values, were crucial in setting up the simulations and are documented in Appendix 10.5.

The transition to 22nm FDSOI technology has shown promising results, significantly enhancing the power efficiency and stability of the LDO regulators due to improved control over the threshold voltage and reduced leakage currents. This chapter underscores the adaptability and scalability of our proposed design methodology across different semiconductor technologies, highlighting its potential for future advancements in LDO design.

In summary, the successful implementation and optimization of LDO regulators in 22nm FDSOI technology pave the way for further research and development in this field. Future work will focus on exploring even smaller technology nodes, integrating more complex functionalities, and continuing to refine the optimization algorithms to push the boundaries of LDO performance and efficiency.

Chapter 7

Conclusion

This thesis has presented a comprehensive study and implementation of Low-Dropout voltage regulators (LDOs) in two advanced semiconductor technologies: 130nm BCD and 22nm FDSOI. The work has aimed to address the increasing demand for efficient, stable, and low-power voltage regulation in modern, highly integrated electronic systems. The primary contributions of this research are summarized as follows:

- **Design Methodology:** A robust design methodology has been developed, integrating advanced optimization techniques with practical circuit design considerations. This approach ensures that the LDOs meet stringent performance specifications such as low dropout voltage, high power supply rejection ratio (PSRR), low quiescent current, and stable transient response.
- **Optimization Techniques:** Various optimization algorithms, including BFGS, Conjugate Gradient, Brent-Powell, and Hooke-Jeeves, were implemented and compared. Each algorithm's effectiveness in fine-tuning the design parameters to achieve optimal performance was thoroughly analyzed, highlighting the strengths and limitations of each approach.
- **Implementation in 130nm BCD Technology:** The LDO design in 130nm BCD technology demonstrated the practical application of the proposed methodology. Detailed simulation results confirmed that the designed LDO met the required specifications, including maintaining a stable output voltage under varying input and load conditions.
- **Implementation in 22nm FDSOI Technology:** Adapting the design methodology to 22nm FDSOI technology showcased its versatility and scalability. The design achieved enhanced performance metrics, benefiting from the advanced features of FDSOI technology, such as reduced leakage currents and improved threshold voltage control.
- **Simulation and Analysis:** Extensive simulation studies were conducted for both technologies, providing in-depth insights into the LDO's behavior under different operating conditions. Key performance parameters such as dropout voltage, PSRR, transient response, and stability were rigorously evaluated, demonstrating the robustness of the proposed design methodology.

The findings of this research underline the critical importance of integrating advanced optimization techniques with practical circuit design principles to develop high-performance LDOs. The proposed methodology not only enhances the efficiency and reliability of LDOs but also offers a scalable approach applicable to different semiconductor technologies.

7.1 Future Work

While this thesis has made significant strides in LDO design, several areas warrant further exploration:

- **Advanced Compensation Techniques:** Further investigation into more sophisticated compensation techniques could enhance the stability and transient response of LDOs, especially in ultra-low power applications.
- **PVT Corner Variations:** Analyzing the performance of the designed LDOs under Process, Voltage, and Temperature (PVT) corner variations could provide a more comprehensive understanding of their reliability in real-world scenarios.
- **Integration with Other Power Management Units:** Exploring the integration of LDOs with other power management units (PMUs) could lead to more efficient and compact power solutions for complex systems-on-chip (SoCs).
- **Fabrication and Testing:** Fabricating the designed LDOs and conducting real-world testing would validate the simulation results and provide practical insights into the design's performance and manufacturability.

In conclusion, this thesis has laid a strong foundation for the efficient design of LDOs in advanced semiconductor technologies, contributing valuable methodologies and insights to the field of analog and mixed-signal integrated circuit design.

Chapter 8

Appendix

8.1 Python Code

```
1 # ===== Specifications =====
2 Vdd = float(input("input value of Vdd="))
3 Vss = float(input("input value of Vss="))
4 SR = float(input("input value of SR="))
5 GB = float(input("input value of GB="))
6 Cl = float(input("input value of Cl="))
7 phi = float(input("input value of Phi="))
8
9
10
11 ##### LDO_Specifications #####
12 Iload_LDO = float(input("input value of Iload="))
13 C_out_LDO = float(input("input value of Cout="))
14 LDO_DO = float(input("input value of LDO_DO="))
15 Vout_LDO = float(input("input value of Vout_LDO="))
16 V_Ref = 1.2
17
18
19 ##### Physical constants and process
20
21 ##### Auxiliar derived quantities
22
23 ##### Design steps =====
24 # (1) Compensation Capacitor Cc
25 Cc = 0.3 * Cl
26
27 # Form factor of Mosfet 1 and Mosfet 2
28 gm1 = omega1 * Cc
29
30 # (2) Current of Mosfet 5
31 I5 = Cc * SR
32 Ibias = I5
```

```

33 I8 = I5
34
35 I1 = I5 / 2; I2 = I1
36 I3 = I1; I4 = I2
37
38 # (3) Form factor of Mosfet 1 and Mosfet 2
39 gm2 = gm1
40 S1 = (gm1 ** 2) / (2 * k_n * I1)
41 S2 = S1 # Balanced differential pair
42
43
44 # (4) Length Mosfet 3 & 4
45 Vdsat3 = Vdd - Vin_cm_max - Vtp + Vtn
46 S3 = I5 / (k_p * (Vdsat3 ** 2))
47 S4 = S3
48 gm4 = np.sqrt(2 * k_p * S4 * I4)
49 gm3 = gm4
50
51 # Compute gm/ID ratios
52
53 gm1_id_ratio = gm1 / I1
54 # gm/ID for Mosfet 1
55 gm4_id_ratio = gm4 / I4
56 # gm/ID for Mosfet 4
57
58 # Use the interpolate_gds_id function for NMOS1
59 nmos1_filename = 'nmos1.dat',
60 gds_id_interpolated_nmos1 =
61 interpolate_gds_id(nmos1_filename, [gm1_id_ratio])
62 Ln1 = gds_id_interpolated_nmos1[0]
63 print(f"Interpolated gds/Id for NMOS1:
64 {gds_id_interpolated_nmos1[0]}")
65
66 # Use the interpolate_Cgg function for NMOS1
67
68 cgg1_interpolated_nmos1 =
69 interpolate_cgg(nmos1_filename, [gm1_id_ratio])
70
71 Cgg_1 = cgg1_interpolated_nmos1[0]
72 print(f"Interpolated Cgg for NMOS1: {Cgg_1}")
73
74
75 # Use the interpolate_gds_id function for PMOS3
76 pmos3_filename = 'pmos3.dat',
77 gds_id_interpolated_pmos3 =
78 interpolate_gds_id(pmos3_filename, [gm4_id_ratio])
79 Lp1 = gds_id_interpolated_pmos3[0]
80 # Assuming you want the first (and only)

```

```

81 | interpolated value
82 | print(f"Interpolated gds/Id for PMOS3:
83 | {gds_id_interpolated_pmos3[0]}")
84 |
85 |
86 | # Use the interpolate_Cgg function for PMOS3
87 | cgg3_interpolated_pmos3 =
88 | interpolate_cgg(pmos3_filename, [gm4_id_ratio])
89 |
90 | Cgg_3 = cgg3_interpolated_pmos3[0]
91 | print(f"Interpolated Cgg for PMOS3: {Cgg_3}")
92 |
93 | # Use Ln1 and Lp1 in your subsequent calculations
94 | gds2 = I2 * Ln1
95 | gds4 = I2 * Lp1
96 |
97 | # (4) Width Mosfet 5 & 8
98 | Vdsat5 = Vin_cm_min - Vss -
99 | np.sqrt(2 * I5 * 10e-6 / k_n * S1) - Vtn_max
100 | S5 = 2 * I5 / (k_n * (Vdsat5 ** 2))
101 | S8 = S5
102 |
103 | # (5) For more than 60 Phase margin and Mosfet 6
104 | gm6_sym = gm1 * C1 / (Cc * sp.tan(sp.rad(85 - phi)))
105 | gm6 = gm6_sym.evalf()
106 |
107 |
108 |
109 | # L6 calculation
110 | S6 = (gm6 / gm4) * S4
111 | I6 = gm6 ** 2 / (2 * k_p * S6)
112 | I7 = I6
113 |
114 |
115 | # (7) Form factor of Mosfet 7
116 | S77 = ((I7 / I5) * S5)
117 | S7 = S77
118 | gm7 = np.sqrt(2 * k_p * S7 * I7)
119 |
120 |
121 | # Compute gm/ID ratios
122 |
123 | gm6_id_ratio = gm6 / I6
124 | # gm/ID for Mosfet 1
125 | gm7_id_ratio = gm7 / I7
126 | # gm/ID for Mosfet 4
127 |
128 | # Use the interpolate_gds_id

```

```

129 function for NMOS7
130 nmos7_filename = 'nmos7.dat',
131 gds_id_interpolated_nmos7 =
132 interpolate_gds_id(nmos7_filename, [gm7_id_ratio])
133 Ln2 = gds_id_interpolated_nmos7[0]
134 print(f"Interpolated gds/Id for
135 NMOS7: {gds_id_interpolated_nmos7[0]}")
136
137
138 # Use the interpolate
139 Cgg function for NMOS7
140
141
142 cgg7_interpolated_nmos7 =
143 interpolate_cgg(nmos1_filename, [gm7_id_ratio])
144
145 Cgg_7 = cgg7_interpolated_nmos7[0]
146 print(f"Interpolated Cgg for
147 NMOS7: {Cgg_7}")
148
149
150 # Use the interpolate_gds_id function for PMOS6
151 pmos6_filename = 'pmos7.dat',
152 gds_id_interpolated_pmos6 =
153 interpolate_gds_id(pmos6_filename, [gm6_id_ratio])
154 Lp2 = gds_id_interpolated_pmos6[0]
155 # Assuming you want the first (and only)
156 interpolated value
157 print(f"Interpolated gds/Id for
158 PMOS6: {gds_id_interpolated_pmos6[0]}")
159
160 # Use the interpolate Cgg function for PMOS6
161
162
163 cgg1_interpolated_pmos6 =
164 interpolate_cgg(nmos1_filename, [gm6_id_ratio])
165
166 Cgg_6 = cgg1_interpolated_pmos6[0]
167 print(f"Interpolated Cgg for PMOS6: {Cgg_6}")
168
169
170 # Use Ln1 and Lp1 in your subsequent calculations
171 gds6 = I6 * Lp2
172 gds7 = I7 * Ln2
173
174
175 # (10) Compensation resistor
176 Rc = (2 / gm6)

```

```

177
178 # Total dissipated power
179 P = Vdd * (I6 + I5)
180
181 Av1 = (gm1) / (gds2+gds4)
182
183 Av2 = (2 * gm6) / (gds6+gds7)
184
185 R1 = (1/ (gds2+gds4))
186 R2 = (1/ (gds6+ gds7))
187
188 C1 = 2* Cgg_1+Cgg_3 + Cc
189 C2 = Cgg_6+Cgg_7 + C1
190
191
192 # gain at DC
193 Av_cal = 20 * np.log10(Av1*Av2)
194
195 # Width of Pass transistor
196 S_pass = 2 * Iload_LDO / (k_p * (LDO_DO ** 2))
197
198 #Feedback Netwrok
199 Rf2 = 100e3
200 Rf1 = (Vout_LDO/V_Ref - 1)* Rf2
201
202 # poles and zero calculation
203
204 GBW = -gm1/(2*np.pi*Cc);
205 P1 = -gm1/(2*np.pi*Av_cal*Cc);
206 P2 = -gm6/(2*np.pi*C1);
207 P3 = -gm3/(2*0.667*W3*L*C_ox);
208 Z1 = -gm6/(2*np.pi*Cc);
209
210 # Define symbolic variables
211 s, v1, vs, vout = sp.symbols('s v1 vs vout')
212 gm1_sym, gm6_sym, R1_sym, R2_sym, C1_sym, C2_sym,
213 Cc_sym, Rc_sym, vs_sym =
214 sp.symbols('gm1 gm6 R1 R2 C1 C2 Cc Rc vs')
215
216
217 # Define the equations
218 eq1 = sp.Eq(-gm1_sym * vs + v1/R1_sym
219 + v1*s*C1_sym + (v1-v2)*s*Cc_sym/(1+s*Cc_sym*Rc_sym), 0)
220
221 eq2 = sp.Eq(gm2_sym * v1 + v2/R2_sym
222 + (v2-v1)*s*Cc_sym/(1+s*Cc_sym*Rc_sym)
223 + v2*s*C2_sym + (v2-vout)*s*Cgd_sym, 0)
224

```

```

225 eq3 = sp.Eq(gmp_sym * v2 + vout/rop_sym
226 + vout*s*Cout_sym
227 /(1 + s*Cout_sym*Resr_sym), 0)
228
229 eq4 = sp.Eq(vfb - (vout * Rf2_sym)
230 /(Rf1_sym + Rf2_sym), 0)
231
232
233 # Solve the equations for v1 and vo
234 solution = sp.solve([eq1, eq2, eq3, eq4],
235 (v1, v2, vout, vfb))
236 vs = 1
237
238 # Define DC gain
239 Av = gm1_sym*R1_sym*(gm2_sym*R2_sym)
240 *gmp_sym*rop_sym*
241 (Rf2_sym/(Rf2_sym+Rf1_sym))
242
243 ## Get Num and Den of
244 vout/vs after substituting vout
245
246 vout_vs = solution[vout]/vs
247 n, d = sp.fraction(vout_vs)

```

8.2 Initial Calculations Results

Input Specifications Provided: DESIGN 1

Vdd = 1.8 V
 Vss = 0 V
 Slew Rate (SR) = 10e6 V/s
 Load Capacitor (Cl) = 10e-12 F
 Gain Bandwidth Product (GB) = 20e6 Hz
 Phase Margin (Phi) = 60 degrees

Interpolated Parameters:

Interpolated gds/Id for NMOS1: 0.026889347699308598
 Interpolated Cgg for NMOS1: 1.3974341459636575e-14 F
 Interpolated gds/Id for PMOS3: 0.04594729897025933
 Interpolated Cgg for PMOS3: 2.4133226781313362e-14 F
 Interpolated gds/Id for NMOS7: 0.014844180374179115
 Interpolated Cgg for NMOS7: 2.2903440676437792e-14 F
 Interpolated gds/Id for PMOS6: 0.045509110493756715
 Interpolated Cgg for PMOS6: 2.183199582387732e-14 F

Calculated Component Values:

Compensation Capacitor (C_c): 3 pF
 Compensation Resistor (R_c): 663.146 Ohm
 Bias Current (I_{bias}): 30 uA
 Input Common-Mode Range Plus (ICMR+): 1.75 V
 Input Common-Mode Range Minus (ICMR-): 0.6 V

MOSFET Sizing:

MOSFET	Width (W) [nm]	Length (L) [nm]	Size (S) [nm/nm]
M1	1400.715	150	9.39
M2	1400.715	150	9.39
M3	969.828	150	6.466
M4	969.828	150	6.466
M5	1244.542	150	8.297
M6	14624.655	150	97.498
M7	9383.624	150	62.557
M8	1244.542	150	8.297

Drain Currents:

Current	Value (uA)
I1	15.000
I2	15.000
I3	15.000
I4	15.000
I5	30.000
I6	226.195
I7	226.195
I8	30.000

Transconductance Values (gm) and Resistances

- $gm_1 = 0.000376 \text{ V/V}$
- $gm_6 = 0.002 \text{ V/V}$
- $R_1 = 915290.169 \text{ ohm}$
- $R_2 = 73251.526 \text{ ohm}$
- $C_1 = 3.05 \text{ pF}$
- $C_2 = 10.136 \text{ pF}$

Power and Gain

- Static Power: $P = 461.150 \text{ uW}$
- Open-Loop Gain: $A_v = 96 \text{ dB}$

Frequency Response

- Dominant Pole: $P_1 = 0.198 \text{ MHz}$
- Gain Bandwidth Product (GBW): 20.000 MHz
- Non-Dominant Pole: $P_2 = 36.000 \text{ MHz}$
- Third Pole: $P_3 = 26860.632 \text{ MHz}$
- LHP Zero: $Z_1 = 120.000 \text{ MHz}$

8.3 Design 1 Variables Sweeping Setup

- C_C (Compensation Capacitor): Range from 1 pF to 5 pF
- W_1 : Range from 6 μm to 12 μm
- W_4 : Range from 46 μm to 50 μm
- W_5 : Range from 26 μm to 32 μm
- W_6 : Range from 620 μm to 680 μm
- W_7 : Range from 150 μm to 170 μm
- R_C (Compensation Resistor): Range from 300 kOhm to 600 kOhm

Design 1 Parameters:

- Gain: Maximize (Target: 70 dB)
- Phase Margin: Greater than 60 degrees
- Slew Rate: Less than 11 V/ μs
- UGF: Greater than 20 MHz
- Transistor Regions: Ensuring correct operation regions for M1, M3, M5, M6, and M7

BFGS Algorithm Setup:

- Algorithm: BFGS
- Evaluation: Full
- Starting Point: Initial Design Variables
- Stopping Criteria: All specifications met

Design 1		Design 2		Design 3	
Parameter	Value	Parameter	Value	Parameter	Value
C _c	3 pF	C _c	1.5 pF	C _c	1.2 pF
R _c	663 Ohm	R _c	425 Ohm	R _c	350 Ohm
I _{dc}	30 μ A	I _{dc}	45 μ A	I _{dc}	50 μ A
M1	9.39 μ m	M1	16 μ m	M1	22 μ m
M2	9.39 μ m	M2	16 μ m	M2	22 μ m
M3	6.466 μ m	M3	9.7 μ m	M3	10.3 μ m
M4	6.466 μ m	M4	9.7 μ m	M4	10.3 μ m
M5	8.297 μ m	M5	12.7 μ m	M5	13.5 μ m
M6	97.498 μ m	M6	202 μ m	M6	243.7 μ m
M7	62.557 μ m	M7	130 μ m	M7	162 μ m
M8	8.297 μ m	M8	12.7 μ m	M8	13.5 μ m

Table 8.1: MOSFET Sizing for Design 1, Design 2, and Design 3

MOSFET Sizing for Design 1, Design 2, and Design 3:

Note: - All sizes (W) are given in micrometers (μ m). - I_{dc} values are given in microamperes (μ A).

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