

East West University
Course Title: Computer Architecture
Course Code: CSE360, Fall 2025
Assignment 1

Question 1: Performance Metrics of Different Architectures

Two processors, P1 and P2, operate at 2 GHz and 1.5 GHz respectively. P1 uses a RISC architecture, requiring 4 cycles on average for each instruction. P2 uses a CISC architecture, with an average of 12 cycles per instruction but executes 3 instructions per cycle due to its complex instruction set.

- Calculate the MIPS (Million Instructions Per Second) for both processors.
- Determine which processor has a higher instruction throughput and justify your answer.

Question 2: Pipeline Processing and Throughput

A 5-stage pipeline has the following stage delays: 3 ns, 2 ns, 4 ns, 5 ns, and 2 ns.

- Calculate the clock cycle time based on the slowest pipeline stage.
- Determine the ideal throughput of the pipeline.
- If there is a structural hazard that forces every third instruction to wait for an additional cycle, calculate the actual throughput.

Question 3: Superscalar Processor Performance

A superscalar processor can issue up to 3 instructions per cycle and has a branch misprediction penalty of 5 cycles. Assume the instruction mix and their frequencies in a program are as follows: 30% loads/stores, 20% branches (with a 2% misprediction rate), and 50% ALU operations.

- Calculate the effective CPI (Cycles Per Instruction) for this processor.
- If the processor clock rate is 2 GHz, estimate the execution time for a program with 1 million instructions.

Question 4: Multilevel Cache and Main Memory Access

A system uses a 3-level cache hierarchy (L1, L2, L3) before accessing main memory. The access times and miss rates are as follows: L1 cache - 1 ns and 1%, L2 cache - 3 ns and 5%, L3 cache - 10 ns and 10%, and main memory access time is 100 ns.

- Calculate the effective access time for this system.
- If improving the L3 cache miss rate by 2% increases its access time by 1 ns, what is the new effective access time, and is the trade-off worthwhile?

Question 5: Address Translation and Virtual Memory

A computer uses a 4-level hierarchical page table for address translation with a 64-bit virtual address space and 4 KB page size. Each page table entry is 8 bytes.

- a) Calculate the size of each page table level.
- b) If the Translation Lookaside Buffer (TLB) hit rate is 95% and the memory access time is 100ns, estimate the effective memory access time considering a TLB access time of 1 ns and a 2-level page table walk.

Question 6: Addressing and Memory Organization

A system uses 24-bit addresses and has a 4 MB memory. It uses a 2-level paging scheme with a page size of 1 KB. The first level page table has 256 entries.

- a) Calculate the number of bits for the second level page table entries.
- b) Determine the size of a second level page table if each entry is 4 bytes.

Question 7: Representing Instructions in the Computer

An integer array B has its base address in \$s4. You want to load B[13] into \$t5.

- a) Compute the byte offset for B[13].
- b) Write the corresponding I-format instruction in standard MIPS syntax:

lw \$t5, offset(\$s4)

- c) Using the I-format layout, write the decimal values for each field.
- d) Encode the full 32-bit binary word and then convert it to hexadecimal.

Instructions for Students:

- There should be a proper front page with name, ID, section, assignment no etc.
- Show all your work clearly and concisely.
- Solve the problems with different data, not the data given in the questions.
- Justify your answers with proper reasoning.
- Where assumptions are needed, state them clearly.