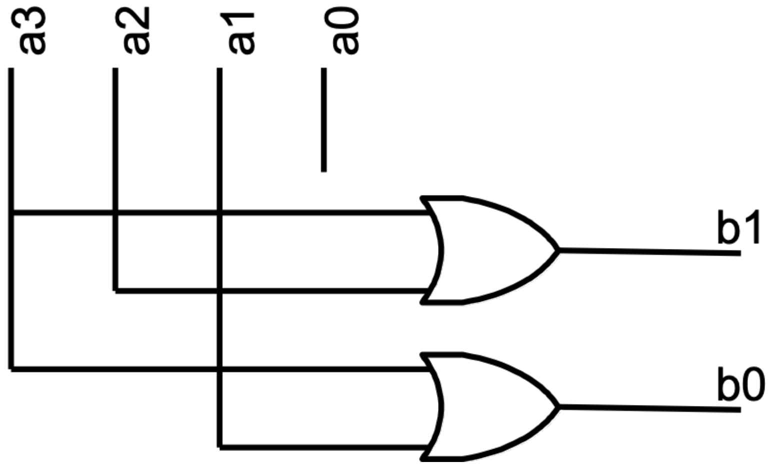
Encoders

Encoder (1/3)

- An encoder is an inverse of a decoder
  - Converts a one-hot input signal to a binary-encoded output signal
  - Other input patterns are forbidden in the truth table
- Example: a 4-to-2 encoder

a3	a2	a1	a0	b1	b0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



$$b_0 = a_3 + a_1$$

$$b_1 = a_3 + a_2$$

Encoders (2/3)

- A combinational logic that performs the inverse operation of a decoder
  - Only one input has value 1 at any given time
  - Can be implemented with OR gates

$x = D_4 + D_5 + D_6 + D_7$

$y = D_2 + D_3 + D_6 + D_7$

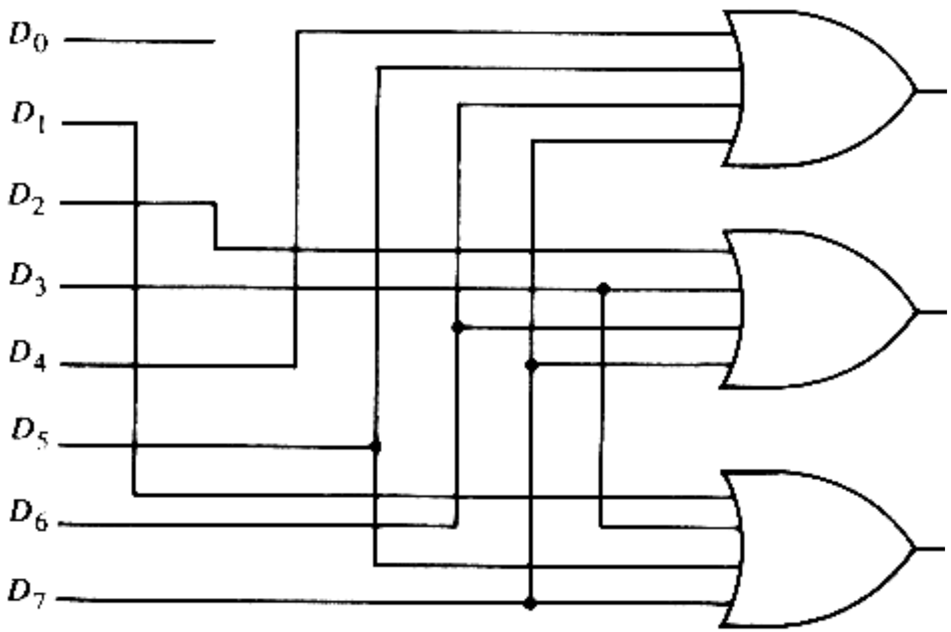
$z = D_1 + D_3 + D_5 + D_7$

8-to-3 encoder

Truth Table of an Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Encoders (3/3)



$x = D_4 + D_5 + D_6 + D_7$

$y = D_2 + D_3 + D_6 + D_7$

$z = D_1 + D_3 + D_5 + D_7$

- **Limitations** Illegal Inputs
  - When both D_3 an D_6 go high, output will be 111 → ambiguity
  - Use priority encoder!

Priority Encoders (1/2)

- Ensure only one of the input is encoded
- D_3 has the highest priority, while D_0 has the lowest priority
- X is the don't care conditions
- V is the valid output indicator

status flag

Truth Table of a Priority Encoder

Inputs				Outputs		valid
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

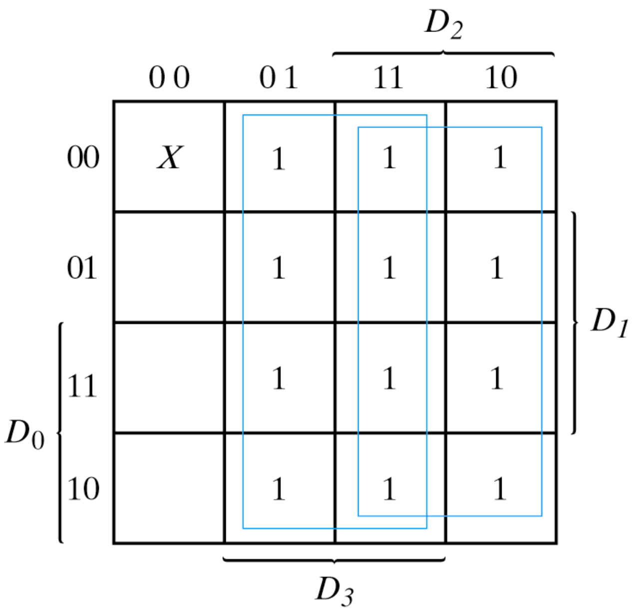
don't care

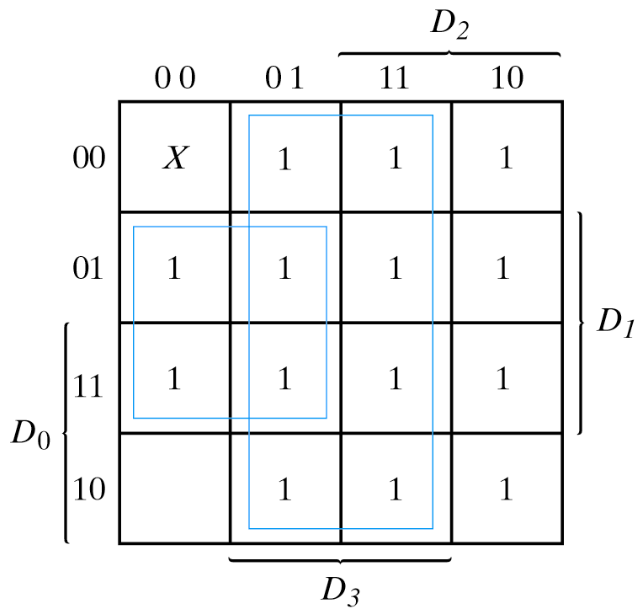
2 minterms

4 "

8 "

Priority Encoders (2/2)

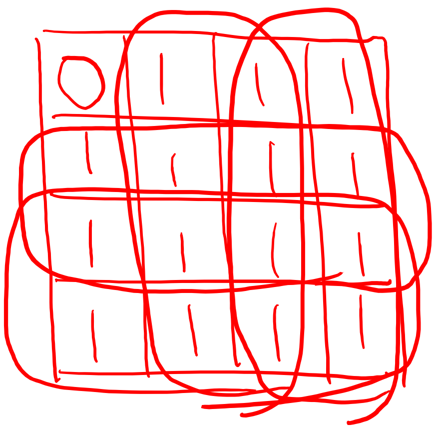


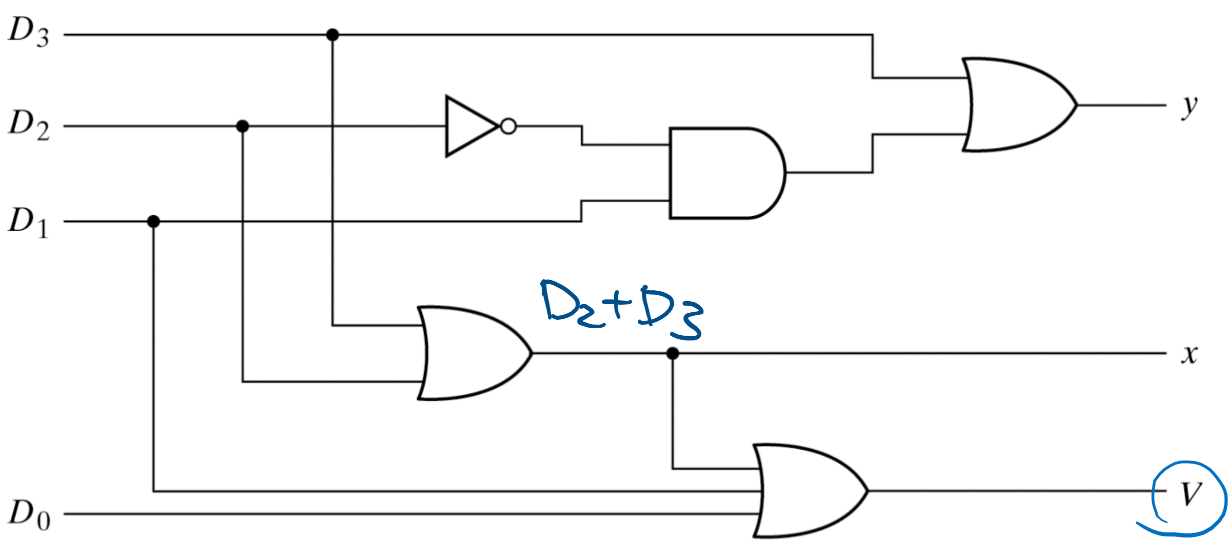


$x = D_2 + D_3$

$y = D_3 + D_1 D_2'$

$V = D_0 + D_1 + \underbrace{(D_2 + D_3)}_{x}$





Multiplexer

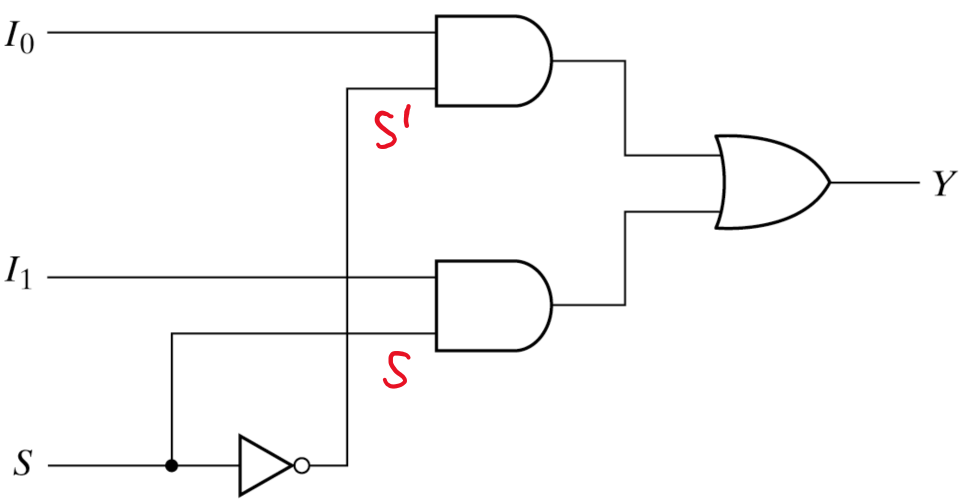
Multiplexers

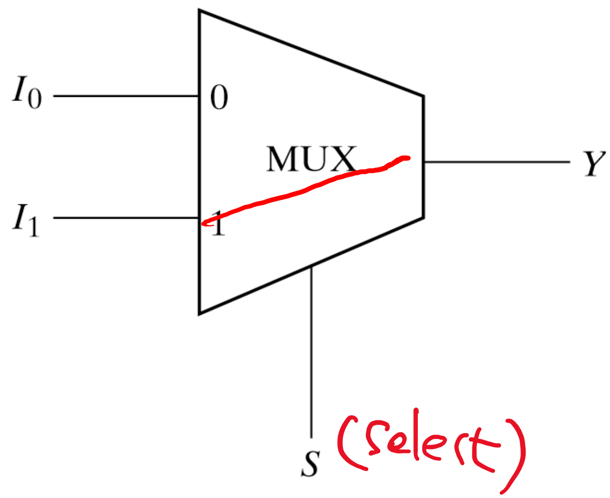
- A multiplexer (or MUX) selects (usually by *n* select lines) binary information from one of many (usually 2^n) input lines and directs it to a single output line
- 2-to-1 MUX (2:1 MUX)

if (s) Y = I1
else Y = I0

S	Y
0	I_0
1	I_1

$$Y = S'I_0 + SI_1$$

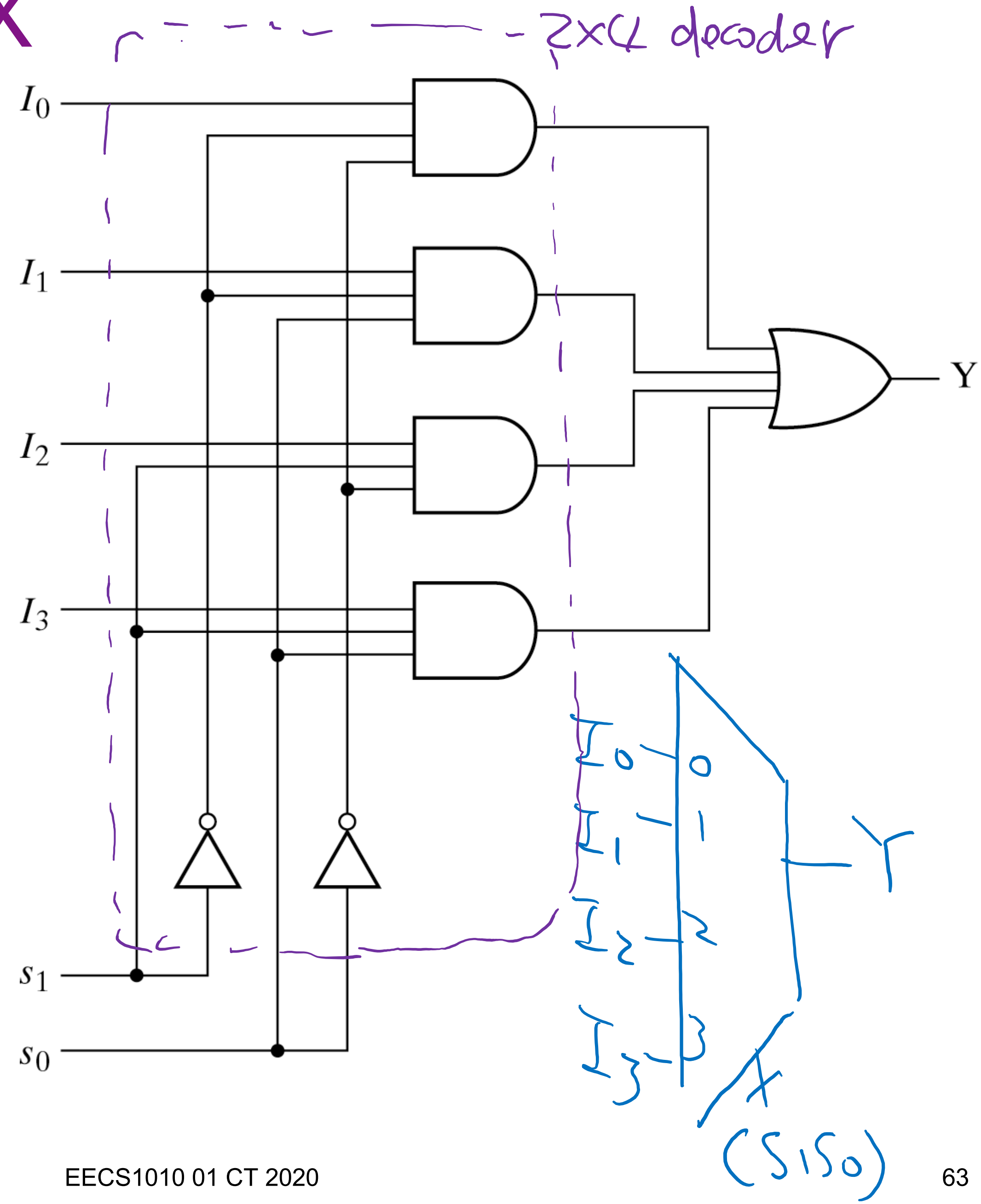




4-to-1-line MUX

s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$



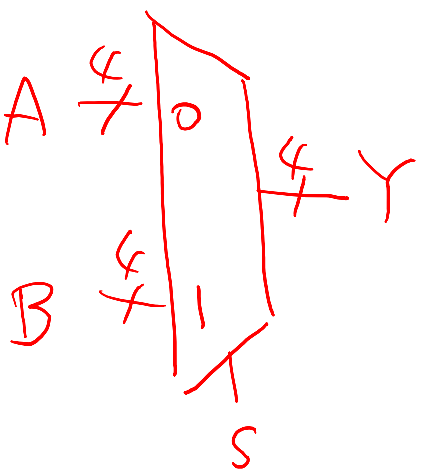
Quadruple 2-to-1-line MUX

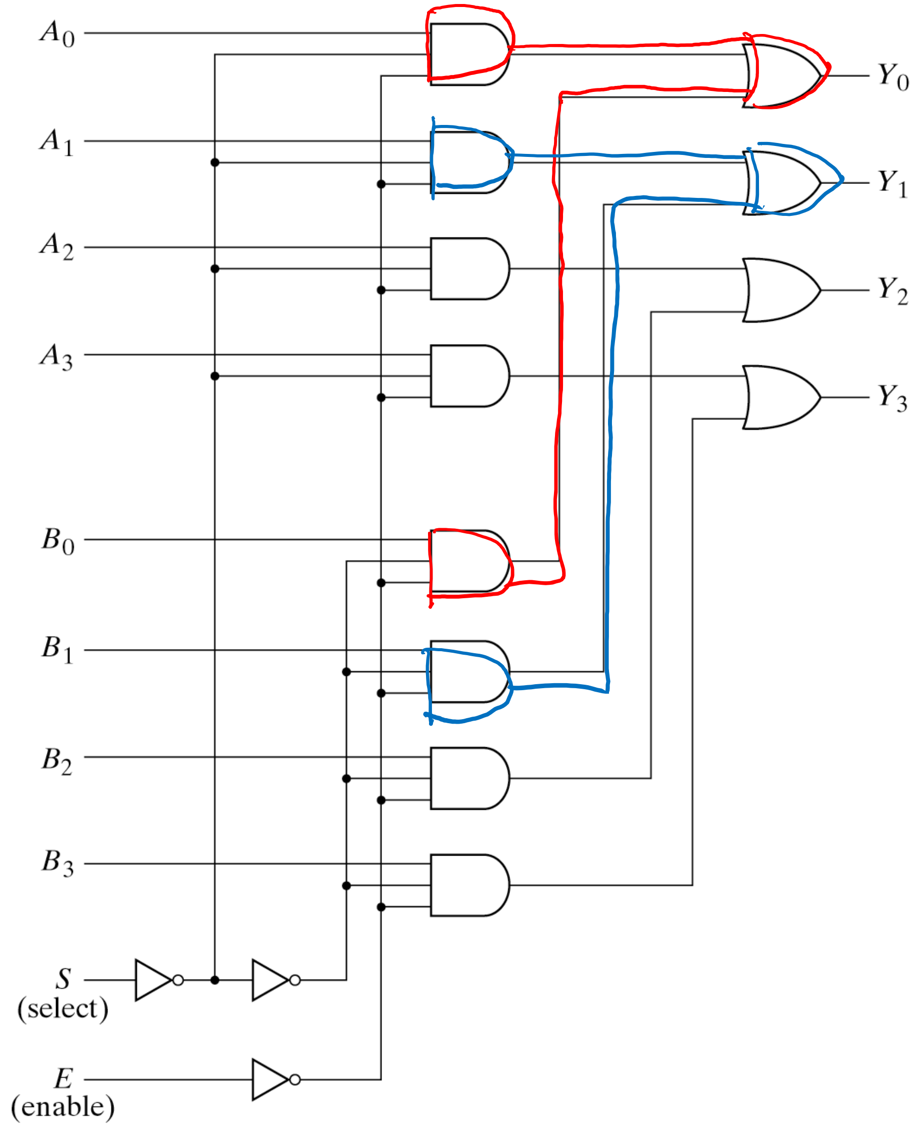
Function table

E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B

Two 4-bit vectors

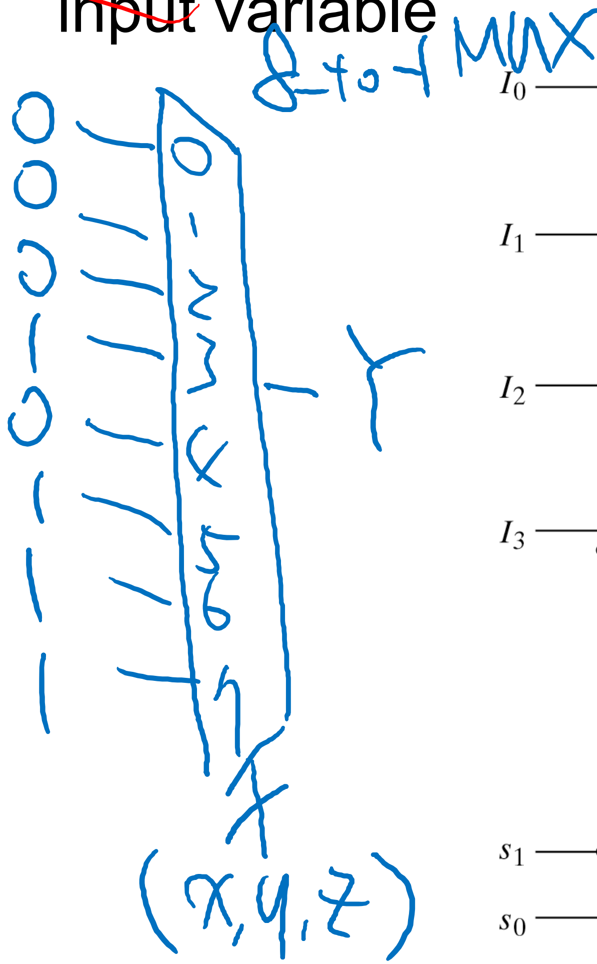
$\Rightarrow$ 4 2-to-1 MUXes

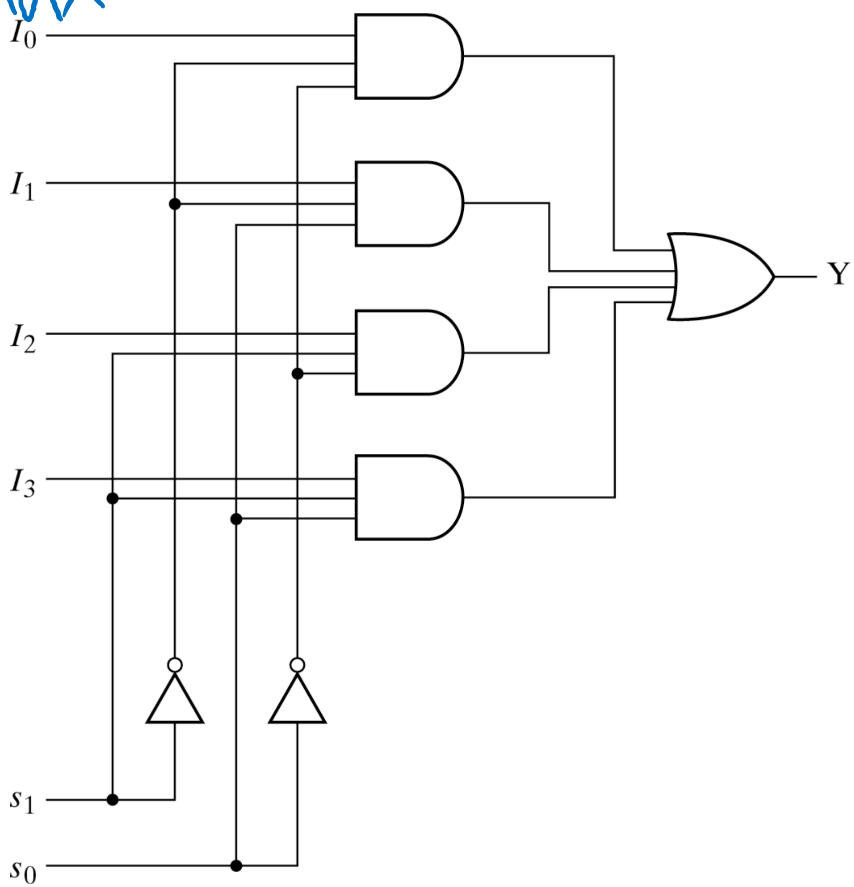




Boolean Function Implementation (1/4)

- MUX: decoder + OR gate
- 2^{n-1}-to-1 MUX can implement any Boolean function of n input variable



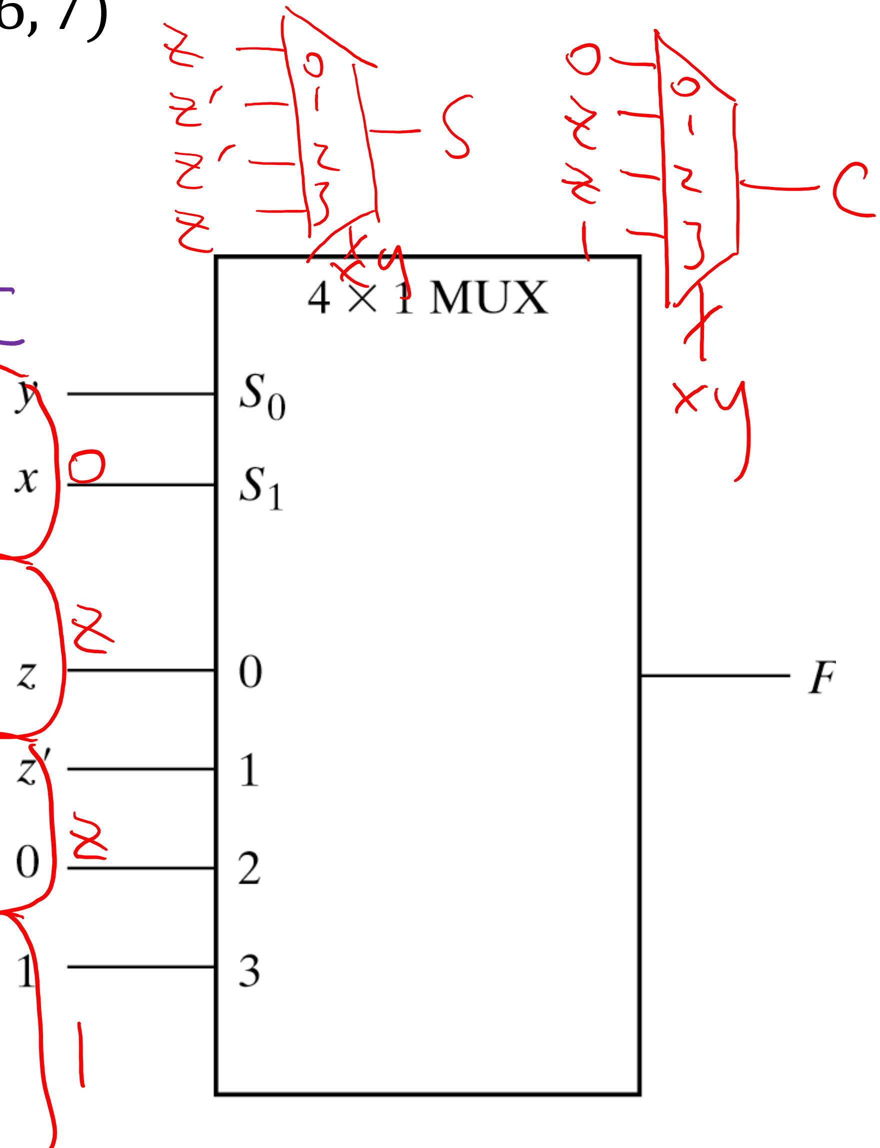


Boolean Function Implementation (2/4)

- Example: $F(x, y, z) = \sum(1, 2, 6, 7)$

$S = \Sigma(1,2,4,7)$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



Boolean Function Implementation (3/4)

2^{n-1}-to-1

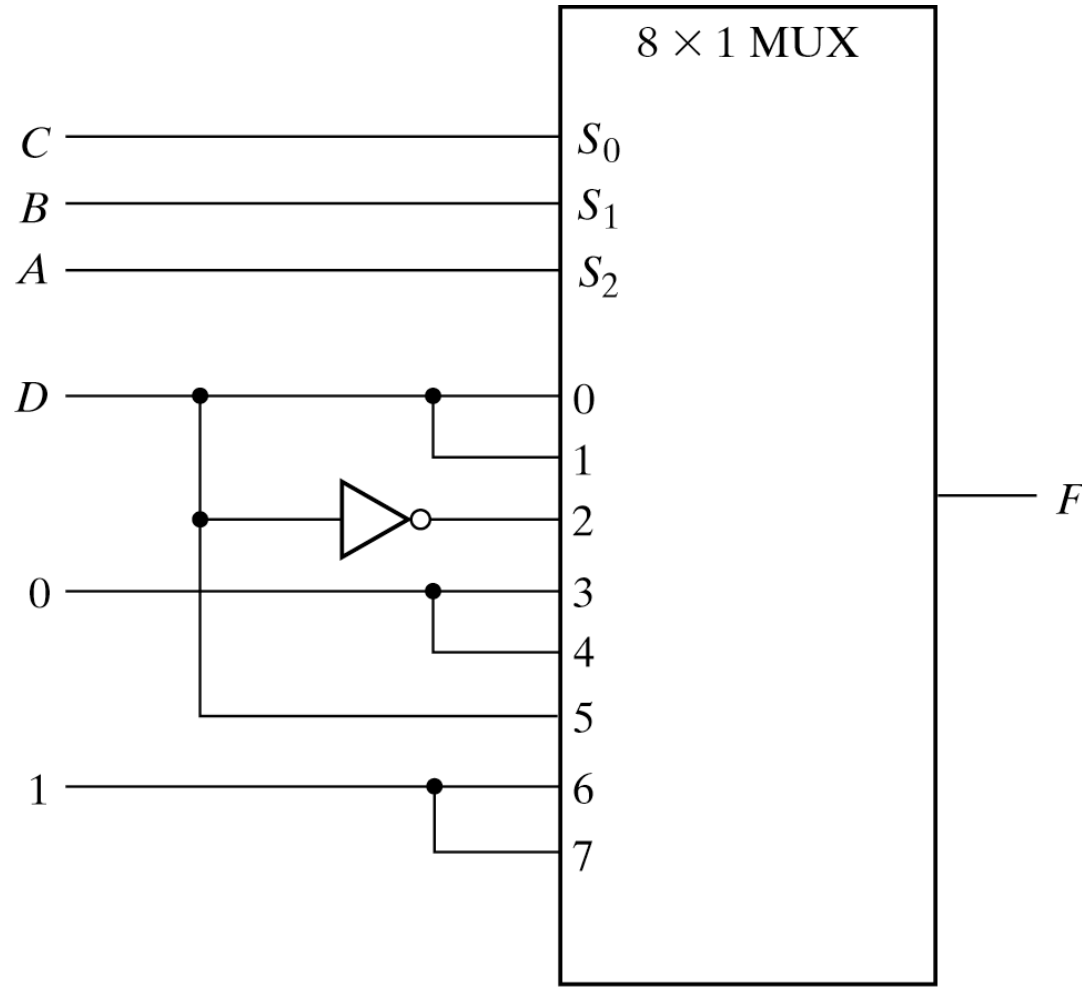
- For an *n*-variable function
- Assign an ordering sequence of the $n - 1$ input variables to the selection input of MUX
- The last (rightmost) variable will be used for the input lines
- Construct the truth table
- Consider a pair of consecutive minterms starting from m_0
- Determine the input lines according to the last variable and output signals in the truth table

Boolean Function Implementation (4/4)

- Example: $F(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$

select

A	B	C	D	F	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = D'$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	

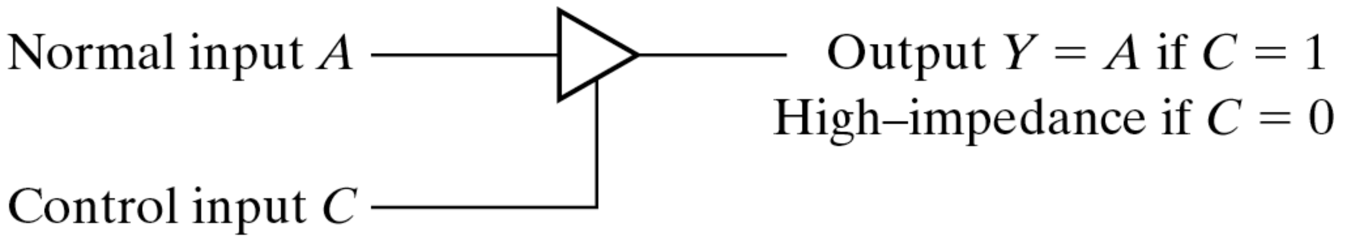


Three-State Gates

(Tri-state)

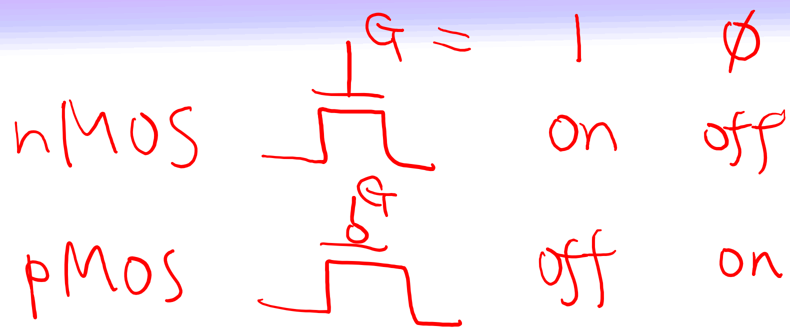
Three-State Gates (1/2)

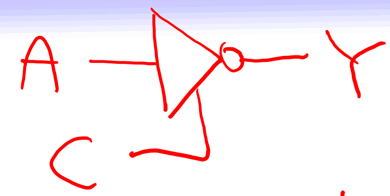
- A multiplexer can be constructed with three-state gates
- Output states: 0, 1, and Z (high-impedance, or open circuits)

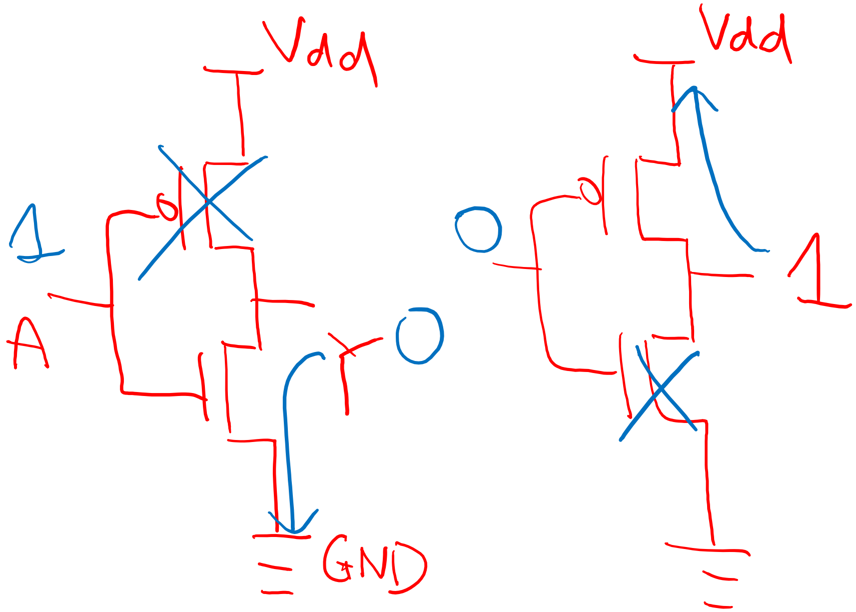


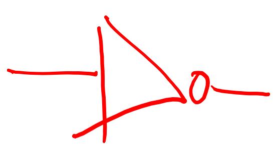
C	Y
0	Z
1	A

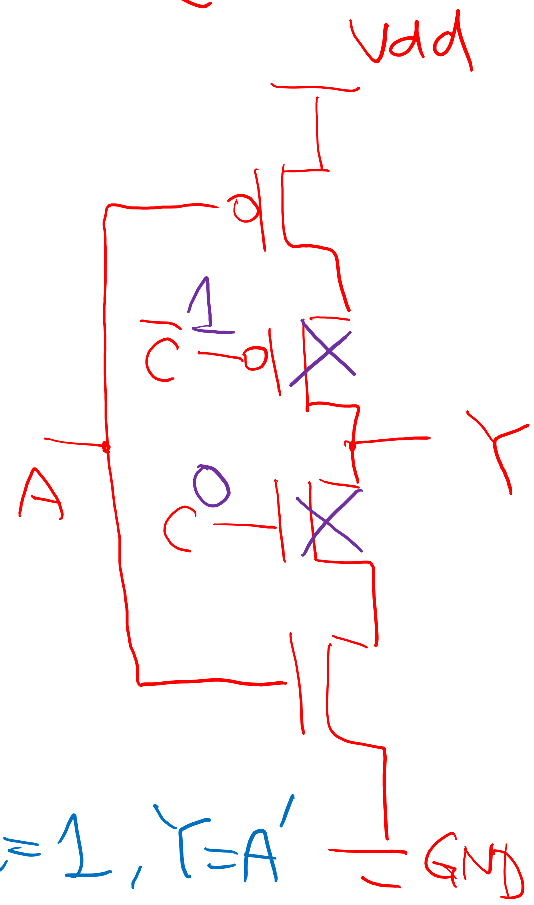
- Three-state gates can be used to build up a *bus*
  - A communication channel among different modules in a digital system











$C = 1,\ Y = A'$

$C = 0,\ Y = \text{hi-z}$

high-z

high-impedance

Three-State Gates (2/2)

- Examples: multiplexers with three-state gates