Design Assignment 3: AntVengers!

Due on June 24 23:00

Objective

In this assignment, you are going to design a simple finite-state machine to explore and escape the maze with limited inputs from outside environment. In addition, you can also learn some Verilog coding and shell script tricks which may help you not only for HDL coding but also for software programming, including

1. The way to import data from an ASCII file to a memory in Verilog;
2. The ability to pass a string or number to the Verilog simulator at runtime;
3. The style of using a header file with `` `define `` in Verilog;
4. The usage of the compiler directives, `` `ifdef/`endif `` in Verilog;
5. The usage of the task in Verilog;
6. The usage of simple shell scripts to help simplify the simulation.

Problem Description and Design Specification

You woke up and found yourself becoming an Ant-Person, being trapped in a dark Maze Universe!! You also lost the eyesight! But instead, you got two antennas, left and right. In the first place, you know that you need to escape the Maze Universe (and save the world, of course. With Great Power Comes Great Responsibility, you know)!

Using the two antennae as inputs you can sense the Maze walls. Design the finite-state machine to explore and escape the maze universe.

1. Please read **`da3-2_AntVengers.pdf`** for the detailed problem description.
   a. Read the **`da3-3_00_README.txt`** for the description about each source file and the simulation details too.
   b. Look into the source files. Remember that the source code is the best documentation to a programmer.
   c. You must design proper finite-state machine to solve the problem.
2. Your mission is to replace the `ant_suit.v`. Note that the sample module is just a Zombie example which walks in a fixed order of moves.
3. Test your Ant-Person Suit with the different mazes. Design your own ones (at least two mazes) with the size bigger than 15x15.
4. We also list two challenges for you:
   a. Challenge of narrow corridors and/or narrow corners
   b. Challenge of wall islands

5. You must discuss the possible solution to either one of the challenges (either Challenge 1 or Challenge 2, or both) in details.
6. To gain extra points, you can propose possible solutions to both the challenges, and provide the solutions to either one challenge or both, in Verilog. You have to provide your own maze(s).
7. Write a report to summarize all the discussions.
   NOTE:
   No score if you simply cut-and-paste waveforms or draw some diagram without proper discussion.

Note

1. Raise the discussion for any questions when in doubt.
2. The **`file.tgz`** can be decompressed and extracted by using the following command on the workstation:
   `$ tar zxvf file.tgz`
3. There will be hidden testbench to verify your designs. Be sure to follow the IO specification and naming convention of files.
4. You should prepare a document, **`da3_README.txt`**, to describe how to perform all the simulations. So that we can repeat your simulation(s) by the copy-n-paste of the instructions inside.
5. You should follow all the instructions to submit the source code and electrical report.
6. Also read the additional notes below:

附註：

1. 請在截止時間內 (**23:00 前**) 上傳，切勿逾期。
2. 上傳檔案請勿壓縮：
   a. ant_suit (your Verilog design)
   b. ant_suit_c1.v, ant_suit_c2.v, ant_suit_cb.v (for Challenge 1, Challenge 2, or both, respectively, if you solve the challenges)
   c. ant.sh, ant_c1.sh, ant_c2.sh, ant_cb.sh (if you have your own shell scripts)
   d. header_maze 寬 x 高.v, maze 寬 x 高.txt (your own testbench, 迷宮可繳交兩個以上,請同學自行編號並說明)
   e. 其他任何自行修改的檔案，有修改請務必上傳，並詳細說明。
   f. Document: da3_README.txt
   g. da3_學號.pdf (your PDF report)
3. Verilog design/testbench 請依照 template 格式。

4. Report 請套用 template 格式撰寫，繳交 PDF 格式，內容至少 300 字以上。請勿單單複製貼上 Source Code (Source Code 不算字數).
5. **請務必自己完成作業，有問題及早詢問助教及老師。**