EECS1010 Design Assignment 02

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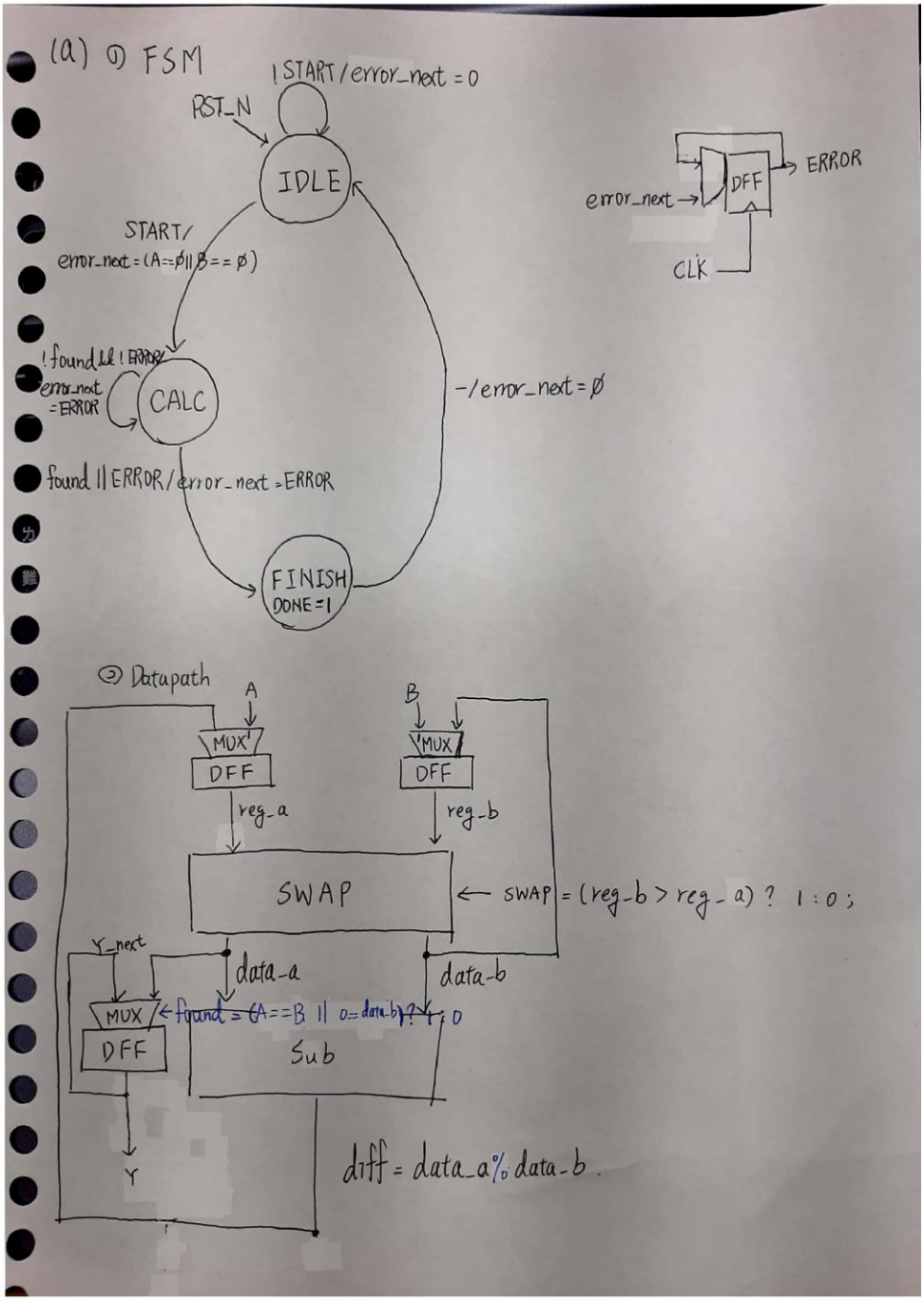
1. Design Concept and Description

(a) FSM & Block Diagram

輾轉相減法——與講義相同，分為 IDLE、CALC、FINISH 三種 state，透過 DFF 連續傳遞 ERROR 的值。

(b) FSM & Block Diagram

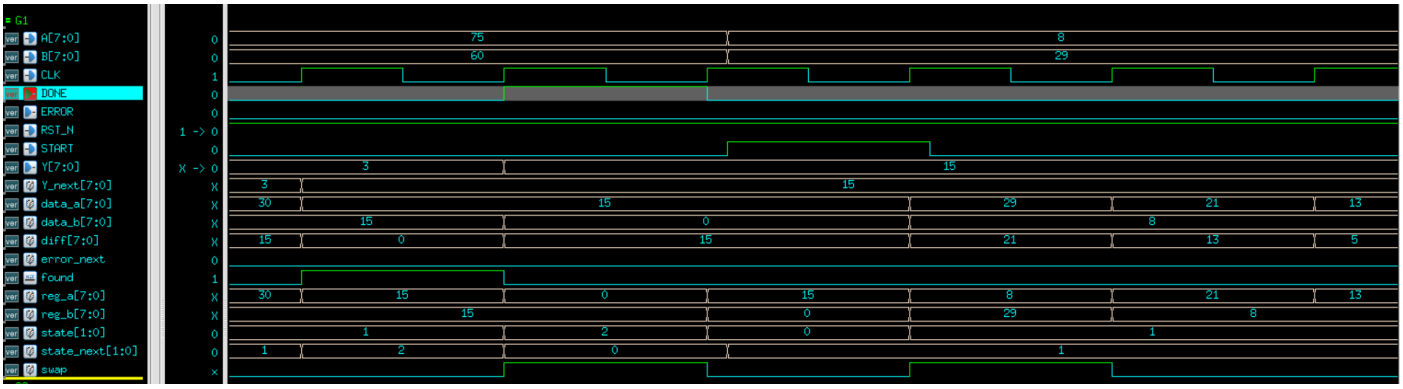
輾轉相除法，當 A 與 B 相等或 data_b==0 時，found：0→ 1。



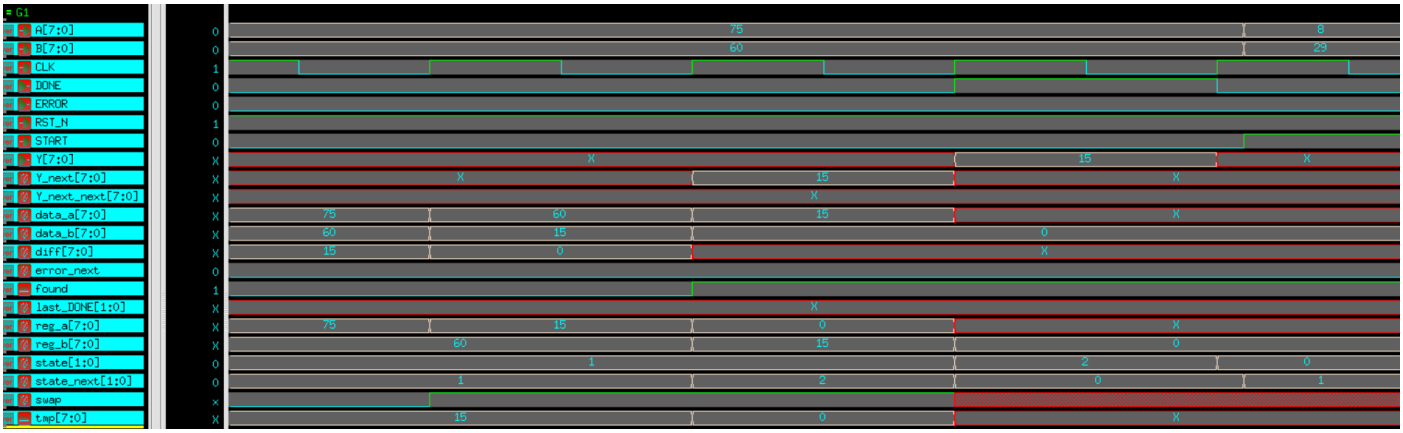
2. Simulation and Discussion

Simulation:

輾轉相減法



輾轉相除法



輾轉相減法：

```
****************************************
Report : area
Design : GCD
Version: K-2015.06-SP1
Date   : Thu Jun 11 21:00:44 2020
****************************************

Library(s) Used:

    slow (File: /theda21_2/CBDK_IC_Contest/cur/SynopsysDC/db/slow.db)

Number of ports:                           53
Number of nets:                           215
Number of cells:                          143
Number of combinational cells:            115
Number of sequential cells:                27
Number of macros/black boxes:               0
Number of buf/inv:                         12
Number of references:                      26

Combinational area:               1108.402204
Buf/Inv area:                       47.527199
Noncombinational area:             952.241390
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2060.643594
Total area:                 undefined
dc_shell> uplevel #0 { report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by group }
```

輾轉相除法：

```
****************************************
Report : area
Design : GCD
Version: K-2015.06-SP1
Date   : Thu Jun 11 21:03:18 2020
****************************************

Library(s) Used:

    slow (File: /theda21_2/CBDK_IC_Contest/cur/SynopsysDC/db/slow.db)

Number of ports:                           96
Number of nets:                           413
Number of cells:                          290
Number of combinational cells:            260
Number of sequential cells:                27
Number of macros/black boxes:               0
Number of buf/inv:                         30
Number of references:                      31

Combinational area:               2610.601206
Buf/Inv area:                      108.633598
Noncombinational area:             952.241390
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  3562.842597
Total area:                 undefined
dc_shell> uplevel #0 { report_timing -path full -delay max -nworst 1 -max_paths 1 -significant_digits 2 -sort_by group }
****************************************
```

從這兩張圖的 combinational area 可以發現，使用輾轉相除法較輾轉相減法大了許多。

輾轉相減法：

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : GCD
Version: K-2015.06-SP1
Date   : Thu Jun 11 21:01:19 2020
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: reg_a_reg[1]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: reg_a_reg[7]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  reg_a_reg[1]/CK (DFFSRX1)                0.00       0.00 r
  reg_a_reg[1]/Q (DFFSRX1)                 0.51       0.51 f
  U271/Y (OR2X1)                           0.24       0.75 f
  U270/Y (AOI222XL)                        0.31       1.06 r
  U269/Y (AOI221XL)                        0.10       1.16 f
  U264/Y (AOI221XL)                        0.20       1.36 r
  U263/Y (AOI221XL)                        0.10       1.46 f
  U261/Y (OAI22XL)                         0.15       1.61 r
  U260/Y (OAI21XL)                         0.14       1.75 f
  U259/Y (AND2X2)                          0.17       1.92 f
  U258/Y (OAI22XL)                         0.24       2.16 r
  U257/Y (CLKBUFX3)                        0.25       2.40 r
  U217/Y (CLKINVX1)                        0.24       2.64 f
  U224/Y (OAI22XL)                         0.30       2.94 r
  sub_148/B[1] (GCD_DW01_sub_0)            0.00       2.94 r
  sub_148/U3/Y (CLKINVX1)                  0.10       3.03 f
  sub_148/U2_1/CO (ADDFXL)                 0.63       3.66 f
  sub_148/B[1] (GCD_DW01_sub_0)            0.00       2.94 r
  sub_148/U3/Y (CLKINVX1)                  0.10       3.03 f
  sub_148/U2_1/CO (ADDFXL)                 0.63       3.66 f
  sub_148/U2_2/CO (ADDFXL)                 0.38       4.03 f
  sub_148/U2_3/CO (ADDFXL)                 0.38       4.41 f
  sub_148/U2_4/CO (ADDFXL)                 0.38       4.79 f
  sub_148/U2_5/CO (ADDFXL)                 0.38       5.16 f
  sub_148/U2_6/CO (ADDFXL)                 0.36       5.52 f
  sub_148/U1/Y (XNOR3X1)                   0.23       5.75 f
  sub_148/DIFF[7] (GCD_DW01_sub_0)         0.00       5.75 f
  U266/Y (AO22X1)                          0.28       6.04 f
  reg_a_reg[7]/D (DFFSRX1)                 0.00       6.04 f
  data arrival time                                   6.04

  clock CLK (rise edge)                   40.00      40.00
  clock network delay (ideal)              0.00      40.00
  reg_a_reg[7]/CK (DFFSRX1)                0.00      40.00 r
  library setup time                      -0.13      39.87
  data required time                                 39.87
  -----------------------------------------------------------
  data required time                                 39.87
  data arrival time                                  -6.04
  -----------------------------------------------------------
  slack (MET)                                        33.83
```

輾轉相除法：

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
         -sort_by group
Design : GCD
Version: K-2015.06-SP1
Date   : Thu Jun 11 21:03:41 2020
****************************************

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: reg_a_reg[7]
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: reg_a_reg[0]
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock CLK (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  reg_a_reg[7]/CK (DFFSRX1)                               0.00       0.00 r
  reg_a_reg[7]/Q (DFFSRX1)                                0.54       0.54 f
  U204/Y (AND2X1)                                         0.20       0.74 f
  U206/Y (OAI32X1)                                        0.22       0.95 r
  U150/Y (CLKINVX1)                                       0.08       1.04 f
  U208/Y (AO22X1)                                         0.33       1.36 f
  U149/Y (OAI31XL)                                        0.10       1.47 r
  U148/Y (CLKBUFX3)                                       0.26       1.72 r
  U124/Y (CLKINVX1)                                       0.27       1.99 f
  U110/Y (OAI22XL)                                        0.37       2.36 r
  rem_157/b[7] (GCD_DW_div_uns_0)                         0.00       2.36 r
  rem_157/U14/Y (CLKINVX1)                                0.14       2.50 f
  rem_157/U103/Y (NAND2X1)                                0.13       2.63 r
  rem_157/U2/Y (CLKINVX1)                                 0.07       2.70 f
  rem_157/U100/Y (NAND3X1)                                0.12       2.82 r
```

```
  rem_157/U103/Y (NAND2X1)                                0.13       2.63 r
  rem_157/U2/Y (CLKINVX1)                                 0.07       2.70 f
  rem_157/U100/Y (NAND3X1)                                0.12       2.82 r
  rem_157/U6/Y (NAND2BX1)                                 0.19       3.01 r
  rem_157/U95/Y (AOI211X1)                                0.10       3.11 f
  rem_157/u_div/u_mx_PartRem_0_7_0/Y (CLKMX2X2)           0.27       3.39 r
  rem_157/U75/Y (NOR2X1)                                  0.06       3.44 f
  rem_157/U77/Y (OAI21XL)                                 0.16       3.61 r
  rem_157/U97/Y (AND3X1)                                  0.28       3.88 r
  rem_157/u_div/u_mx_PartRem_0_6_0/Y (CLKMX2X2)           0.25       4.13 r
  rem_157/U65/Y (NOR2X1)                                  0.05       4.18 f
  rem_157/U67/Y (OA21XL)                                  0.30       4.48 f
  rem_157/U70/Y (AOI21X1)                                 0.11       4.59 r
  rem_157/U98/Y (NOR2BX1)                                 0.28       4.88 r
  rem_157/u_div/u_mx_PartRem_0_5_0/Y (CLKMX2X2)           0.29       5.17 r
  rem_157/U54/Y (NOR2X1)                                  0.06       5.23 f
  rem_157/U56/Y (OAI21XL)                                 0.28       5.51 r
  rem_157/U57/Y (OA22X1)                                  0.24       5.75 r
  rem_157/U99/Y (NOR2BX1)                                 0.33       6.08 r
  rem_157/u_div/u_mx_PartRem_0_4_1/Y (CLKMX2X2)           0.32       6.40 r
  rem_157/U28/Y (NAND2X1)                                 0.08       6.48 f
  rem_157/U30/Y (OAI21XL)                                 0.26       6.74 r
  rem_157/U1/Y (CLKINVX1)                                 0.08       6.81 f
  rem_157/U35/Y (OAI21XL)                                 0.09       6.90 r
  rem_157/U36/Y (OAI21XL)                                 0.13       7.04 f
  rem_157/U38/Y (OAI21XL)                                 0.19       7.23 r
  rem_157/U101/Y (AND3X1)                                 0.39       7.63 r
  rem_157/u_div/u_mx_PartRem_0_3_0/Y (CLKMX2X2)           0.29       7.92 r
  rem_157/u_div/u_add_PartRem_1_2/U6/CO (ADDFXL)          0.58       8.49 r
  rem_157/u_div/u_add_PartRem_1_2/U5/CO (ADDFXL)          0.31       8.81 r
  rem_157/u_div/u_add_PartRem_1_2/U4/CO (ADDFXL)          0.31       9.12 r
  rem_157/u_div/u_add_PartRem_1_2/U3/CO (ADDFXL)          0.31       9.44 r
  rem_157/u_div/u_add_PartRem_1_2/U2/CO (ADDFXL)          0.28       9.71 r
  rem_157/U102/Y (NOR2BX1)                                0.46      10.18 r
  rem_157/u_div/u_mx_PartRem_0_2_0/Y (CLKMX2X2)           0.35      10.52 r
  rem_157/u_div/u_add_PartRem_1_1/A[0] (GCD_DW01_add_1)
                                                          0.00      10.52 r
  rem_157/u_div/u_add_PartRem_1_1/U7/CO (ADDFXL)          0.58      11.10 r
  rem_157/u_div/u_add_PartRem_1_1/U6/CO (ADDFXL)          0.31      11.41 r
  rem_157/u_div/u_add_PartRem_1_1/U5/CO (ADDFXL)          0.31      11.73 r
  rem_157/u_div/u_add_PartRem_1_1/U4/CO (ADDFXL)          0.31      12.04 r
  rem_157/u_div/u_add_PartRem_1_1/U3/CO (ADDFXL)          0.31      12.36 r
```

```
rem_157/u_div/u_add_PartRem_1_1/U4/CO (ADDFXL)          0.31      12.04 r
rem_157/u_div/u_add_PartRem_1_1/U3/CO (ADDFXL)          0.31      12.36 r
rem_157/u_div/u_add_PartRem_1_1/U2/CO (ADDFXL)          0.28      12.63 r
rem_157/u_div/u_add_PartRem_1_1/CO (GCD_DW01_add_1)     0.00      12.63 r
rem_157/U104/Y (NOR2BX1)                                0.49      13.13 r
rem_157/u_div/u_mx_PartRem_0_1_0/Y (MX2XL)              0.39      13.52 f
rem_157/u_div/u_add_PartRem_1_0/A[0] (GCD_DW01_add_2)
                                                        0.00      13.52 f
rem_157/u_div/u_add_PartRem_1_0/U8/CO (ADDFXL)          0.56      14.08 f
rem_157/u_div/u_add_PartRem_1_0/U7/CO (ADDFXL)          0.38      14.45 f
rem_157/u_div/u_add_PartRem_1_0/U6/CO (ADDFXL)          0.38      14.83 f
rem_157/u_div/u_add_PartRem_1_0/U5/CO (ADDFXL)          0.38      15.21 f
rem_157/u_div/u_add_PartRem_1_0/U4/CO (ADDFXL)          0.38      15.58 f
rem_157/u_div/u_add_PartRem_1_0/U3/CO (ADDFXL)          0.38      15.96 f
rem_157/u_div/u_add_PartRem_1_0/U2/CO (ADDFXL)          0.62      16.58 f
rem_157/u_div/u_add_PartRem_1_0/CO (GCD_DW01_add_2)     0.00      16.58 f
rem_157/u_div/u_mx_PartRem_0_0_0/Y (MX2XL)              0.34      16.91 f
rem_157/remainder[0] (GCD_DW_div_uns_0)                 0.00      16.91 f
U158/Y (AO22X1)                                         0.28      17.19 f
reg_a_reg[0]/D (DFFSRX1)                                0.00      17.19 f
data arrival time                                                 17.19

clock CLK (rise edge)                                  40.00      40.00
clock network delay (ideal)                             0.00      40.00
reg_a_reg[0]/CK (DFFSRX1)                               0.00      40.00 r
library setup time                                     -0.13      39.87
data required time                                                39.87
-----------------------------------------------------------------------
data required time                                                39.87
data arrival time                                                -17.19
-----------------------------------------------------------------------
slack (MET)                                                       22.67
```

從 timing report 中可以看出，後者較前者省時。

總合以上兩種報告，若想減少成本可以使用輾轉相減法；想增加運算效率可以使用輾轉相除法。

在寫這份作業時，可謂困難重重：

Q1：不太懂改檔名與加入旁邊的目錄，導致 dc_shell 無法 command

A1：改檔名及重新執行 dc_shell

Q2：寫 case 時，漏了 default，導致根本讀不到訊號

A2：加入 default

Q3：每個 case 中賦予的值沒有相同，而出現 latch

A3：補上缺少的值

Q4：在同一個 block 使用兩次 if…else

A4：分成兩個 block 寫

Q5：不清楚使用 blocking & non-blocking 的時機，陷入無窮迴圈

A5：combinational→blocking；sequentail→non-blocking

3. Summary

感謝教授及助教的耐心指教。

// A brief summary, including suggestions for the lecturer (or for this course).

// 結論，或是想對老師或助教說的話、對課程的建議、提供笑話、告白(?)