A Low-Power Low Dropout Regulator for an Energy Management Unit

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Topics Covered

- Energy Management Unit
- Low Dropout Regulator Basics
- Specifications of the LDO Regulator
- Stability and Frequency Compensation
- LDO Regulator Components Design
- LDO Regulator Simulation Results
- Final Results- Summary
- Possible Improvements

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Energy Management Unit

- Supplied through inductive energy transmission.
- Powered by a bank of 4 parallel supercapacitors.
- Lower discharge voltage of the capacitors is achieved by changing the connection form parallel to series, thus increasing the available energy.
- Two low dropout regulators (LDO) : the Main LDO and the low-power LDO.
- Main LDO regulator : Powers the implant.
- Low- power LDO regulator : Powers different circuitry of the energy management unit.

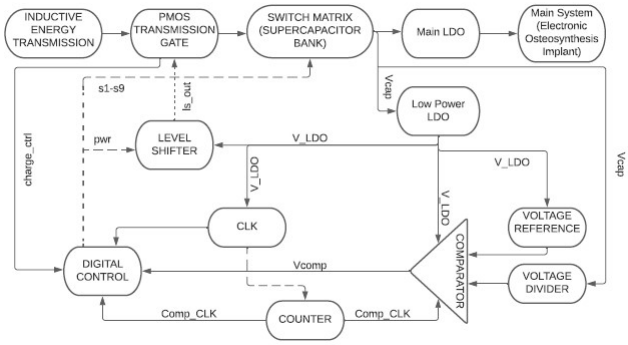


Figure 1: Energy Management Unit of the electronic osteosynthesis implant.

Low Dropout Regulator

- Regulation is maintained for a varying supply voltage.
- Main components:
  - Pass element
  - feedback network
  - reference voltage
  - error amplifier
  - frequency compensation network.
- Main Operational regions :
  - Regulation region
  - dropout region
  - off-region.
- Low quiescent current.

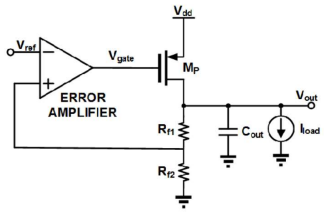


Figure 2 : A basic LDO Regulator [17]

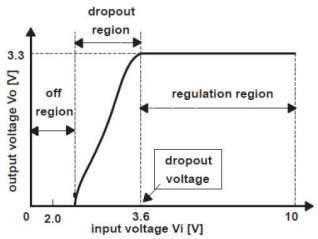
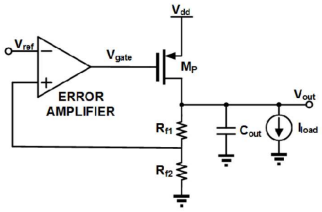


Figure 3: LDO Regulator operating regions [11]

Low Dropout Regulator

- Pass element:
  - Used for transferring large currents from the input to the load.
  - Driven by the error amplifier in a feedback loop.
  - Generally a MOSFET is used as a pass device.
  - Additional step-up voltage converter required for NMOS pass device.
  - PMOS pass transistor configuration doesn't require extra circuit to bias the error amplifier, has a low dropout voltage, typically used in LDO regulators.

- Feedback network:
  - Forms a control loop between the error amplifier and the pass transistor.
  - Scales down the LDO regulator output voltage to compare against the error amplifier reference voltage.
  - A resistive voltage divider is typically used as the feedback network.
  - A series of diode connected PMOS transistors could be used as the voltage divider to reduce area consumption.



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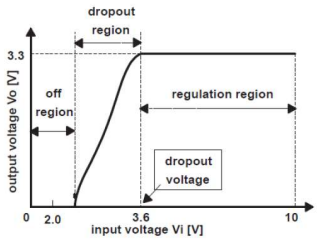

Figure 3: LDO Regulator operating regions [11]

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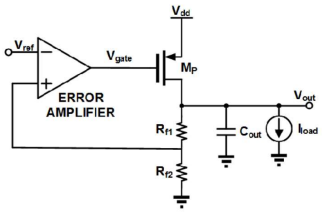
Low Dropout Regulator

- Error Amplifier:
  - Consumes the most current of the LDO regulator, a simple architecture is desirable.
  - Typically, a two stage operational amplifier is used for achieving a higher gain.
  - Major requirements:
    - High open-loop gain
    - Low quiescent current
    - Operation under low V_{in} conditions.
    - High bandwidth
    - High power supply rejection
    - High output voltage swing

- Voltage reference:
  - Constant dc 1.2V supply. (Designing the voltage reference wasn't a part of the project work)



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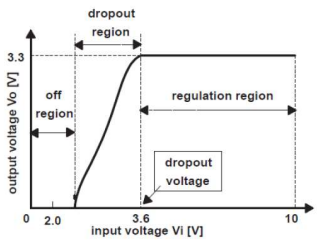

Figure 3: LDO Regulator operating regions [11]

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Specifications of the desired LDO regulator

Parameters	Value
$V_{in,min}$	2V
$V_{in,max}$	5V
V_{out}	1.8V
V_{DO}	200mV
$I_{load\ (active)}$	25µA
$I_{load\ (inactive)}$	6.7µA

Table 1: LDO regulator specifications obtained from the energy management unit.

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Frequency Compensation Approach

- Proper compensation approach is necessary to achieve stability.
- Two types of compensation approach:
  - External compensation:
    - Uses a high valued output capacitor.
    - LDO regulator output pole is the dominant pole.
    - The load capacitor creates an equivalent series resistor (ESR) whose value changes with frequency.
    - The ESR could lead to a modified AC and transient response.
    - Implementation into very small or lightweight equipment isn't possible.
  - Internal compensation:
    - Miller compensation approach.
    - Can be fully integrated onto system-on-chip (SoC).
    - Error amplifier output pole is the dominant pole.

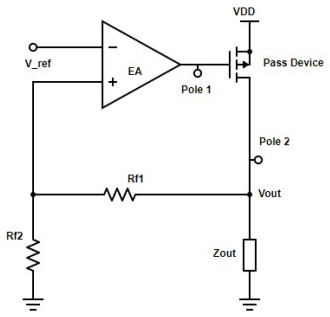

Figure 4: LDO regulator with major pole locations [4]

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Frequency Compensation Approach

- Internal compensation:
  - Known as capacitor-less LDOs.
- Approximate pole locations:
  - $f_{p,out} = \frac{1}{2\pi r_{eq} C_{Load}}$
  - $f_{p,EA} = \frac{1}{2\pi r_{out,EA} C_{PT}}$
  - r_{eq}= equivalent resistance at the output node of the LDO regulator
  - $r_{out,EA}$= equivalent resistance at the output node of the error amplifier
  - C_{PT} = total equivalent capacitor at the pass-transistor gate
  - C_{Load} = load capacitance
- $f_{p,out}$ and $f_{p,EA}$ both at low frequencies for an uncompensated LDO regulator.
- Internal compensation places $f_{p,out}$ far away from $f_{p,EA}$; ensuring the stability of the LDO regulator.

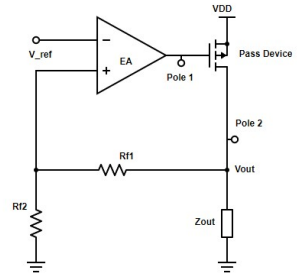

Figure 4: LDO regulator with major pole locations [4]

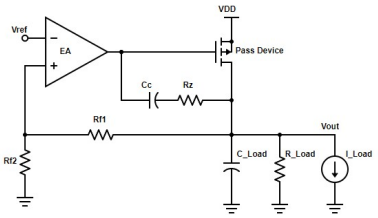

Figure 5: Internally compensated LDO regulator [4].

Frequency Compensation Approach

- Internal compensation:
  - $P_d = -\frac{1}{r_{out,EA}(C_C+C_{PT})+(C_C+C_{Load})r_{eq}+gm_{PT}r_{out,EA}r_{eq}C_C}$
  - $P_{nd} = -\frac{gm_{PT}\,C_C}{(C_C+C_{Load})C_{PT}+C_C\,C_{Load}}$
  - $z = \frac{1}{\left(\frac{1}{gm_{PT}} - R_Z\right)C_C}$

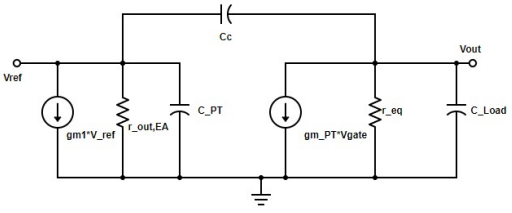

Figure 6: Small-signal equivalent circuit of the open-loop miller compensated LDO Regulator [4].

LDO Regulator Components Design

Parameter	Threshold Voltage Low(V)	Threshold Voltage Typical(V)	Threshold Voltage High(V)	μC_{ox} ($\mu \frac{A}{V^2}$)
PMA	-1.05	-1.2	-1.35	12.85
NMA	1.13	1.23	1.33	46.16
PE	-0.67	-0.7	-0.73	28.69

Table 2: Process parameters for the transistors

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LDO Regulator Components Design

- Pass Transistor:
  - 6V PMA transistor.
  - $\left(\frac{W}{L}\right)$ calculation:
    - $V_{in,min}$ = 2V, $V_{in,max}$= 5V, I_{load} = 25µA, V_{out} = 1.8V
    - $V_{SG} = V_s - V_G$ = 2V-300mV =1.7V
    - $I_D = \mu_p C_{ox,p} \frac{W}{L} \left[\left(V_{SG} - V_{Th,p} \right) - \frac{V_{SD}}{2} \right] V_{SD}$
    - $\left(\frac{W}{L}\right)_{Pass} = \frac{I_{load}}{\mu_p C_{ox,p} \left[\left(V_{SG} - V_{Th,p} \right) - \frac{V_{SD}}{2} \right] V_{SD}} \approx 24$
    - L = 2.5µm, W = 68µm

Parameter	Value
Minimum input voltage $V_{in,min}$	2V
Load current I_{load}	25µA
Channel Width, W	68µm
Channel Length, L	2.5µm

Table 3: Parameters for the pass device

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LDO Regulator Components Design

- Feedback Network:
  - V_{out} =1.8V; V_{ref} =1.2V
  - $\frac{V_{out}}{V_{ref}} = \frac{R_{f1}+R_{f2}}{R_{f2}}$; $\frac{V_{out}}{V_{ref}} = 1 + \frac{R_{f1}}{R_{f2}}$; $\frac{R_{f1}}{R_{f2}} = \frac{1.8}{1.2} - 1$; $\frac{R_{f2}}{R_{f1}} = 2:1$
  - $I_{req} = \frac{V_{out}}{R_{f1}+R_{f2}}$
  - I_{req} = 0.05 % of I_{load} (25µA) =13nA
  - $R_{f2} = \frac{V_{ref}}{I_{req}} = \frac{1.2V}{13nA} = 92.3M\Omega$
  - $R_{f1} = \frac{V_{out}}{I_{req}} - R_{f2} = \frac{1.8V}{13nA} - 92.3M\Omega = 46.15M\Omega$

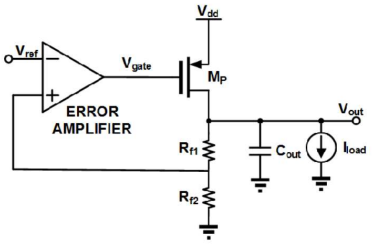

Figure 7: Basic LDO Regulator [17]

LDO Regulator Components Design

- Feedback Network:
  - 1.98V PE transistor.
  - $\left(\frac{W}{L}\right)$ calculation:
    - I_{req} = 13nA
    - n (sub-threshold swing coefficient) = 1.5
    - $V_{SD} = V_{SG}$ =600mV
    - V_t = Thermal voltage =26mV
    - $\left(\frac{W}{L}\right)_{feedback} = \frac{I_{req}}{\mu_p C_{ox,p}(n-1)V_t^2 e^{-V_{Th}/nV_t} e^{-V_{SG}/nV_t}(1-e^{-V_{SD}/V_t})} \approx 8.11$
    - From simulation, $\left(\frac{W}{L}\right)_{feedback}$ =0.9
    - W= 2µm , L = 2.22µm

Parameter	Value
Output voltage V_{out}	1.8V
Reference Voltage V_{ref}	1.2V
Bias current I_{req}	13nA
Channel Width, W	2µm
Channel Length, L	2.22µm

Table 4: Parameters for the feedback network

LDO Regulator Components Design

Parameter	Value
Open-loop DC gain	$60dB$
Phase margin	90^0
Settling time	$30Hz \times 10 = 3000Hz$ $= 333.33\ \mu s$
Unity gain frequency	$1/t_{settling} = 3kHz$
Slew rate	$0.015V/\mu s$
Load capacitance	$170.79fF$

Table 5: Error amplifier assumed specifications

Parameter	Transistor Used	Width(W) (µm)	Length(L) (µm)	Operating region
$M_{1,2}$	6V NMA	200	1	Sub-threshold
$M_{3,4}$	6V PMA	2.5	2.5	Saturation
M_5	6V NMA	8	1	Saturation
M_6	6V PMA	2.5	1	Saturation
M_7	6V NMA	8	1	Saturation
M_8	6V NMA	8	1	Saturation

Table 6: Error amplifier transistor sizes and operating regions

Parameter	Value
C_c	20pF
R_z	163.6KΩ

Table 7: Error amplifier frequency compensation parameters

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LDO Regulator Components Design

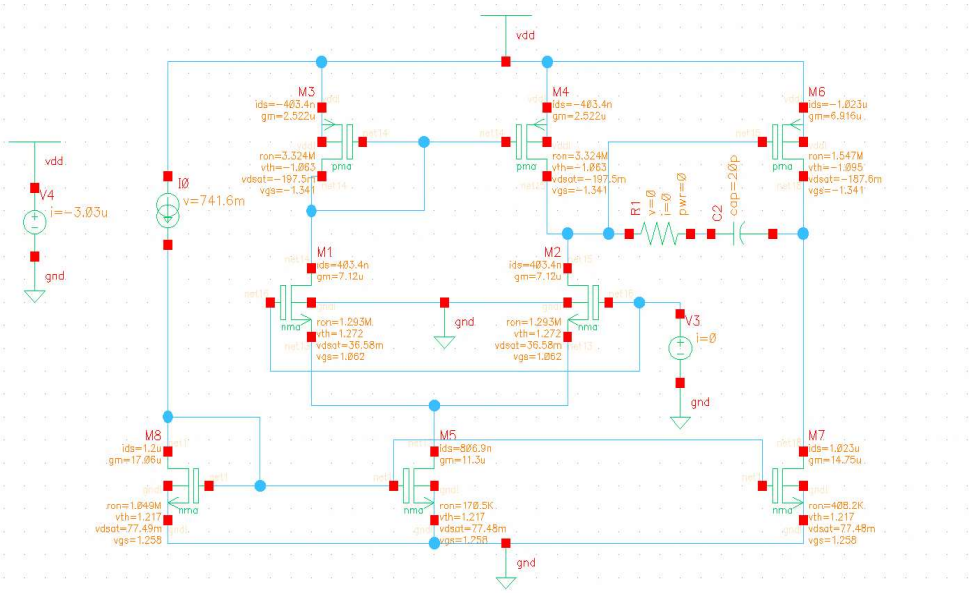

Figure 8: Error amplifier schematic

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LDO Regulator Frequency Compensation Parameters

- $PM = 75^0$; A_v =60dB

$$PM = 180^0 - arctan\left(\frac{\omega_u}{\omega_{p1}}\right) - arctan\left(\frac{\omega_u}{\omega_{p2}}\right) - arctan\left(\frac{\omega_u}{\omega_{z1}}\right)$$

$$arctan\left(\frac{\omega_u}{\omega_{p2}}\right) = 180^0 - 75^0 - arctan(A_v) arctan\left(\frac{\omega_u}{10 \times \omega_u}\right)$$

$$\omega_u = 0.18 \times \omega_{p2}$$

$$\frac{gm_{in}}{C_c} = 0.18 \times \frac{gm_{PT}}{C_L}$$

$$\frac{gm_{in}}{C_c} = 0.18 \times \frac{10 \times gm_{in}}{C_L}$$

$$C_c \geq 0.55 \times C_L$$

Parameter	Value
C_c	100fF
C_L	1pF
R_z	14.15KΩ

Table 8: Frequency compensation parameters

- $z = \frac{1}{\left(\frac{1}{gm_{PT}} R_z\right) C_c}$
- $R_z = \frac{1}{gm_{PT}}$

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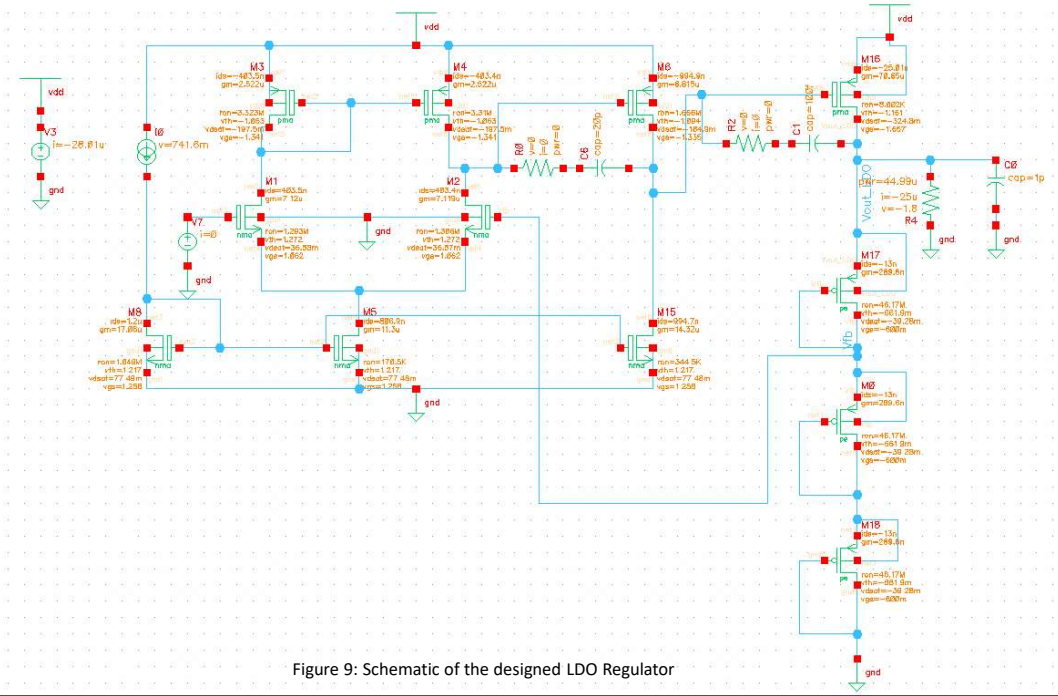

Figure 9: Schematic of the designed LDO Regulator

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DC Analysis

- Regulated 1.8V output voltage for an input voltage of 1.9443 or above.
- $V_{DO} = 145mV$

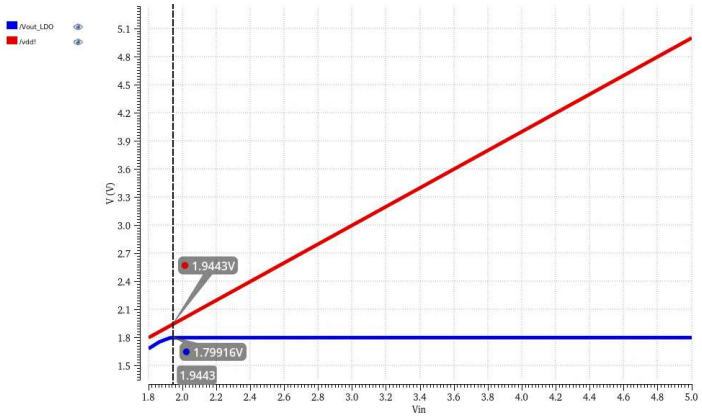
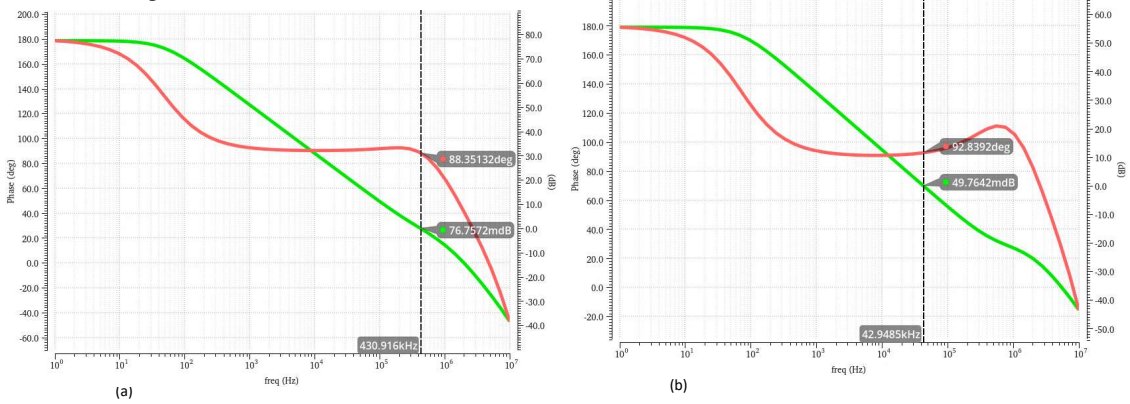


Figure 10: Input-output characteristics

AC Analysis



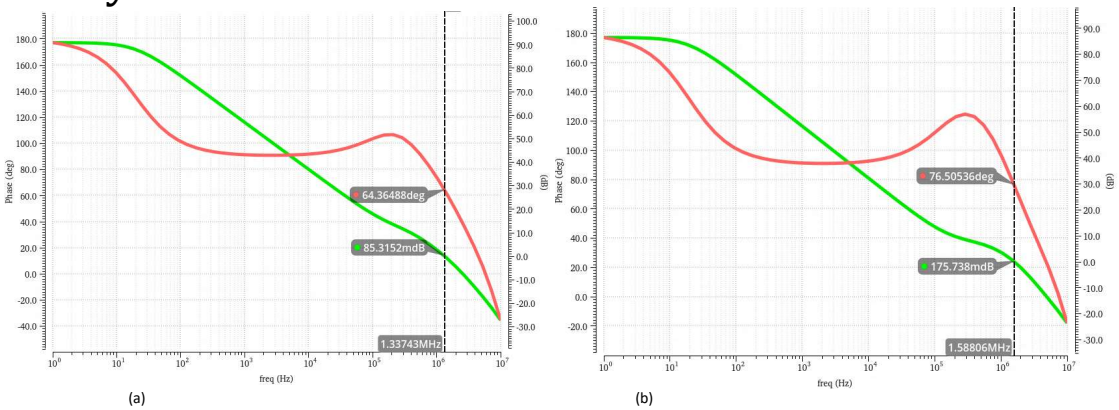
(a) (b)

Figure 11: LDO regulator frequency response at V_{in} =2V for (a) I_{load} = 6.7µA and (b) I_{load} = 25µA

Parameter	I_{load} = 6.7µA	I_{load} = 25µA
DC gain A_{DC} (dB)	77.5	55.5
Bandwidth (Hz)	18	26
Unity Gain Frequency (kHz)	430.916	42.94
Phase Margin (degrees)	88.35	92.8

Table 9: AC simulation parameters for V_{in} = 2V

AC Analysis



(a) (b)

Figure 12: LDO regulator frequency response at V_{in} =5V for (a) I_{load} = 6.7µA and (b) I_{load} = 25µA

Parameter	I_{load} = 6.7µA	I_{load} = 25µA
DC gain A_{DC} (dB)	90.7	86.3
Bandwidth (Hz)	12.8	11.5
Unity Gain Frequency (MHz)	1.34	1.58
Phase Margin (degrees)	64.36	76.5

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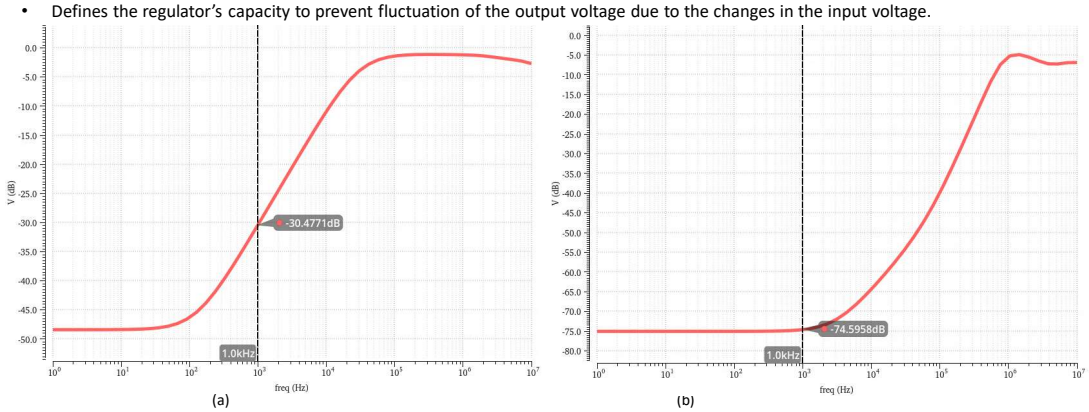
Table 10: AC simulation parameters for V_{in} = 5V

Power Supply Rejection(PSR)

- Defines the regulator's capacity to prevent fluctuation of the output voltage due to the changes in the input voltage.



(a) (b)

Figure 13: LDO regulator PSR at (a) V_{in} =2V (b) V_{in} = 5V at I_{load} = 25µA

Input voltage V_{in}	PSR (dB) (at 1kHz)
2V	-30.4771
5V	-74.5958

Table 11: LDO regulator PSR at (a) V_{in} =2V (b) V_{in} = 5V for I_{load} = 25µA

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Power Supply Rejection(PSR)

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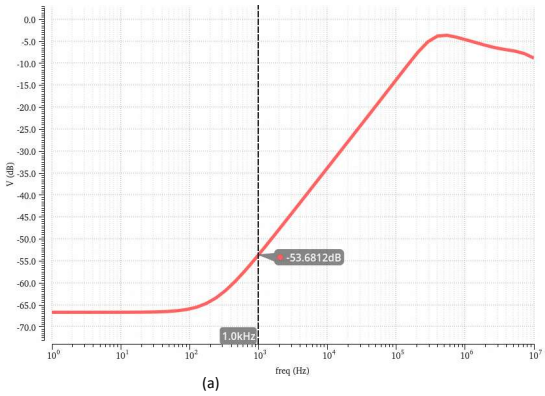
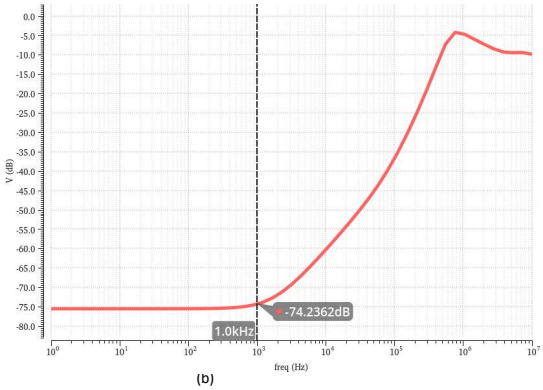


(a)



(b)

Figure 14: LDO regulator PSR at (a) V_{in} =2V (b) V_{in} = 5V for I_{load} = 6.7µA

Input voltage V_{in}	PSR (dB) (at 1kHz)
2V	-53.6812
5V	-74.2362

Table 12: LDO regulator PSR at (a) V_{in} =2V (b) V_{in} = 5V for I_{load} = 6.7µA

Transient Simulation

- Tests the circuit behavior in real-time with varying signals.
- Line transient : Displays the LDO regulator output behavior with a varying supply voltage.
  - Input signal rise time:
    - Analyzed from the simulation results of the capacitor bank from the energy management unit.
  - Input signal fall time :
    - Fastest discharging of the supercapacitors possible when all are in series connection.
    - $C_{eq} = 2.75mF, R_{Load} = 3.6k\Omega, R_{ESR} = 160\Omega$
    - $Time\ constant\ of\ discharging, \tau = C_{eq}(R_{Load} + 4R_{ESR}) = 11.66s$
    - $V(t) = V_{init}\, e^{\frac{-t}{\tau}}$; $V(t) = 2V$, $V_{init} = 5V$
    - $Time\ t\ for\ the\ voltage\ to\ reduce\ from\ 5V\ to\ 2V = 10.68s$
    - $\frac{dV}{dt} = -\frac{V_{init}}{\tau}\, e^{\frac{-t}{\tau}} = -\frac{171.58mV}{s}$, $t_f = \frac{\Delta V}{SR} = 17.48s$
  - LDO regulator Input signal t_{rise} = t_{fall} = 300µs

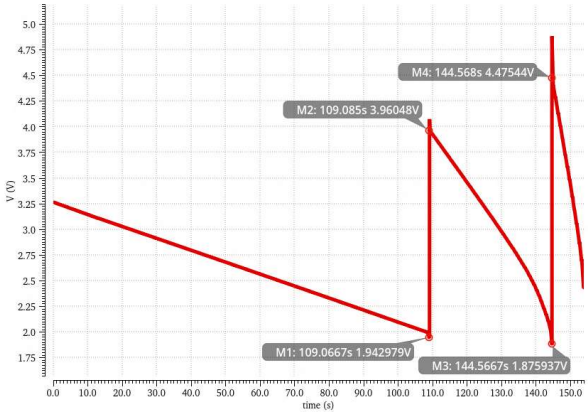
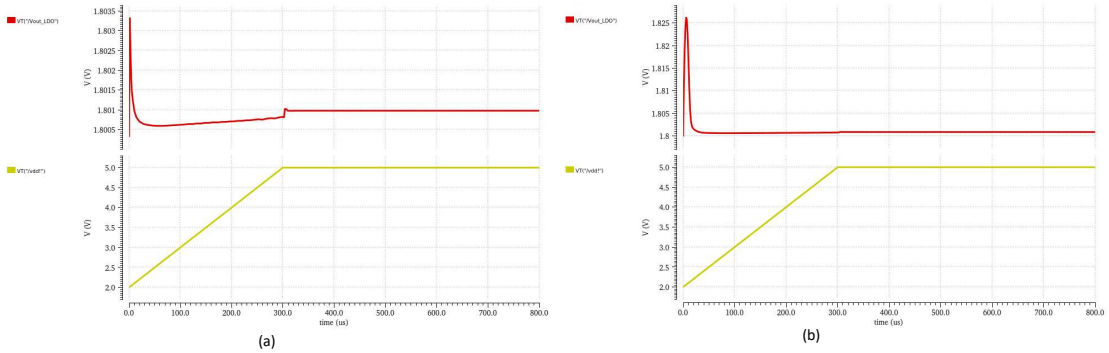


Figure 15: Transient simulation result of the capacitor bank from the energy management unit

Topology switch	Rise time
Topology 1 to 2	18.3ms
Topology 2 to 3	1.3ms

Table 13: Capacitor voltage rise time during topology switch

Transient Simulation- Line Transient Response



(a) (b)

Figure 16: LDO regulator line transient response at (a) I_{load} = 6.7µA (b) I_{load} = 25µA with t_{rise} = t_{fall} = 300µs

I_{load} (µA)	Max. Overshoot (mV)
6.7	3.3
25	25

Table 14: Line transient response maximum overshoot with t_{rise} = t_{fall} = 300µs

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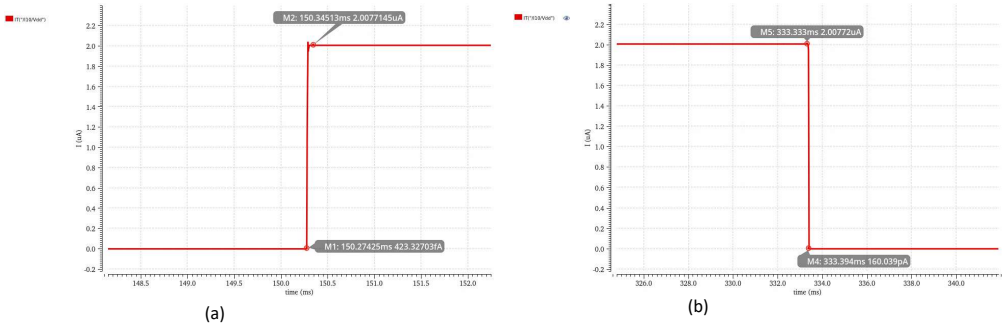
Transient Simulation

- Load transient : Displays the LDO regulator output behavior with a varying load current.
- Input signal rise time and fall time:
  - Input signal t_{rise} = t_{fall} = 60µs (from the behavior of the comparator of the energy management unit)



(a) (b)

Figure 17: Transient response of the comparator supply current from the energy management unit to analyze its (a) rise time (b) fall time.

Rise time	70µs
Fall time	61µs

Table 15: Rise time and fall time analysis of the comparator supply current from the energy management unit

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Transient Simulation- Load Transient Response

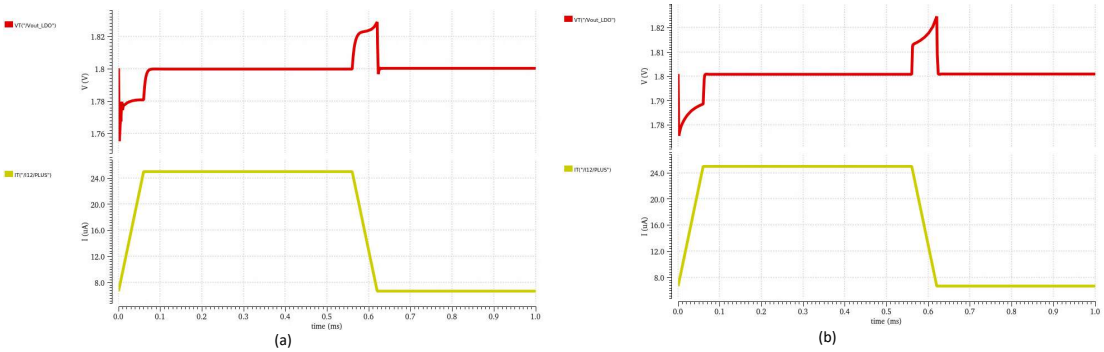

Figure 18: LDO regulator Load transient response at (a) V_{in} = 2V (b) V_{in} = 5V for I_{load} = 6.7µA to 25µA

V_{in} (V)	Max. Overshoot (mV)	Max. Undershoot (mV)
2	28	43
5	24	23.9

Table 16: Load transient response maximum overshoot and undershoot

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Transient behavior under process variations

- Process variations:
  - Typical corner (normal NMOS and normal PMOS)

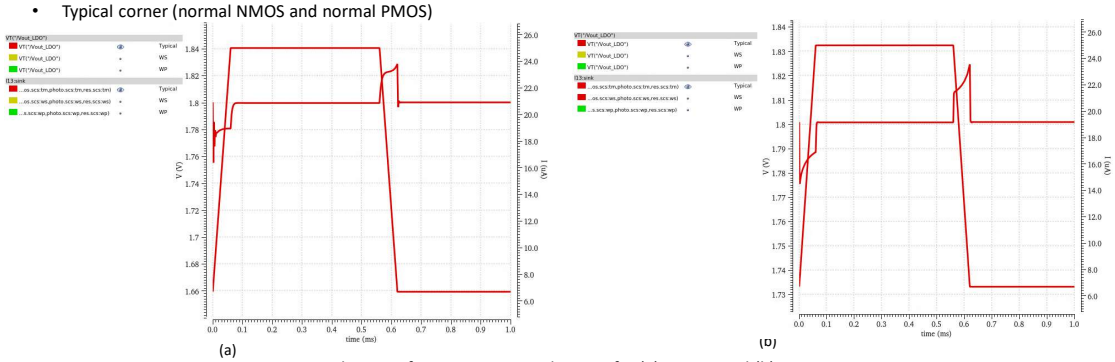

Figure 19: LDO regulator performance at Typical corner for (a) V_{in} =2V and (b) V_{in} = 5V

V_{in} (V)	Max. Undershoot (mV)	Max. Overshoot (mV)
2	43	29
5	23.9	24.4

Table 17: LDO regulator maximum undershoot and overshoot at Typical corner

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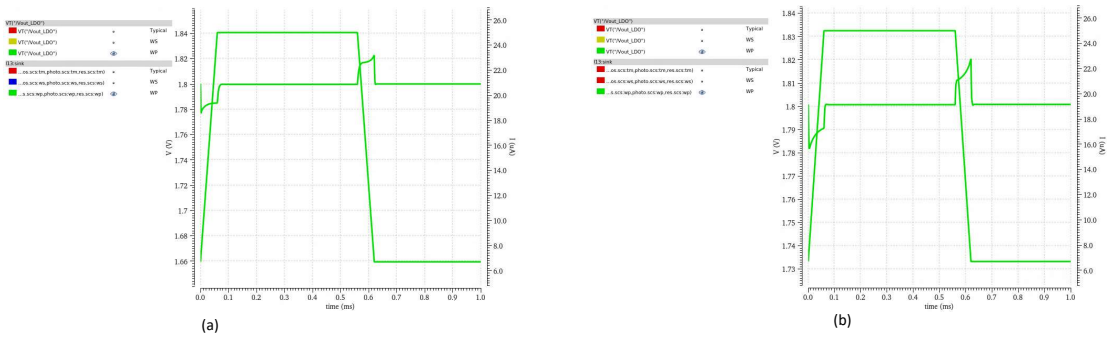
Transient behavior under process variations

- Process variations:
  - Worst power (fast NMOS and fast PMOS)



(a) (b)

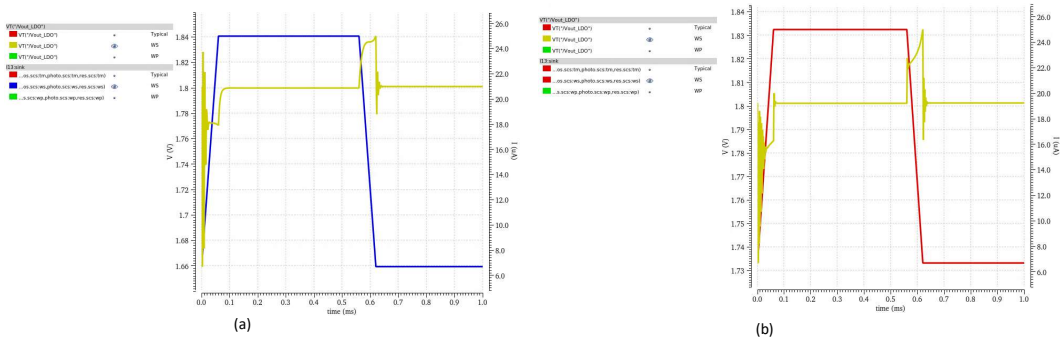
Figure 20: LDO regulator performance at Worst power corner for (a) V_{in} =2V and (b) V_{in} = 5V

V_{in} (V)	Max. Undershoot (mV)	Max. Overshoot (mV)
2	23	22.8
5	18.3	20

Table 18: LDO regulator maximum undershoot and overshoot at Worst power corner

Transient behavior under process variations

- Process variations:
  - Worst speed (slow NMOS and slow PMOS)



(a) (b)

Figure 21: LDO regulator performance at Worst speed corner for (a) V_{in} =2V and (b) V_{in} = 5V

V_{in} (V)	Max. Undershoot (mV)	Max. Overshoot (mV)
2	125.5	40.8
5	63.2	31.7

Table 19: LDO regulator maximum undershoot and overshoot at Worst speed corner

Transient behavior under temperature variations

- Temperatures: $-40^0C, 0^0C, 60^0C, 120^0C$

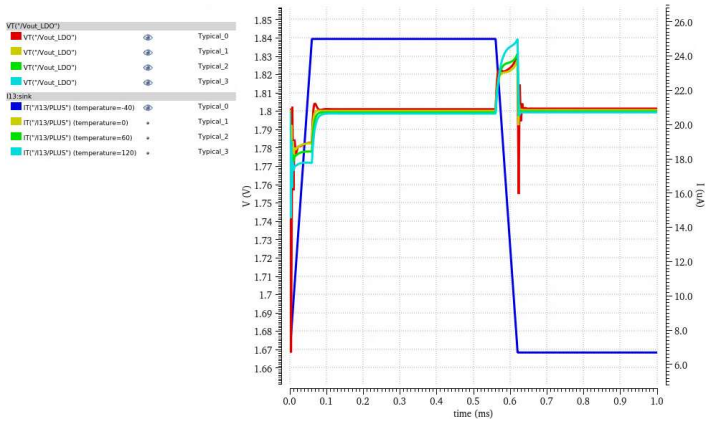


Figure 22: LDO regulator performance at V_{in} =2V for varying temperatures

Temperature (^{0}C)	Max. undershoot (mV)	Max. overshoot (mV)
-40	130	30
0	50	28
60	45	30
120	58	40

Table 20: LDO regulator maximum undershoot and overshoot for varying temperatures at V_{in} =2V

Transient behavior under temperature variations

- Temperatures: $-40^0C, 0^0C, 60^0C, 120^0C$

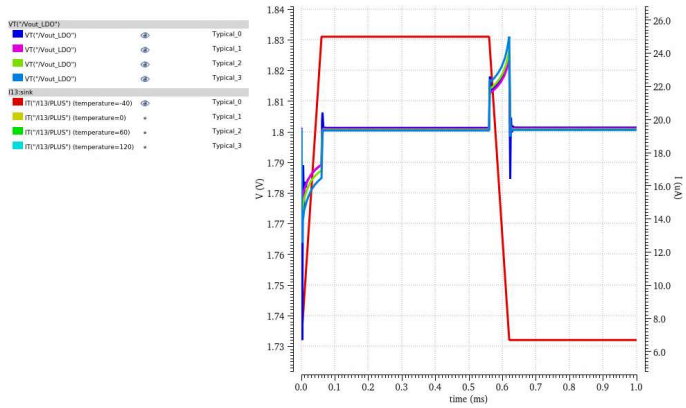


Figure 23: LDO regulator performance at V_{in} =5V for varying temperatures

Temperature (^{0}C)	Max. undershoot (mV)	Max. overshoot (mV)
-40	65	25
0	30	23
60	30	26
120	40	30

Table 21: LDO regulator maximum undershoot and overshoot for varying temperatures at V_{in} =5V

DC Line Regulation

- Defined as the change in output voltage in response to a change in the input voltage at a fixed load current.
- LNR= $\frac{\Delta V_{out}}{\Delta V_{IN}}$
- Commonly tested under maximum load current.
- LNR 0.20mV/V at the point of maximum slope.

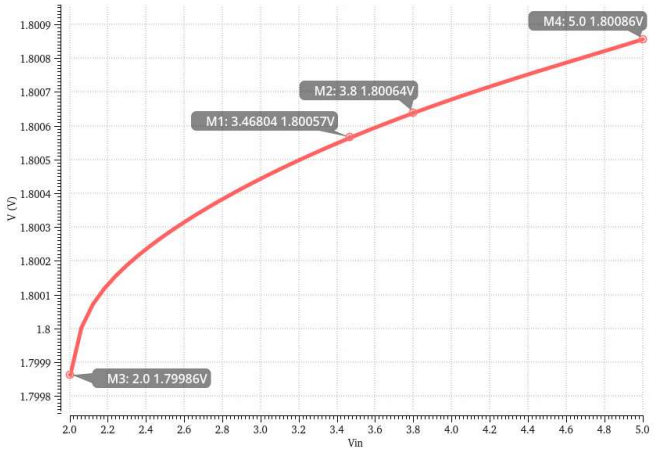
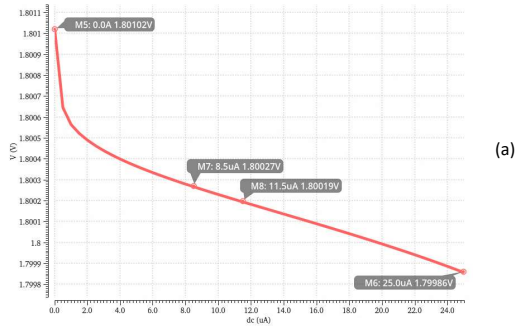


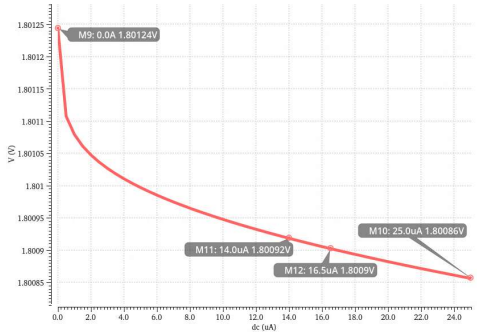
Figure 24: LDO regulator Line Regulation

DC Load Regulation

- Defined as the rate of change of the output voltage in response to a change in the load current, at a constant input voltage.
- LDR= $\frac{\Delta V_{out}}{\Delta I_{load}}$
- Load current is varied from 0 to 25µA.
- LDR 0.026mV/µA at the point of maximum slope for V_{in} =2V.
- LDR 8µV/µA at the point of maximum slope for V_{in} =5V.



(a)



(b)

Figure 25: LDO regulator load regulation for (a) V_{in} =2V (b) V_{in} =5V

Efficiency

- Current efficiency $\eta_I = \frac{I_{load}}{I_{in}} = \frac{I_{load}}{I_{load}+I_Q}$
- Power efficiency $\eta = \frac{V_{in}-V_{DO}}{V_{in}} * \eta_I = \left[1 - \frac{V_{DO}}{V_{in}}\right] \eta_I$
- Quiescent current I_Q :

Parameter	Error amplifier	Pass transistor	Feedback network	Total consumption
I_Q	3.1799µA	13.1nA	13.11nA	3.2µA

Table 22: LDO Regulator total current consumption

- $I_{load(active)}$ = 25µA, $I_{load(inactive/average)}$ = 6.7µA, V_{in} = 2V, V_{DO}=145mV
- η_I = 88.65%, η = 82.22% for $I_{load(active)}$
- η_I = 67.67%, η = 62.76% for $I_{load(inactive/average)}$

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Final results- Summary

Parameter	Specification	Nominal Results
V_{out}	1.8V	1.8V
V_{DO}	<0.2V	145mV
I_Q	-	3.2µA
Gain (worst case)	-	55.5dB
Unity Gain Frequency (worst case)	-	42.94kHz
Phase margin (worst case)	$>45^0$	64.36^0
Power efficiency ($I_{load,active}$)	-	82.22%
Power efficiency ($I_{load,inactive/average}$)	-	62.76%

Table 23: Comparison between specification and final result of the designed LDO regulator

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Possible Improvements

- Instead of a constant voltage source, a voltage reference circuit can be designed as the reference voltage of the error amplifier.
- The common-source PMOS transistor at the error amplifier output stage could be biased in triode region to increase the open-loop gain for higher load currents [4].
- A current amplifier could be used as a capacitance multiplier instead of a high valued Miller capacitor to save chip area [15].

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Thank You