

A Low-Power Low Dropout Regulator for an Energy Management Unit

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Declaration of Authorship

I, M K Akif Alvi Arnab, born on March 1, 1994, hereby declare that I have authored and submitted the project work under the title “A Low-Power Low Dropout Regulator for an Energy Management Unit” on my own. This work was not previously presented to another examination board and has not been published. Only declared sources and auxiliaries were used.

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Abstract

The storage energy is an important parameter for autonomously operating electronic implants. Ideally, sufficient energy has to be provided to power the implant between two recharging cycles. Supercapacitors are used as energy sources in wireless medical implants as they can store energy for a longer time, are available in smaller sizes, and can be recharged in shorter times. An energy management unit consisting of 4 supercapacitors for an electronic osteosynthesis implant is developed by M.Sc Christian Adam at the Institute for Integrated Circuits (IIC) at the Hamburg University of Technology. The supercapacitors have a capacitance of $11mF$ and 3.3V maximum voltage. Initially, the supercapacitors are in parallel connection and can not be discharged below 1.8V which results in the remaining stored energy on the capacitors being lost for the application. Switching the connection from parallel to series between the supercapacitors results in reducing the minimum discharge voltage and increasing the available energy. The energy management unit consists of an inductive energy transmission, a PMOS transmission gate, a switch matrix where the connection between the supercapacitor changes from parallel to series, a digital control unit that controls the topology switch of the supercapacitors, a comparator that compares the supercapacitor voltage coming through a voltage divider with a voltage reference, a timer and a counter that is used to activate the comparator. There are two LDO (low dropout) regulators in the energy management unit. The output from the switch matrix is converted to a stable 1.8V voltage by the main LDO regulator and is sent to the implant. The output from the switch matrix goes to another low-power LDO regulator that powers different circuitry of the energy management unit. The project work focuses on building this low-power low dropout regulator for the energy management unit. As the energy management unit has to operate continuously, the low-power LDO regulator has to be active continuously. Thus a lower power consumption is necessary for the regulator so that the energy management unit does not consume more energy than it supplies by discharging the capacitors to a lower voltage. The LDO regulator is designed in Cadence design environment using X-Fab 180nm XH018 technology. The regulator is designed using a two-stage operational amplifier as an error amplifier, a PMOS transistor as the pass device, and a series of diode-connected PMOS transistors as the feedback network. For the frequency compensation, an internal compensation scheme with a miller capacitor and a zero nulling resistor is followed. Finally, the results show that the LDO regulator exhibits a stable 1.8V output voltage and has a dropout voltage of $145mV$. The regulator achieves a very low quiescent current in the range of micro-amperes.

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Acronyms

AC alternating current.

ASIC application-specific integrated circuit.

CMOS complementary metal-oxide-semiconductor.

DC direct current.

IIC institute for integrated circuits.

LDO low drop out.

LDR load regulation.

LNR line regulation.

MOSFET metal-oxide-semiconductor field-effect transistor.

NMOS n-channel MOSFET.

OPAMP operational amplifier.

OTA operational transconductance amplifier.

PMOS p-channel MOSFET.

PSRR power supply rejection ratio.

SoC system-on-chip.

Chapter 1

Introduction

Power management in electronic circuits is a very important aspect nowadays with ever-decreasing size of electronic devices but the battery efficiency being almost at the same level. The purpose of power management is to reduce power consumption and increase battery life. Modern technologies are pushing towards a complete system-on-chip (SoC) design that requires power management. A SoC requires many building blocks that have different supply requirements. This is where a voltage regulator, DC-DC converter, Switching Regulator, or their combinations are utilized. This master project is on building a low power low dropout regulator (LDO) for the energy management Unit of an Electronic Osteosynthesis implant developed by the Institute for Integrated Circuits at the TUHH. LDO regulators are one of the fundamental building blocks of power management Unit and are used in many battery-powered systems since it provides constant output voltage maintaining line regulation, load regulation, temperature variation, power supply rejection (PSR). The designed LDO regulator will supply a constant 1.8V regulated voltage to the components of the Energy Management Unit.

Topics covered in the project work are:

- Defining the specifications of the LDO Regulator
- Selecting an architecture for the Regulator
- Selecting the right compensation approach
- Deriving specifications for the components of the LDO Regulator
- Simulation of the designed LDO regulator

1.1 Motivation

An Energy Management Unit of an electronic osteosynthesis implant is developed by M.Sc Christian Adam at the Institute for Integrated Circuits(IIC) at the TUHH. The implant is powered by a bank of 4 supercapacitors. Supercapacitors are used because they can be charged at a faster rate and has a longer lifetime (10^6 charging cycles) [14]. Initially, the supercapacitors are in parallel connection and can not be discharged lower than 1.8

volts. The formula for energy stored in a capacitor

$$E = \frac{1}{2}C \cdot V^2 \quad (1.1)$$

The equation of the available energy is

$$E_{avail} = 2 \cdot C_{single} \cdot (V_{max}^2 - V_{min}^2) \quad (1.2)$$

Where C_{single} is the capacitor value of a single capacitor 11mF and V_{max} and V_{min} are the maximum and minimum voltages for all the capacitors. The maximum voltage, in this case, is 3.3V as the selected model was CPH3225A. If it is assumed that the supercapacitors can be completely discharged to 0 volts, meaning $V_{min}=0$, the available energy results in 0.2396J. Discharging the capacitor from the maximum voltage to 1.8 V results in 0.1683 J of accessible energy and thereby 70.24% of the total energy available.

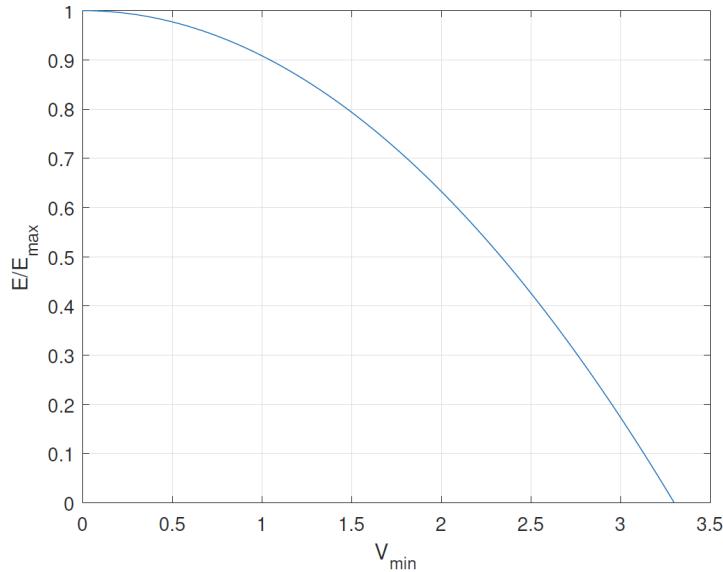


Figure 1.1: Available energy over minimum discharge voltage

The available energy vs minimum discharge voltage curve obtained from [13] in Figure 1.1 shows that the lower the discharging voltage of the supercapacitors, the higher the available energy is. The minimum discharge voltage was achieved by changing the topology from parallel to all supercapacitors in series with an intermediate connection as shown in Figure 1.2 [13]. With all supercapacitors in series, the minimum discharge voltage reduces to 0.45 volt and thus the available energy rises to 0.2351J which is 98.12% of the maximum available energy.

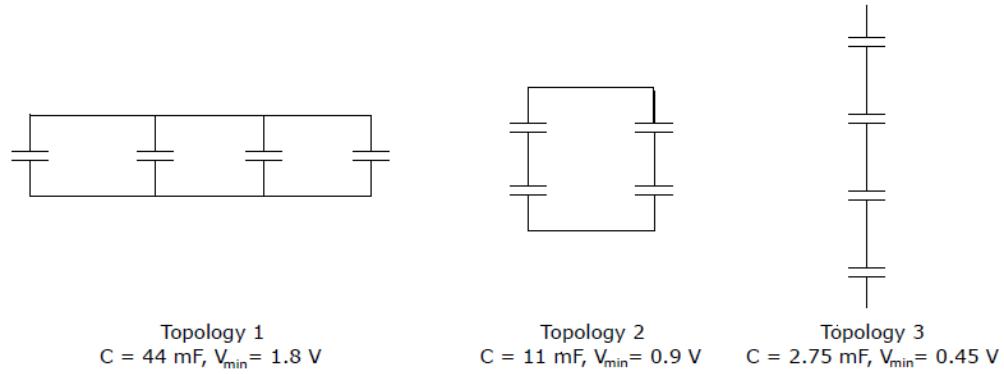


Figure 1.2: Different topologies for supercapacitor connection

1.2 The Energy Management Unit

The Energy Management Unit of the electronic osteosynthesis implant is shown in Figure 1.3. The energy is supplied through inductive energy transmission. A PMOS transmission gate is connected between the clamp cell and the switch matrix of the supercapacitor bank which is only conducting while the charging voltage is present and is avoiding leakage current of the inductive energy transmission. The available energy is maximized by changing the topology of the supercapacitors in the switch matrix from parallel to series. A Digital Control Unit controls the topology switch and the resulting output voltage is converted by the main LDO regulator into a stable voltage of 1.8 and is sent to the main system. The output voltage of the supercapacitor bank V_{cap} also goes to another low-power LDO regulator which will be designed during this project work and will supply constant 1.8V voltage to the parts of the Energy Management Unit such as the voltage reference, the comparator, level shifter, clock, the counter and the digital control. The comparator compares the voltage of the supercapacitor bank through a voltage divider with the voltage reference and the output of the comparator is sent to the digital control unit. The comparator clock signal $CompCLK$ is generated from a timer and is sent to both the comparator and the digital control. The level shifter circuit is used to convert the digital signals at the low voltage level to the voltage level present at the PMOS transmission gate.

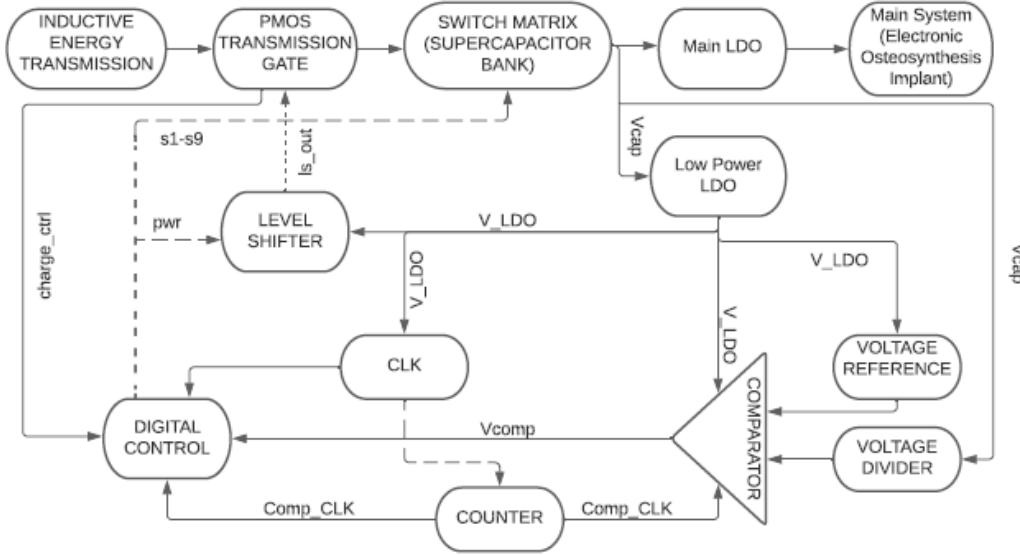


Figure 1.3: Energy management unit of the electronic osteosynthesis implant

1.3 Specification of the LDO Regulator

The LDO regulator will be designed using X-fab 180nm XH018 technology as the main system is designed using the same technology. The input voltage is coming from the output voltage of the supercapacitor bank which is defined as a minimum of 2V to a maximum of 5V and the output of the regulator is 1.8V. The Dropout voltage thus is 200mV. The load current is calculated from the current consumption of all the blocks that will be powered by the LDO regulator in the energy management unit. The maximum current consumption values were obtained from the results presented in the previous project work under load condition of $R_L = 3.6k\Omega$ and $C = 1.1mF$ [13]. The current is distinguished as the active stage and the inactive stage current of the energy management unit. During the inactive stage, only the digital control and the counter are active in the energy management unit and consume a current of roughly $6.7\mu A$ and for the active case, the maximum current consumption was calculated as $25\mu A$.

The specifications are assumptions about the final design. Based on these requirements, the design of the low-power low dropout regulator is carried out. Table 1.1 summarizes the LDO regulator initial specifications.

Parameter	Value
$V_{in,min}$	2V
$V_{in,max}$	5V
V_{out}	1.8V
V_{DO}	200mV
$I_{load(active)}$	25 μ A
$I_{load(inactive)}$	6.7 μ A

Table 1.1: LDO regulator specification

Chapter 2

Types of Voltage Regulators

There are two main types of voltage regulators: linear regulators and switching regulators. Both types regulate a system's voltage, but linear regulators operate with relatively low efficiency, and switching regulators operate with higher efficiency. In high-efficiency switching regulators, most of the input power is transferred to the output without dissipation.

2.1 Linear Regulators

A linear voltage regulator utilizes an active pass device (such as a BJT or MOSFET), which is controlled by a high-gain operational amplifier. To maintain a constant output voltage, the linear regulator adjusts the pass device resistance by comparing the internal voltage reference to the sampled output voltage and then driving the error to zero. These regulators offer a few advantages: they are generally easy to design, dependable, cost-efficient, and offer low noise as well as a low output voltage ripple. Their simplicity and reliability make them intuitive and simple devices for engineers and are often highly cost-effective.

2.2 Switching Regulators

A switching regulator circuit is generally more complicated to design than a linear regulator and requires selecting external component values and careful layout design. Switching regulators can be step-down converters, step-up converters, or a combination of the two, which makes them more versatile than a linear regulator. Advantages of switching regulators include that they are highly efficient, have better thermal performance and can support higher current and wider V_{IN} / V_{OUT} applications. They can achieve greater than 95 percent efficiency depending on the application requirements. Unlike linear regulators, a switching power supply system may require additional external components, such as inductors, capacitors, FETs (field-effect transistors), or feedback resistors.

2.3 Low Dropout Regulator

The Project work is on building a Low Drop out regulator. It consists of a Pass element, a feedback network, an error amplifier, and a compensation network. The feedback network comprises of a resistive voltage divider, which delivers a scaled output voltage that is equal to the reference voltage when the output is at its nominal voltage. The Error Amplifier compares the reference voltage and the voltage from the feedback network. This difference is amplified and the output of the error amplifier drives the pass element to keep the output voltage level at a desired value. Figure 2.1 [17] shows a basic LDO regulator.

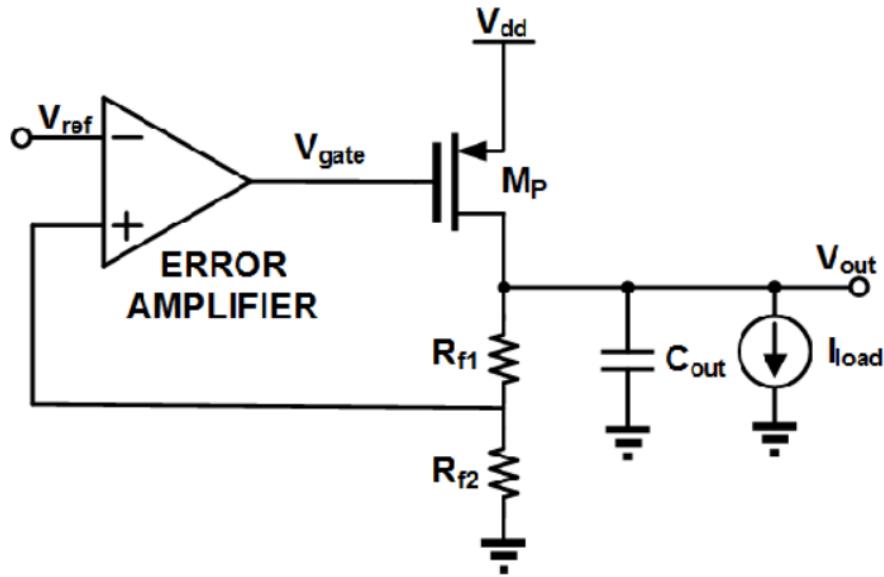


Figure 2.1: Basic low dropout regulator

A classical LDO has three operating regions according to Power Supply V_{in} [4].

Regulation Region The output voltage in this region is high enough for the LDO regulator to perform correctly, delivering stable output voltage and required current to the load.

Dropout Region When the input power is reduced to a level that the LDO regulator can no longer produce a stable output voltage, it enters the Dropout Region. The control loop loses gain and the LDO regulator cannot regulate further, as one or more transistors enter the triode region.

Off Region The voltage level of the power supply is too low to keep all the transistors ON and the circuit is cut-off.

Figure 2.2 [11] represents the LDO regulator operating regions.

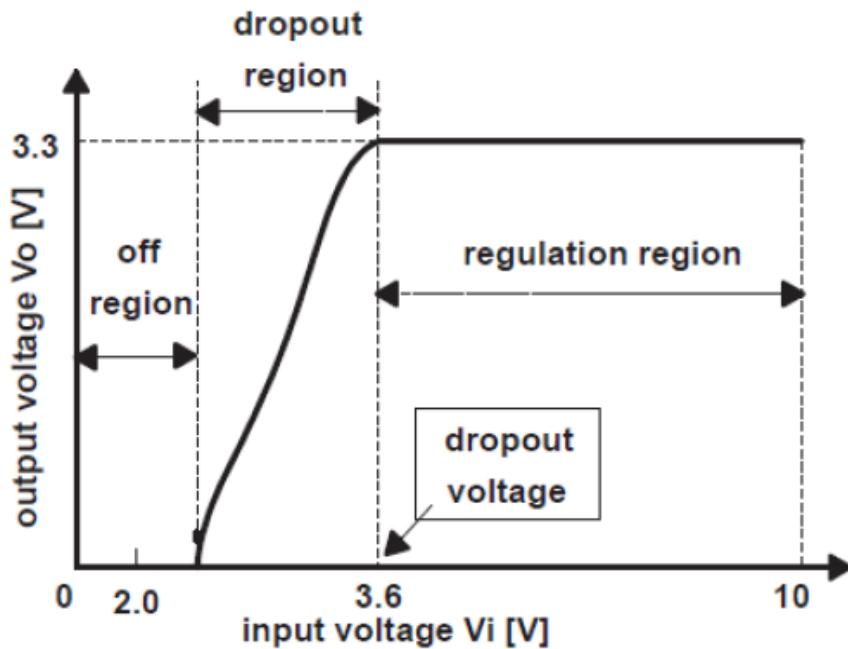


Figure 2.2: LDO regulator operating regions

2.3.1 Voltage Reference

The voltage reference is the starting point of all regulators, setting up the operating point of the error amplifier. In most cases, this voltage reference is of the band-gap type, because it provides the ability to work at low supply voltages. Moreover, its accuracy and stability under varying temperature is sufficient for the design of linear regulators. The design of a voltage reference is not a part of this project work.

2.3.2 Error Amplifier

The error amplifier design is supposed to be kept as simple as possible to keep the current consumption at a low level. The DC open-loop gain should be high under all load conditions to ensure the accuracy of the output. The bandwidth of the amplifier should be large enough to react fast upon changes in the load conditions and input voltages. The output voltage swing of the amplifier is also important because, at low load currents, the pass device needs to be turned off, which leads to the error amplifier output being driven close to one of the supply rails depending on the pass device type. The Error amplifier must satisfy the following requirements [4]

High open-loop gain (A_{OL}) Load regulation is enhanced if the open-loop gain of the system is high.

Low quiescent current (I_Q) Quiescent current has to remain low to extend the battery life and increase the efficiency of the regulator.

Operation under low V_{in} conditions The amplifier must operate properly even if the input voltage supply is low as a consequence of battery discharge.

High bandwidth (BW) The bandwidth should be large enough to reach a fast time response to abrupt changes in load current.

High power supply rejection (PSR) A good PSR means that the output will not be affected by any fluctuation in input supply.

High output voltage swing A high output voltage swing is necessary because the error amplifier drives the pass device to control the current flow that is demanded by the load. The error of the feedback network is sensed by the operational amplifier and it sets the adequate voltage value at the gate of the pass transistor so that it could provide the required current to the load.

2.3.3 Pass Device

The Pass device is used for transferring large currents from the input to the load and is driven by the error amplifier in a feedback loop. Generally, a MOSFET is used as a pass device. NMOS pass element has the advantage of source follower configuration, so the output node is at the source of the transistor, which translates to lower output resistance, which may improve stability, but it depends on the size of the output capacitor [6]. However, an additional step-up voltage converter for error amplifier biasing is required in this configuration to generate sufficient high voltage at the transistor's gate as shown in Figure 2.3 [6].

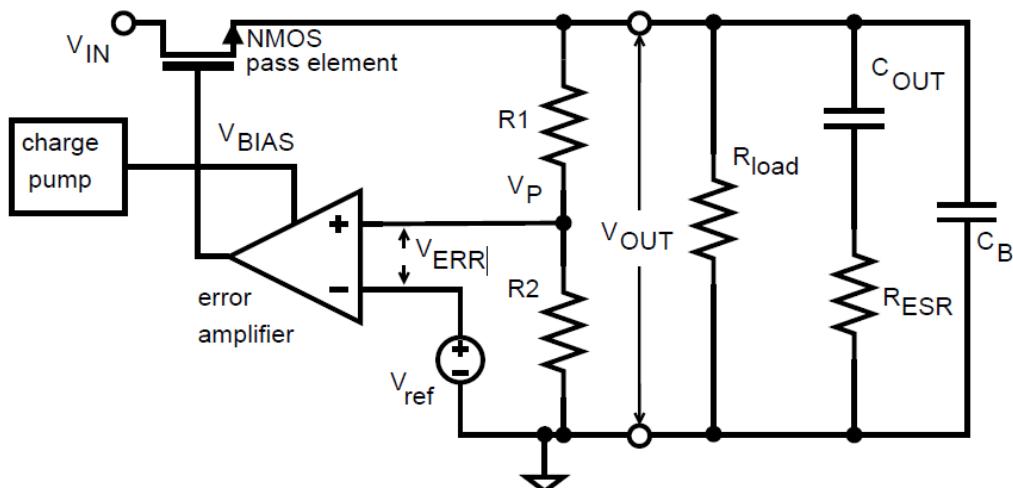


Figure 2.3: LDO with NMOS Pass Device [6].

On the contrary, for the PMOS Pass device, which is typically used in LDO regulators, the error amplifier can be directly biased by the input voltage. One disadvantage, in this case, would be the lower efficiency due to the lower hole mobility or the increased device-width which yields a larger area on silicon. Also, the Miller effect could play a vital role which might lead to an unstable error amplifier.

2.3.4 Feedback Network

The Feedback Network forms a control loop between the error amplifier and the pass transistor. It counteracts the effects of the load and also biases the pass transistor. The output voltage is scaled down to compare against the voltage reference of the error amplifier. As the reference voltage is fixed, the only way to change the output voltage is by changing the configuration of the feedback network. A resistive voltage divider could be used as the feedback network. The current flowing through the divider contributes to the quiescent current of the voltage regulator, so for low consumption, it is necessary to properly scale the value of the resistors so it correlates with the load current and with the current consumption of the error amplifier. The overall quiescent current of the regulator has to be as low as possible, and the resistances have to be in $M\Omega$ to reduce it. This leads to a trade-off between area consumption and parasitic capacitance of the resistors, which may have an impact on the stability of the system and the quiescent current of the LDO voltage regulator. A diode-connected PMOS voltage divider as shown in Figure 2.4 [6] could be a good alternative as it reduces the area of the divider.

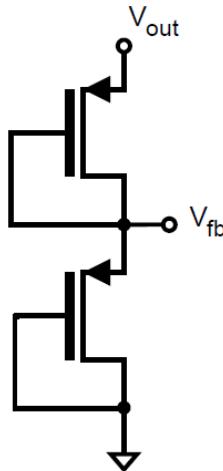


Figure 2.4: MOSFET voltage divider

2.3.5 LDO Regulator Performance Parameters

The most important aspects to take into account in designing a regulator are DC and AC regulating performances, power consumption, and operational requirements. The regulating performance includes load regulation, line regulation, power supply rejection, dropout voltage and efficiency.

Load Regulation Load regulation is a parameter defining the ability of the regulator to maintain the desired output voltage with varying load current. It can be defined as

$$LDR = \frac{\Delta V_{out}}{\Delta I_{load}} \quad (2.1)$$

where ΔV_{out} is the dc change in the output due to a change in the load current I_{load} . A widely variable load would cause considerable voltage swings at the LDO regulator internal nodes, and these changes would be reflected at the output node. Load regulation is highly dependent on the LDO regulator open-loop gain, the input-offset voltages, and the equivalent resistance at the output node. In general, load regulation can be improved if the LDO open-loop gain is increased and the output resistance is decreased.

Line Regulation Line regulation is defined by the change in the output voltage caused by a change in the input voltage at a fixed load current. Line regulation can be described by the following equation

$$LNR = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (2.2)$$

Input voltage variations (ΔV_{in}) can be produced in two ways: directly and indirectly. The first one considers variations through the supply itself, which can be a noisy power source or the output of another regulator. The indirect way is through changes in the voltage reference (V_{ref}). The closed-loop gain of the regulator is expressed by the following equation. It can be observed that any variation in the reference voltage will be amplified in the output.

$$A_{CL} = \frac{V_{out}}{V_{ref}} = \frac{R_{FB2}}{R_{FB1}} + 1 \quad (2.3)$$

Power Supply Rejection Power supply rejection(PSR) is known as the regulator's ability in preventing fluctuation of regulated output voltage caused by input voltage variation. PSR is an AC parameter and can be expressed as

$$PSR = \frac{V_{out}}{V_{in}} \quad (2.4)$$

Dropout Voltage Dropout voltage V_{DO} is as discussed earlier defines as the voltage at which the circuit ceases to regulate against further reductions in input voltage. It can also be expressed as the difference between the minimum supply voltage and the output voltage ($V_{DO} = V_{in,min} - V_{out}$). Dropout voltage is often the limiting factor in the efficient performance of LDO regulators.

Efficiency Efficiency is defined by the fraction of source energy that reaches the load. It is given by

$$\eta = \frac{E_{load}}{E_{source}} \quad (2.5)$$

The energy is defined as how much power P is transferred over time interval t. If the power is kept constant through time, the efficiency can be expressed as

$$\eta = \frac{E_{load}}{E_{source}} = \frac{P_{load.t}}{P_{source.t}} = \frac{I_{load}V_{out}}{I_{in}V_{in}} \quad (2.6)$$

Where E_{load} is the energy required by the load, E_{source} is the energy provided by the source, P_{load} is the power consumption of the load, P_{source} is the power supplied by the source, I_{load} is the load current, V_{in} is the input voltage, and I_{in} is the input current. I_{in} includes I_{load} and quiescent current I_Q . The current efficiency can be defined as

$$\eta_I = \frac{I_{load}}{I_{in}} = \frac{I_{load}}{I_{load} + I_Q} \quad (2.7)$$

Efficiency is one of the most important parameters in the world of portable electronics as the operational life of the battery-powered devices is defined by it. Using the above 2 equations, the expression of efficiency can be obtained as

$$\eta = \frac{V_{out}I_{load}}{V_{in}(I_{load} + I_Q)} = \frac{V_{out}}{V_{in}}\eta_I \quad (2.8)$$

If the quiescent current I_Q is low, the operational life of the battery and the voltage regulator efficiency will be maximized. Remembering that $V_{DO} = V_{in} - V_{out}$

$$\eta = \frac{V_{in} - V_{DO}}{V_{in}} * \eta_I = [1 - \frac{V_{DO}}{V_{in}}]\eta_I \quad (2.9)$$

The overall performance and the quality of the designed LDO regulator can be estimated if the above mentioned points are analyzed.

Chapter 3

Stability and Frequency Compensation

One of the most important aspects of an LDO regulator is its stability. Stability is achieved through a proper compensation approach which can be external or internal. In general, external compensation is achieved through using a high-valued output capacitor in the order of μF . It has some drawbacks as the load capacitor creates an equivalent series resistor whose value changes with frequency. It can lead to a modified AC and transient response. Also, its implementation into very small or lightweight equipment aren't possible. For the internal compensation, Miller compensation is a commonly used approach [20] that provides AC stability and improved transient response. Also, it can be fully integrated into a system-on-chip (SoC). External compensation makes the output pole of the LDO regulator the dominant pole of the whole system [6], whereas, in internal compensation, the pole at the output node of the error amplifier is the dominant one [4]. Other approaches can be found in the literature [2]. In this project work, internal compensation will be used to achieve stability for the LDO regulator and will be discussed in the following sections.

3.1 Feedback Loop

Generally, operational amplifiers are designed to have a high open-loop gain. But they're commonly used in a negative feedback loop to trade-off gain for some desirable properties such as gain desensitization, non-linearity reduction, control of input and output impedance and bandwidth increase of the amplifier [4].

Figure 3.1 [6] shows a basic feedback loop. The loop contains a sampling circuit that senses the output, a gain block A_{OL} , a feedback block β_{FB} and a summation point that performs the summation or subtraction of the inputs based on the polarity of the inputs.

The feedback factor is represented by β_{FB} and A_{OL} is the forward open-loop gain from the summation point to the sampler. The loop gain A_{LG} across the whole loop would be

$$A_{LG} = A_{OL}\beta_{FB} \quad (3.1)$$

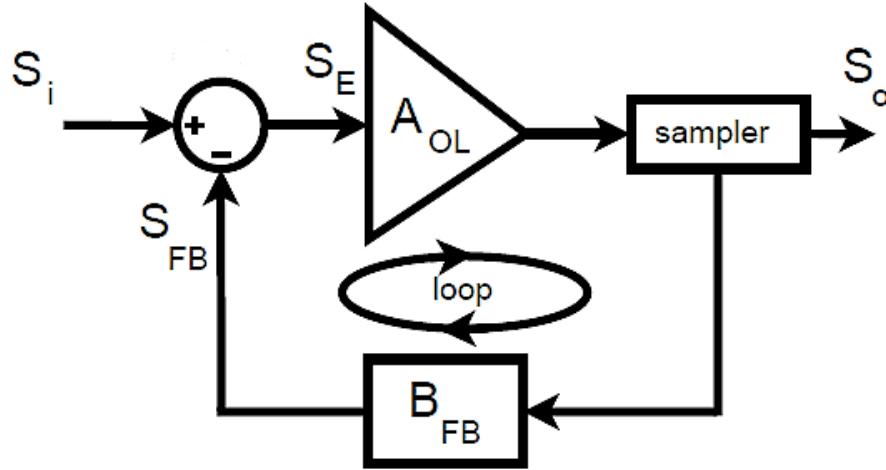


Figure 3.1: Block representation of a feedback loop

The negative sign in the input summation point indicates the feedback loop is negative feedback. So, the gain across the loop is inverting. If A_{OL} or β_{FB} becomes negative, the feedback becomes positive which may lead to instability, depending on the magnitude of A_{OL} .

The error signal S_E is the difference between the input signal S_i and the feedback signal S_{FB} . The regulation effect is obtained from A_{OL} itself, as the system stabilizes when S_E is close to zero.

$$S_E = S_i - S_{FB} = S_i - S_E A_{OL} \beta_{FB} = S_i - S_E A_{LG} = \frac{S_i}{1 + A_{LG}} \quad (3.2)$$

The above equation shows that S_E is closer to zero with higher A_{LG} . Therefore, increasing the loop gain results in better accuracy.

$$S_{FB} = S_E A_{OL} \beta_{FB} = S_E A_{LG} = (S_i - S_{FB}) A_{LG} = \frac{S_i A_{LG}}{1 + A_{LG}} \approx S_i \quad (3.3)$$

The feedback factor β_{FB} senses the output signal S_o and translates it to be comparable with the input signal S_i .

$$S_o = (S_i - S_{FB}) A_{OL} = (S_i - S_o \beta_{FB}) A_{OL} = \frac{S_i A_{OL}}{1 + A_{OL} \beta_{FB}} \approx \frac{S_i}{\beta_{FB}} \quad (3.4)$$

The closed-loop gain A_{CL} can be defined as

$$A_{CL} = \frac{S_o}{S_i} = \frac{A_{OL}}{1 + A_{OL} \beta_{FB}} \approx \frac{1}{\beta_{FB}} \quad (3.5)$$

From the equations, it can be understood that the feedback factor defines how the output is scaled to the input at steady-state and the open-loop gain defines how fast the system is regulating itself to match the scaled output to the input.

3.2 Uncompensated LDO Regulator

In this section, the LDO regulator behavior with a no compensation approach will be discussed. Figure 3.2, reproduced from [4] shows an LDO regulator without any compensation and the nodes at which the most important poles occur. We can see that there are 2 major poles, one at the output of the error amplifier, pole 1, and the other one at the output of the LDO regulator, pole 2. Pole 1 is defined by the error amplifier output and the gate capacitance of the pass device whereas pole 2 is defined by the PMOS pass device's drain capacitance and the load impedance.

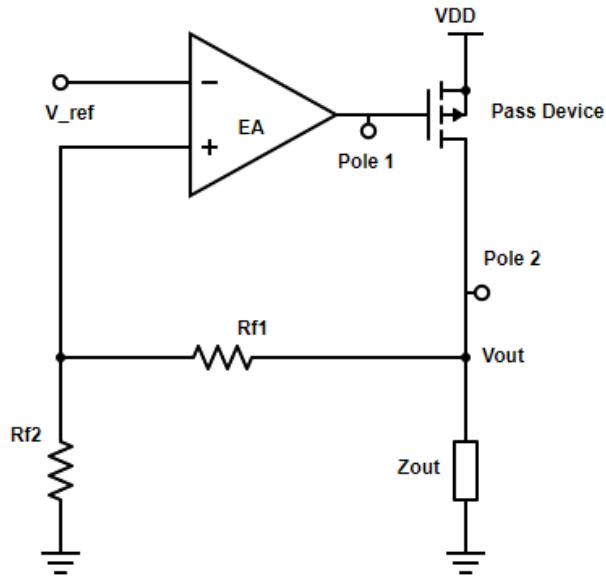


Figure 3.2: LDO regulator poles

An uncompensated LDO regulator frequency response is shown in Figure 3.3 [4]. The main problem with this LDO regulator is the system becomes unstable in the occurrence of a change in load. It makes the output pole move towards the origin and as a result, causes a loss in phase and thus, the system leads towards instability. When the demanded LDO regulator output current decreases, the pole moves towards the origin. The phase margin gets reduced and the system leads to instability. If the output current increases, the output resistance of the pass transistor decrease, causing the pole to move away from the origin and also reducing the regulator's DC gain. Moreover, the transient response also experiences a very large undershoot which almost reaches zero voltage. A proper compensation approach is necessary to rectify the above issues and make the system stable.

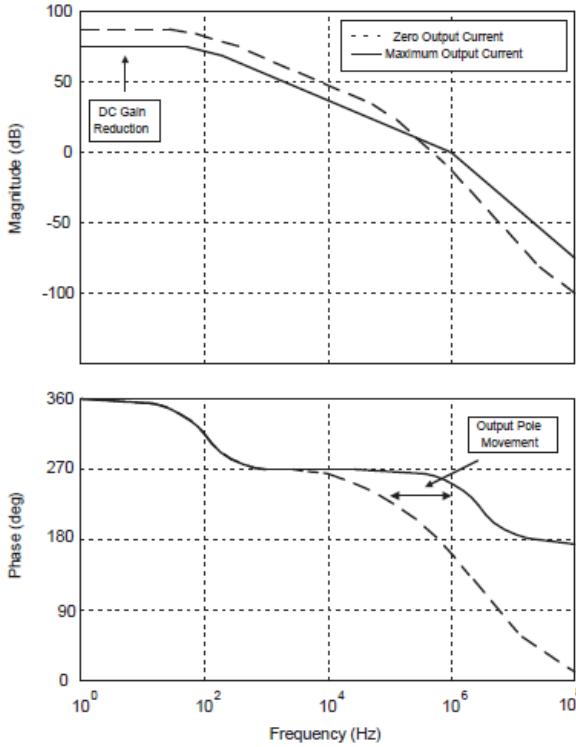


Figure 3.3: Uncompensated LDO regulator frequency response

3.3 Internal Compensation

The internally compensated LDO regulators, also known as capacitor-less LDOs, allow the LDO regulator to be fully integrated with other circuits in the same system on chip (SoC). This compensation scheme doesn't depend on a large output capacitor or its equivalent series resistance and provides AC stability and improves the transient response.

From Figure 3.2, we know the LDO regulator has 2 major poles. The approximate pole location can be expressed as

$$f_{p,out} = \frac{1}{2\pi r_{eq} C_{Load}} \quad (3.6)$$

$$f_{p,EA} = \frac{1}{2\pi r_{out,EA} C_{PT}} \quad (3.7)$$

where r_{eq} is the equivalent resistance formed by the parallel connection of the pass transistor output resistance, the feedback resistance, and the load resistance, C_{Load} is the load capacitance, $r_{out,EA}$ is the error amplifier output resistance, C_{PT} is the total equivalent capacitance at the pass transistor gate. In an uncompensated LDO regulator, the pole at the output of the error amplifier and the pole at the output of the LDO regulator

are both at low frequencies, which causes the system to be unstable. Theoretically, stability would be achieved if the output pole is placed far away from the error amplifier pole, which is achieved through internal compensation.

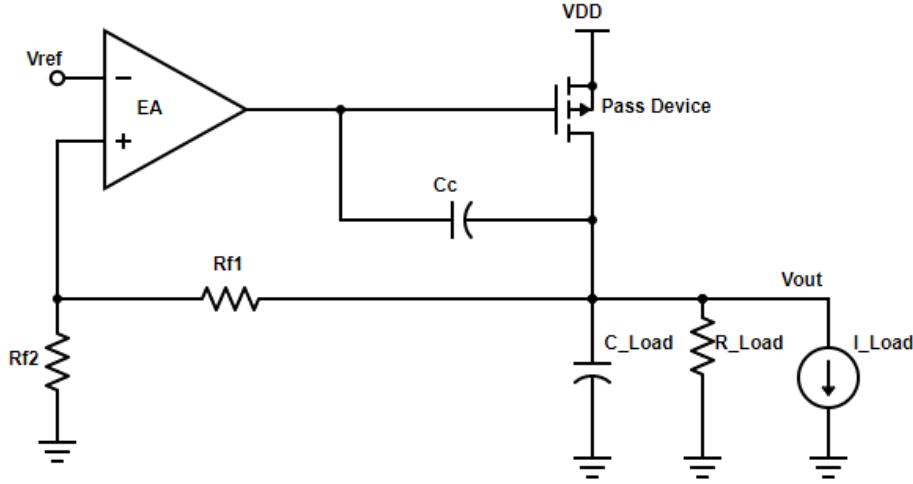


Figure 3.4: Internally compensated LDO Regulator

Figure 3.4, reproduced from [4] shows an internally compensated LDO regulator with a miller capacitor C_c . The miller capacitor determines the dominant pole. The small-signal equivalent circuit of the open-loop miller compensated LDO regulator could be shown as in Figure 3.5 [4].

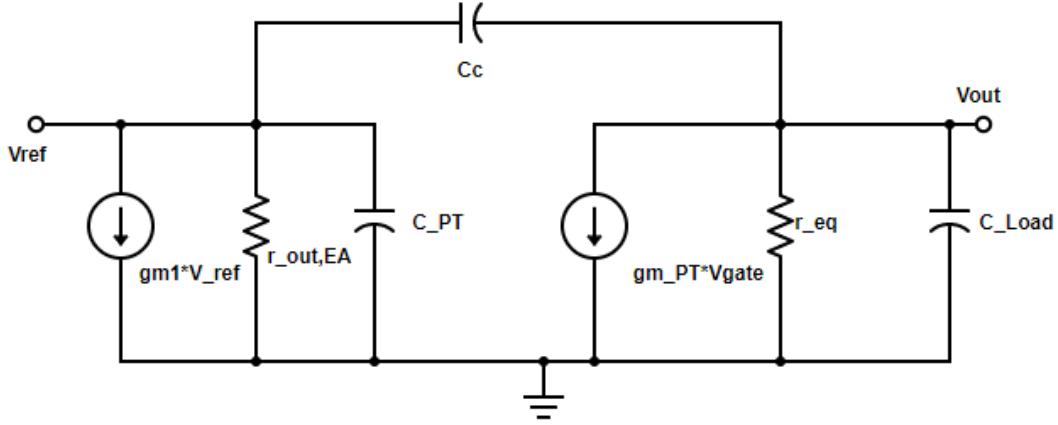


Figure 3.5: Small-signal equivalent circuit of the open-loop miller compensated LDO regulator

where gm_{PT} is the pass transistor transconductance, $r_{out,EA}$ and C_{EA} are the equivalent output resistance and capacitance at the output node of the error amplifier, C_c is the compensation capacitor, r_{eq} is the

equivalent resistance at the output node and C_{Load} is the load capacitance.

The location of the dominant pole (P_d) and the first non-dominant pole (P_{nd}) are given by the following equations

$$P_d = -\frac{1}{r_{out,EACPT} + (C_c + C_{Load})r_{eq} + gm_{PT}r_{out,EAr_{eq}}C_c} \quad (3.8)$$

$$P_{nd} = -\frac{gm_{PT}C_c}{(C_{Load} + C_c)C_{PT}} \quad (3.9)$$

However, a zero is also created due to the presence of the miller capacitor. To achieve stability, the zero has to be moved far away to the right half side of the s-plane or placed at the same frequency as the first non-dominant pole, so they both cancel each other. A zero nulling resistor is a good option in this regard. The location of the zero with a zero nulling resistor R_z is given by:

$$z = \frac{1}{(\frac{1}{gm_{PT}} - R_z)C_c} \quad (3.10)$$

R_z nullifies the effect of the zero created by the miller capacitor and a higher value of it moves the zero further into the right half side of the s-plane, making the system more stable. If R_z is increased further as $R_z > 1/gm_{PT}$, the zero can be moved towards the left half side of the s-plane and can cancel out the non-dominant pole, making the system even more stable. Thus, stability is achieved for the voltage regulator. Figure 3.6, reproduced from [4] shows the internally compensated LDO regulator with a miller capacitor and a zero nulling resistor.

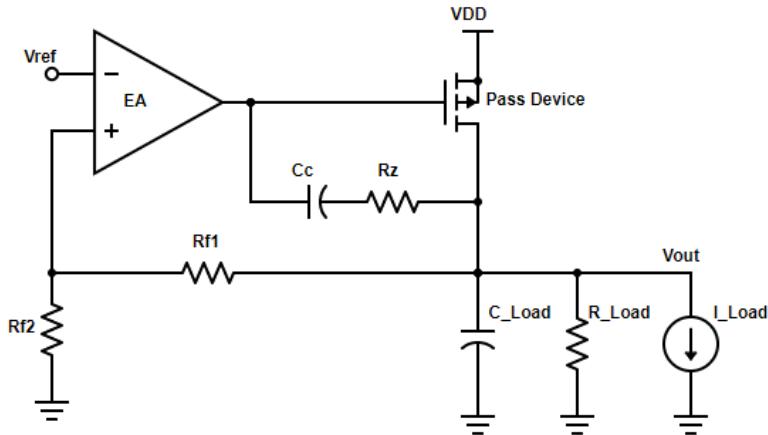


Figure 3.6: Internally compensated LDO regulator with a zero nulling resistor

Chapter 4

LDO Regulator Components Design

In this chapter, the value of the LDO regulator components will be defined. All the sections represent the design procedure of different blocks. The whole design is implemented on X-fab 180nm XH018 technology. The NMOS and PMOS transistors used are 6V NMA, PMA, and 1.98V PE.

4.1 Process Parameters

The effective mobility of the transistors was calculated through a DC simulation. The PMOS β_{eff} was calculated using a PMA transistor and 2 DC voltage sources as shown in Figure 4.1. The gate voltage V_g was swept from 0 to 3.3V with a 1000 linear step size. The transistor Width(W) and Length(L) were both swept from $1\mu m$ to $4\mu m$ with a step size of $500nm$.

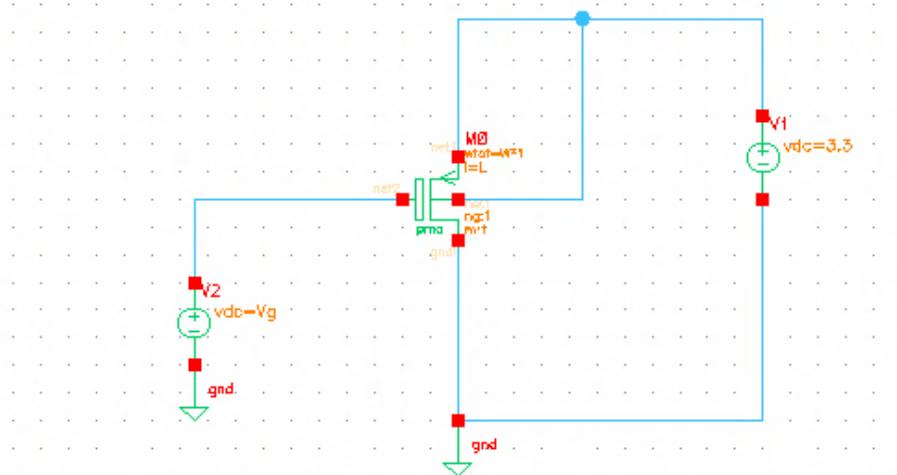


Figure 4.1: PMOS Circuit for $\beta_{eff,p}$

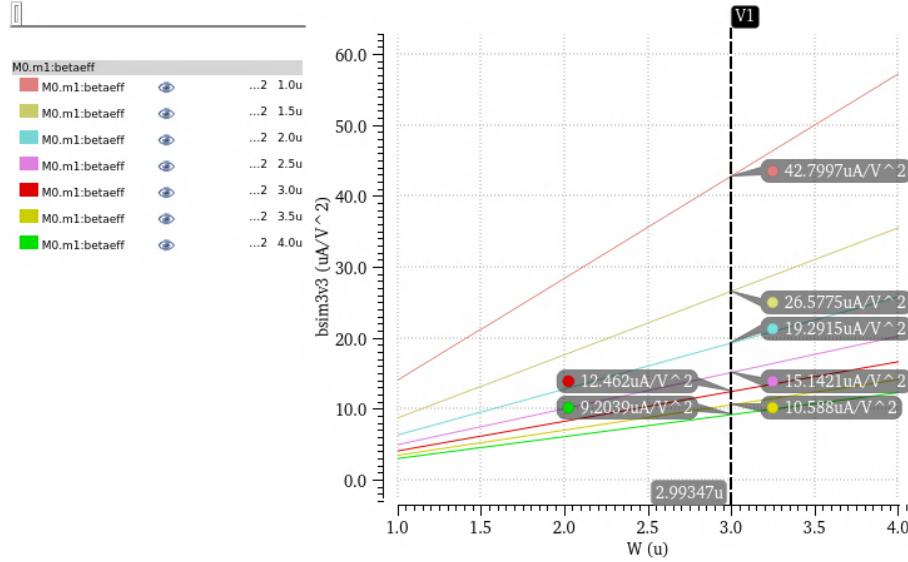
Figure 4.2: Simulation result for $\beta_{eff,p}$ circuit

Figure 4.2 shows the simulation result for the $\beta_{eff,p}$ circuit. As we know,

$$\beta_{effective} = \mu_p C_{ox,p} \frac{W}{L} \quad (4.1)$$

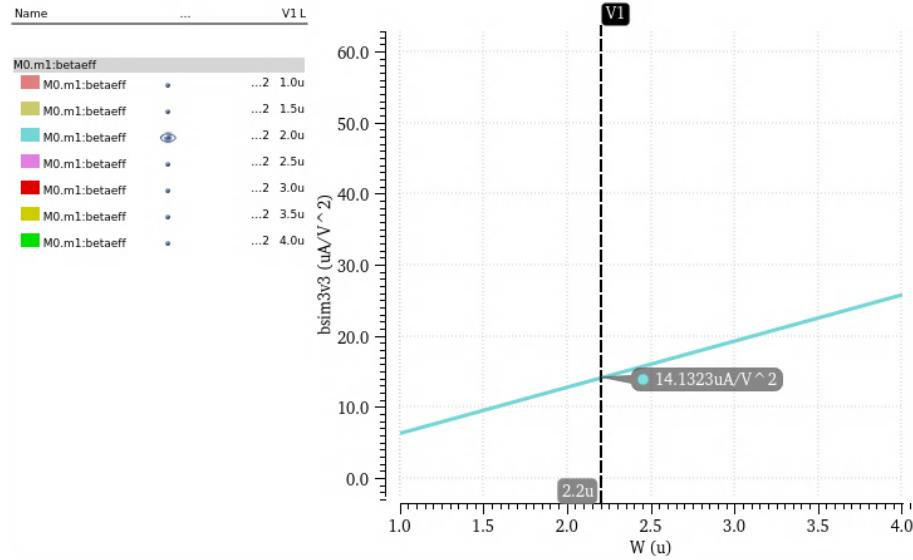
where β is a process parameter, μ is charge-carrier effective mobility, C_{ox} is the Capacitance of the gate oxide, and W and L are the channel width and length of the transistors respectively. From the graph, we can see if $L = 1.0\mu m$, $W = 3.0\mu m$, then β_{eff} is $42.8939\mu A/V^2$ So we can find the $\mu_p C_{ox,p}$ as

$$\mu_p C_{ox,p} = \frac{\beta_{effective}}{\frac{W}{L}} = \frac{42.8939\mu}{\frac{3}{1}} = 14.23\mu \frac{A}{V^2} \quad (4.2)$$

If we take another value for example if $L = 2.0\mu m$, $W = 3.0\mu m$, then β_{eff} is $19.2915\mu A/V^2$ So we can find the $\mu_p C_{ox,p}$ as

$$\mu_p C_{ox,p} = \frac{\beta_{effective}}{\frac{W}{L}} = \frac{19.2915\mu}{\frac{3}{2}} = 12.861\mu \frac{A}{V^2} \quad (4.3)$$

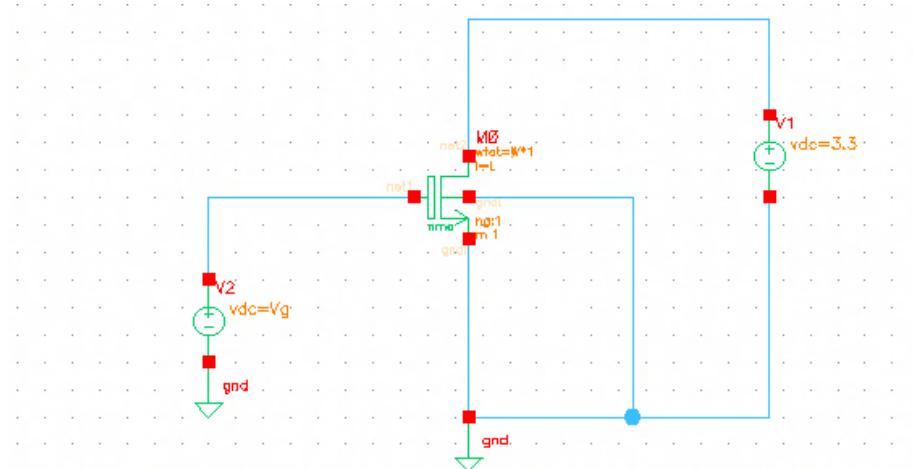
or if $L = 2.0\mu m$, $W = 2.20\mu m$ as shown in Figure 4.3, then β_{eff} is $14.1323\mu A/V^2$ So we can find the $\mu_p C_{ox,p}$ as

Figure 4.3: $\beta_{eff,p}$ for $W = 2.2\mu m$ and $L = 2.0\mu m$

$$\mu_p C_{ox,p} = \frac{\beta, effective}{\frac{W}{L}} = \frac{14.1323\mu}{\frac{2.2}{2}} = 12.85\mu \frac{A}{V^2} \quad (4.4)$$

As the values are closer, the value of $\mu_p C_{ox,p}$ was chosen as $12.85 \mu \frac{A}{V^2}$.

Similarly, The NMOS β_{eff} was also calculated using an NMA transistor and 2 DC voltage sources as shown in Figure 4.4. The gate voltage V_g was swept from 0 to 3.3V with a 1000 linear step size. The transistor Width(W) and Length(L) were both swept from $1\mu m$ to $4\mu m$ with a step size of $500nm$.

Figure 4.4: NMOS Circuit for $\beta_{eff,n}$

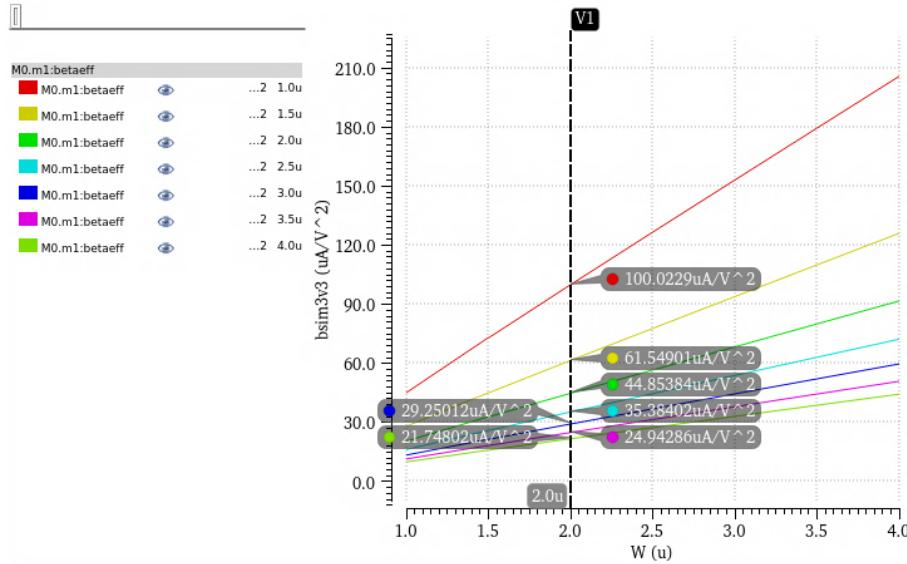
Figure 4.5: Simulation result for $\beta_{eff,n}$ circuit

Figure 4.5 shows the simulation result for the $\beta_{eff,n}$ circuit. The $\mu_n C_{ox,n}$ was calculated in a similar process as $\mu_p C_{ox,p}$, and the value was chosen as $46.16 \mu \frac{A}{V^2}$.

For 1.98V PE transistors, the same process was followed and the $\mu_p C_{ox,p}$ for PE transistors were chosen as $28.69 \mu \frac{A}{V^2}$.

Another important process parameter is the Threshold voltage of the transistors. They were obtained from the X-FAB process and device specification document and are listed in the table below.

Parameter	Low(V)	Typical(V)	High(V)	$\mu C_{ox} (\mu \frac{A}{V^2})$
PMA	-1.05	-1.2	-1.35	12.85
NMA	1.13	1.23	1.33	46.16
PE	-0.67	-0.7	-0.73	28.69

Table 4.1: Process Parameters for the transistors

4.2 Pass Transistor

PMOS pass transistor was chosen due to its comparatively low dropout voltage, as opposed to NMOS and bipolar implementations. The design was completed with $V_{DD} = 2V$ to $5V$ with $V_{min} = 2V$, $I_{load} = 25\mu A$, $V_{out} = 1.8V$. With these parameters, the aspect ratio of the pass device can be figured out. V_{SG} can be figured out by assuming a minimum value for the gate voltage of the pass device, which is the output voltage of the error amplifier. Let's say it's 300mV. And the worst-case voltage for the V_S terminal should be considered to have the full load current flowing through it. In that case, it's the minimum input voltage of 2V. So V_{SG}

$= V_{IN,min} - V_G = 2 \text{ V} - 300\text{mV} = 1.7 \text{ V}$. The operating region for the transistor, in this case, is Linear as $V_{SD} = 2\text{V} - 1.8\text{V} = 0.2\text{V}$ is less than $V_{SG} - |V_{Th,p}| = 1.7 - 1.2 = 0.5\text{V}$. We know from the square-Law equation of Mosfet operating in Linear Region,

$$I_D = \mu_p C_{ox,p} \frac{W}{L} [(V_{SG} - |V_{Th,p}|) - \frac{V_{SD}}{2}] V_{SD} \quad (4.5)$$

$$(W/L)_{pass} = \frac{I_D}{\mu_p C_{ox,p} [(V_{SG} - |V_{Th,p}|) - \frac{V_{SD}}{2}] V_{SD}} \quad (4.6)$$

$$(W/L)_{pass} = \frac{25 \times 10^{-6}}{12.85 \times 10^{-6} \times (0.5 - \frac{0.2}{2}) \times 0.2} = 24.32 \approx 24 \quad (4.7)$$

The channel length of the pass device was chosen as $L = 2.5\mu\text{m}$, so the channel width for the pass device was $W = 2.5 \times 24 = 60\mu\text{m}$. In the simulation, the value of W was increased up to $68\mu\text{m}$.

Parameter	Value
Minimum Input Voltage $V_{in,min}$	2V
Load Current I_{load}	$25\mu\text{A}$
Channel Width W	$68\mu\text{m}$
Channel Length L	$2.5\mu\text{m}$

Table 4.2: Parameters for the pass device

4.3 Feedback Network

The task of the feedback network is to provide the voltage to the positive input terminal of the error amplifier which would be close to the reference voltage, in this case, 1.2V . The feedback network consists of 2 or more resistors operating as a voltage divider. An important issue is the current flowing through them, which has to be minimized to decrease power consumption. The following equations show the voltage divider transfer function and the current flowing through them

$$\frac{V_{out}}{V_{ref}} = \frac{R_{f1} + R_{f2}}{R_{f2}} \quad (4.8)$$

$$I_{req} = \frac{V_{out}}{R_{f1} + R_{f2}} \quad (4.9)$$

Where V_{out} is the LDO regulator output voltage, V_{ref} is the reference voltage, R_{f1} and R_{f2} are feedback resistors and I_{req} is the current flowing through them. The current flowing through the feedback branch was chosen to be very low, approximately 0.052% of the maximum load current ($I_{load} = 25\mu\text{A}$) to be 13nA . Solving equation 4.8 and 4.9 gives

$$R_{f2} = \frac{V_{ref}}{I_{req}} = \frac{1.2}{13n} = 92.3M\Omega \quad (4.10)$$

$$R_{f1} = \frac{V_{out}}{I_{req}} - R_{f2} = \frac{1.8}{13n} - 92.3M = 46.15M\Omega \quad (4.11)$$

However, using resistors as the voltage divider is not the best possible approach because the resistors are made of high resistivity polysilicon. It consumes a large area and matching between the resistors is important in the fabrication process. A better approach would be using diode-connected PMOS transistors as the voltage divider. The transistors used here are 1.98V PE transistors and they operate in the sub-threshold region as the gate-source voltage is lesser than the threshold voltage. The voltage divider should divide the voltage in the ratio of the feedback resistors, in that case, $R_{f2}/R_{f1} = 2 : 1$. So three diode-connected PMOS transistors are used and the feedback voltage is provided from the drain potential of the first transistor. Each transistor needs to have the voltage drop of $V_{SD} = 600mV = V_{SG}$ and the current flowing through them is $I_{req} = 13n$. Replacing the known parameters into the MOS quadratic equation for the sub-threshold region, the W/L ratio of the feedback network transistors could be figured out.

$$\frac{W}{L} = \frac{I_{req}}{\mu_p C_{ox,p} (n-1) V_t^2 e^{-V_{Th}/nV_t} e^{V_{SG}/nV_t} (1 - e^{-V_{SD}/V_t})} \quad (4.12)$$

Equation 4.12 obtained from [18] represents the formula to find out the W/L ratio for transistors operating in the sub-threshold region. Where $\mu_p C_{ox,p}$ is the product of the charge-carrier effective mobility and the gate oxide capacitance and was found to be $28.69 \mu \frac{A}{V^2}$ for PE transistors, V_t is the thermal voltage of $26mV$, n is the sub-threshold swing coefficient of 1.5 [18] and V_{Th} is the threshold voltage. Substituting all the values in the equation results in a W/L ratio of 8.11. As in the sub-threshold region, the square law equation doesn't describe the circuit accurately [18], to obtain an I_{req} value of $13nA$, the W/L ratios of the transistors were adjusted to 0.9 making the channel length $2.22\mu m$ and the channel width $2\mu m$. Table 4.3 represents the parameters of the feedback network.

Parameter	Value
Output Voltage V_{out}	1.8V
Reference Voltage V_{ref}	1.2V
Bias Current I_{req}	13nA
Channel Width W	$2\mu m$
Channel Length L	$2.22\mu m$

Table 4.3: Parameters for the feedback network

4.4 Error Amplifier

One of the most important blocks of the LDO regulator is the error amplifier. Its task is to provide a constant and stable output proportional to the amplifier's gain and the voltage difference between a voltage used as a reference voltage and voltage from the feedback network. The output voltage of an ideal error amplifier can be given by [3]

$$V_{out} = A_v(V^+ - V^-) \quad (4.13)$$

In general, an operational amplifier is used as an error amplifier of the LDO such as a basic differential pair

[22], a two-stage amplifier [7], a folded cascade amplifier [8], a symmetric OTA (operational transconductance amplifier) [15], class-AB amplifiers [9]. Normally single-stage amplifiers have very little gain and a higher gain is better for line and load regulation of the LDO. Therefore a 2 stage operational amplifier is used for this LDO regulator design.

4.4.1 Error Amplifier specification

The first thing before designing an error amplifier is to define the specifications. From the Energy management Unit of the electronic osteosynthesis implant, the specifications for the whole LDO regulator were defined. The clock frequency used in the energy management unit is 30Hz [13]. The Settling time of the LDO regulator is assumed to be 10 times the clock frequency, so $30\text{Hz} \times 10 = 3000\text{Hz}$ or $333.33\mu\text{s}$. The Unity Gain Frequency(UGF) is approximately a reciprocal of the settling time as so was calculated as $1/333.33\mu\text{s} \approx 3\text{KHz}$ [4]. The Gain Bandwidth product of the LDO was thus calculated as $2 \times pi \times UGF = 18.85\text{KHz}$. The slew rate is assumed to be roughly ten times faster than the settling time specification, assuming the output slews one-half of the supply rail [3]. Therefore, the value of the slew rate was calculated as $0.015\text{V}/\mu\text{s}$. The open-loop gain of the 2-stage operational amplifier was assumed to be $\geq 60\text{dB}$. To avoid overshoot, the phase margin was defined to be 90° [3]. The relation between the load capacitor C_L and the compensation capacitor C_c is carried out by the following equation of a two-pole system [3]

$$PM = 180^\circ - \arctan\left(\frac{\omega_u}{\omega_{p1}}\right) - \arctan\left(\frac{\omega_u}{\omega_{p2}}\right) - \arctan\left(\frac{\omega_u}{\omega_{z1}}\right) \quad (4.14)$$

Where ω_{p1} , ω_{p2} , and ω_z are the locations of the dominant pole, the first non-dominant pole, and the zero respectively. $(\frac{\omega_u}{\omega_{p1}})$ is the open-loop DC gain and PM is the phase margin. Since a 90° phase margin makes the step response of an operation amplifier behave like a first-order response, similar to that of an RC circuit [5], the system with a 90° phase margin would ideally have only one pole. If ω_z is assumed to be located at 10 times the unity gain frequency ω_u , the relation between the unity gain frequency and the non-dominant pole was found to be $\omega_u = 0.08 \times \omega_{p2}$. The unity gain frequency ω_u can be termed as gm_{in}/C_c and the non-dominant pole frequency ω_{p2} can be termed as gm_{out}/C_L . gm_{in} and gm_{out} are input and output stage transistor's transconductance. Since the zero ω_z is assumed to be located at 10 times the unity gain frequency ω_u , the relation between the input and output stage transistor's transconductance can be written as $gm_{out} = 10 \times gm_{in}$. Finally, the relation between C_c and C_L was found to be $C_c \geq 1.25 \times C_L$. In the full LDO regulator design, the capacitance at the output node of the error amplifier will be the equivalent parasitic capacitance of the error amplifier output node and the pass device, which is from the simulation found to be in the order of femtofarads. From the simulation, to have a 90° phase margin for both the minimum and maximum input voltages of the LDO regulator, the compensation capacitor's value was chosen as 20pF .

Defining the value of the input common-mode range was another important specification of the design for which the topology of the 2 stage opamp needed to be changed. The common-mode voltage of the 2-stage opamp needs to be 1.2V or close to 1.2 V as we know from the common-mode equation

$$V_{CM} = \frac{V_{ref} + V_{fb}}{2} = \frac{1.2 + 1.2}{2} = 1.2 \quad (4.15)$$

This point will be discussed more while describing the choice of the topology in the following section.

4.4.2 Choosing the Input Stage

At first, an NMOS input pair 2 stage opamp was chosen. While deriving the aspect ratios of the transistors in the opamp, it was found out the values were very low for all the transistors and at a point practically impossible. For this reason, the W/L ratios of the first-stage transistors were assumed to be 1. The biasing current was chosen to be $1\mu A$. However with $V_{CM} = 1.2$, the $V_{DS,5}$ was coming out to be negative. From figure 4.6 [12] we can say

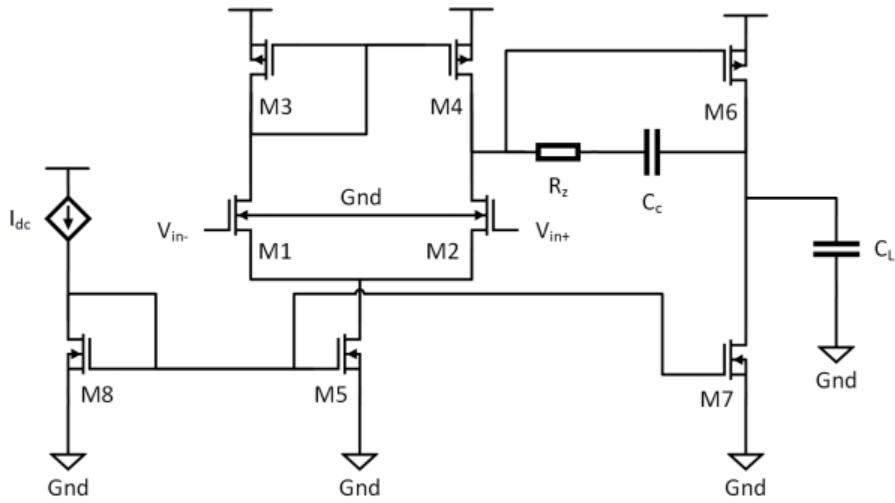


Figure 4.6: 2 Stage Opamp with NMOS Input Stage

$$V_{DS,5} = V_{in,min} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{TH1,max} \quad (4.16)$$

$$V_{DS,5} = V_{in,min} - \sqrt{\frac{I_5}{\mu_n C_{ox,n}(W/L)_1}} - V_{TH1,max} \quad (4.17)$$

$$V_{DS,5} = 1.2 - \sqrt{\frac{1\mu}{46.8\mu \times 1}} - 1.33 = -0.27 \quad (4.18)$$

To avoid this, the topology was changed to PMOS differential pair as shown in Figure 4.7, reproduced from [21]. The location of poles and zeros remain the same and so the C_L and C_c values remain as before [10]. The W/L ratios of the input stage transistors are in general chosen from gm_1 and gain-bandwidth GBW values.

$$gm_1 = GBW \times C_c = 18.85k \times 20p = 3.77 \times 10^{-7} S \quad (4.19)$$

The $(W/L)_1$ can be directly obtained from gm_1 by Equation 4.20 [3]

$$(W/L)_1 = \frac{gm_1^2}{\mu_p C_{ox,p} I_5} \quad (4.20)$$

Where I_5 is the biasing current of $1\mu A$ mirrored to transistor M_5 and $\mu_p C_{ox,p}$ for 6V PMA transistor is $12.85 \mu A/V^2$ as calculated in section 4.1. Substituting the values in the equation results in $(W/L)_1$ as 11.06×10^{-3} . Since the obtained value is very low, the W over L ratios of the input stage transistors were chosen as 1 and using $(W/L)_1 = 1$ in equations 4.19 and 4.20, the gm_1 and the GBW were recalculated as $3.6\mu S$ and $179.2kHz$ respectively. The W/L of the current mirror stage can be calculated from the minimum common-mode equation which is

$$V_{CM,min} = V_{SS} - |V_{TH,1}| + V_{TH,3} + V_{dsat,3} \quad (4.21)$$

$$V_{CM,min} = V_{SS} - |V_{TH,1}| + V_{TH,3} + \sqrt{\frac{I_5}{\mu_n C_{ox,n} (W/L)_3}} \quad (4.22)$$

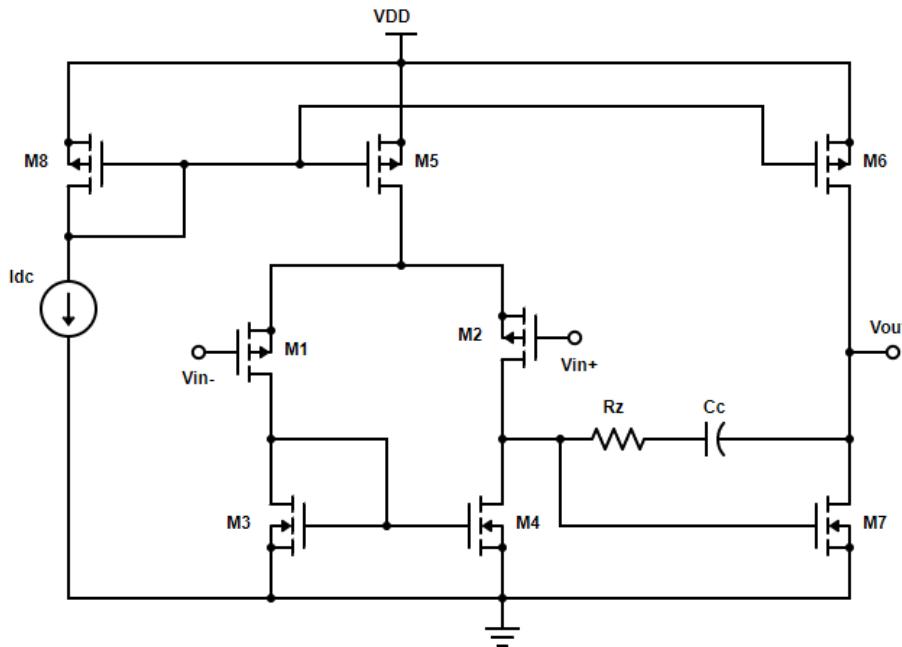


Figure 4.7: 2 Stage Opamp with PMOS Input Stage

The common-mode voltage that would be applied to the inputs of the error amplifier is 1.2V. Since there was no specification about the range of the common-mode voltage where all the transistors will remain in saturation, the minimum and maximum common-mode voltage were calculated by the maximum and minimum common-mode equations assuming the aspect ratios of the transistors as 1. If $(W/L)_3 = 1$, then from equation 4.22, the minimum common-mode voltage is 176mV. The aspect ratio of M_5 was calculated from the maximum common-mode voltage equation which is

$$V_{CM,max} = V_{DD} - V_{dsat,5} - V_{gs,1} \quad (4.23)$$

$$V_{CM,max} = V_{DD} - \sqrt{\frac{2 \times I_5}{\mu_p C_{ox,p}(W/L)_5}} - \sqrt{\frac{I_5}{\mu_p C_{ox,p}(W/L)_1}} - |V_{TH,1}| \quad (4.24)$$

If the supply voltage of the error amplifier is 4V, then the $V_{CM,max}$ voltage using equation 4.24 is 2.34V with $(W/L) = 1$.

One important thing we need to check is if this common-mode voltage range also satisfies the conditions when the supply voltage is 2V. As the supercapacitor bank minimum voltage is 2 V [13], the error amplifier needs to be functioning with the minimum input voltage. The minimum V_{DD} required by this topology to keep all the transistors in saturation is

$$V_{DD} = V_{CM,max} + |V_{TH,1}| - \sqrt{\frac{I_5}{\mu_p C_{ox,p}(W/L)_1}} - \sqrt{\frac{2 \times I_5}{\mu_p C_{ox,p}(W/L)_5}} \quad (4.25)$$

As the common-mode voltage at least needs to be 1.2V and $V_{TH,1}$ of the 6V PMA transistor is also close to 1.2V as we know from table 4.1 , V_{DD} can never be 2V and keep all the transistors in saturation. Thus, this topology too can not satisfy the conditions of the desirable LDO regulator.

Finally, it was decided that an NMOS input pair 2 stage opamp with keeping the input stage transistors in the sub-threshold region and keeping all other transistors in the saturation region will be used. As we know, in the sub-threshold region, $V_{GS} < V_{TH}$, a voltage of 1.2V can be supplied to the positive and negative input terminals of the amplifier for a minimum V_{DD} of 2V. The W/L ratios of the input stages transistors were calculated by the drain current equation for the sub-threshold region.

$$\frac{W}{L} = \frac{I_D}{\mu_n C_{ox,n}(n-1)V_t^2 e^{-V_{TH}/nV_t} e^{V_{GS}/nV_t} (1 - e^{-V_{DS}/V_t})} \quad (4.26)$$

Where $\mu_n C_{ox,n}$ is the product of the charge-carrier effective mobility and the gate oxide capacitance of the NMA transistors and was found to be $46.16 \mu \frac{A}{V^2}$ from section 4.1, V_t is the thermal voltage of $26mV$, n is the sub-threshold swing coefficient of 1.5 [18] and V_{TH} is the threshold voltage. V_{GS} was assumed as 1.2V and V_{DS} was assumed to be greater than 4 times the thermal voltage V_t [23], as approximately 0.2V. Substituting the values resulted in a W/L ratio of the input stage transistors of 64.1.

However, the simple square law equation doesn't provide accurate results in the sub-threshold region. In the simulation, the (W/L) values of the input stage transistors were increased up to 200. The W/L ratios of the other transistors were also analyzed during the simulation. As these transistors need to be in saturation, the square law equation for drain current in saturation region was used. Using the DC operating point voltages of drain and source terminal of all the transistors, the W/L ratios to keep them in saturation were defined. The drain current equation for transistors operating in the saturation region is given by

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (4.27)$$

Equation 4.27 can be re-arranged to have an expression for V_{GS} and $V_{GS} - V_{TH} = V_{GS, effective} = V_{dsat}$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu C_{ox}(\frac{W}{L})}} + V_{TH} \quad (4.28)$$

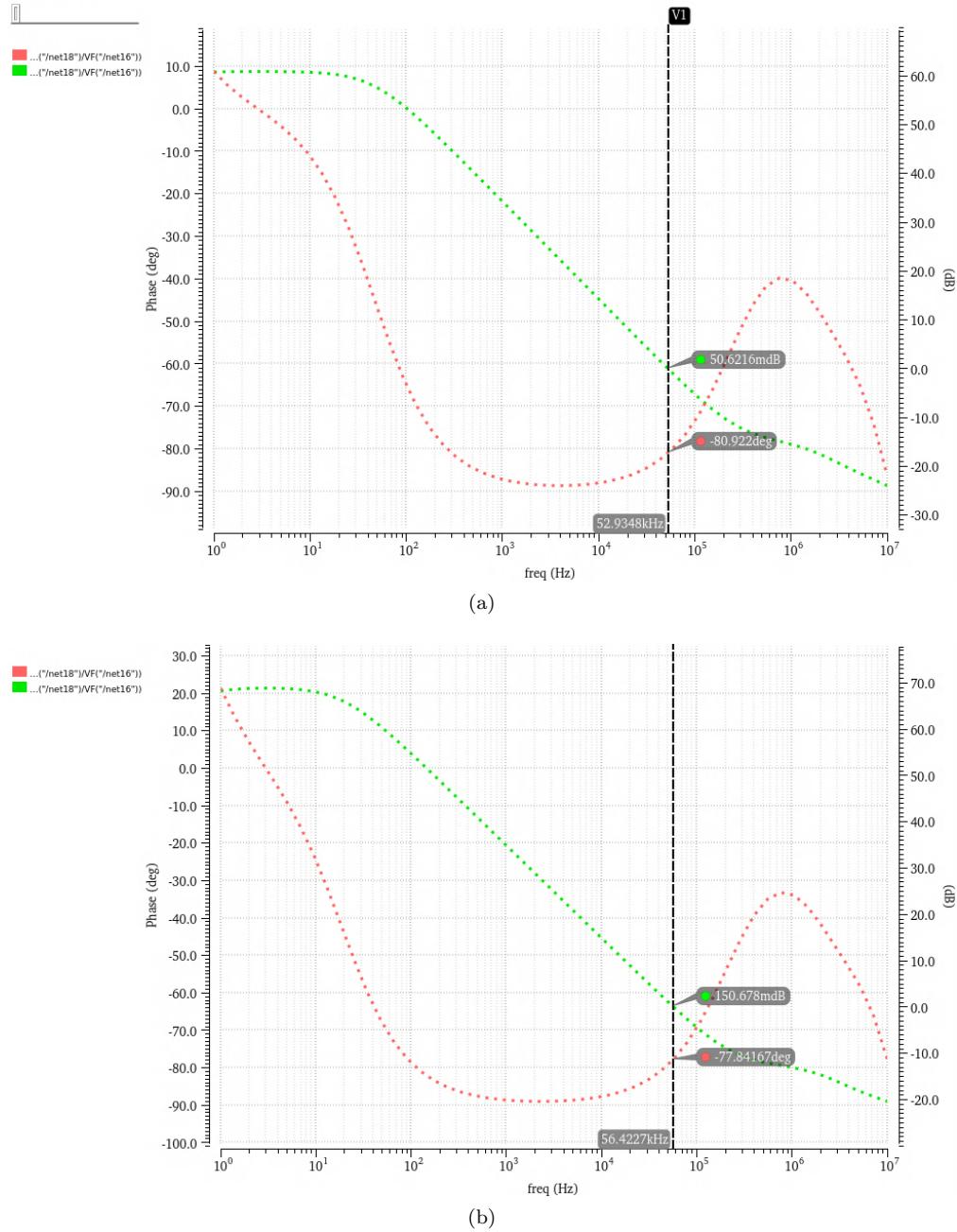
$$V_{dsat} = \sqrt{\frac{2I_D}{\mu C_{ox}(\frac{W}{L})}} \quad (4.29)$$

The W/L ratios of the current mirror stage transistors were chosen as 1 and for M5, it was chosen as 8. From the simulation, to keep M6 and M7 in saturation, their aspect ratios were chosen as 2.5 and 8 respectively. The transistor widths and lengths are listed in Table 4.4. The current through the output branch was 853.8nA and the resistance R_z was $1/gm_6 = 1/6.671\mu \approx 150K\Omega$. The reason for choosing R_z as $1/gm_6$ is described in detail in section 4.5. Finally, in the full LDO regulator design, the R_z value of the error amplifier was increased to $163.3K\Omega$. The schematic of the design is shown in Appendix A.1.

Parameter	Width(W)(m)	Length(L)(m)	Operating Region
$M_{1,2}$	200μ	1μ	Sub-threshold
$M_{3,4}$	2.5μ	2.5μ	Saturation
M_5	8μ	1μ	Saturation
M_6	2.5μ	1μ	Saturation
M_7	8μ	1μ	Saturation
M_8	8μ	1μ	Saturation

Table 4.4: Error Amplifier Transistor Sizes

However, later in the full LDO regulator design, the load transient simulation for the worst-speed corner at the maximum supply voltage of 5V resulted in ringing and the output did not settle down to a stable 1.8V voltage. To rectify this issue, the biasing current of the error amplifier was increased up to $1.2\mu A$ keeping all other values as before. The open-loop gain from the AC simulation was found to be 60.88dB and the phase margin was 99.08 degrees for an input voltage of 2V. The gain and phase margin for the maximum input voltage of 5V for this error amplifier was found to be 68.8dB and 102.16 degrees. To perform the open-loop frequency analysis, a resistance-capacitance RC circuit was used as feedback with the values of the resistor as $100M\Omega$ and the capacitor as $10\mu F$. The schematic of the amplifier with a $1.2\mu A$ bias current and its dc operating points is shown in Appendix A.2 and the frequency response is shown in Figures 4.8a and 4.8b.

Figure 4.8: Error amplifier frequency response at (a) $V_{in} = 2V$ (b) $V_{in} = 5V$

4.5 Frequency Compensation calculation

As it was discussed in chapter 3, frequency compensation is a major parameter in defining the LDO regulator stability. The compensation approach selected for this design was internal compensation as shown in Figure 3.6. In this section, the value of the compensation capacitor C_c and the zero nulling resistor R_z is calculated.

To determine C_c , first, the desired phase margin of the LDO regulator has to be defined. Figure 4.9 from [3] shows the time response of second-order closed-loop system with various phase margins. It is observed that a larger phase margin results in less ringing of the output signal. It is important to have an adequate phase margin to keep the undesirable ringing to an acceptable level.

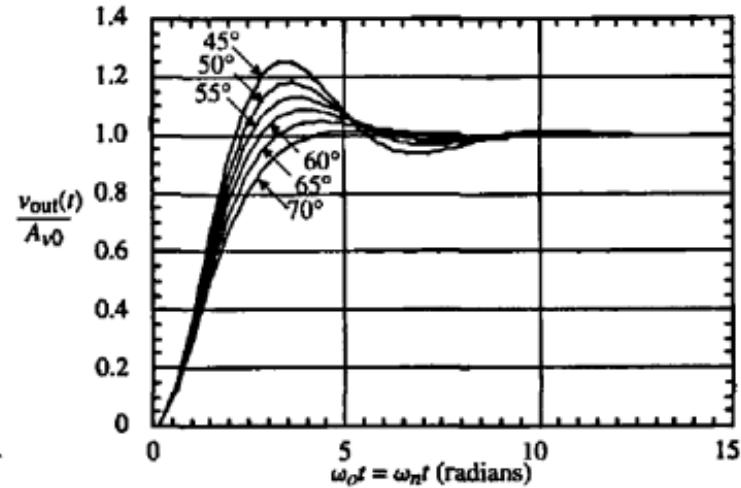


Figure 4.9: Response of a second-order system with various phase margins

Moreover, the error amplifier was designed to have a phase margin of 90° . A 90° phase margin makes the step response of an operational amplifier behave like a first-order response, similar to that of an RC circuit [5]. So in the whole LDO regulator, there are two poles, one at the error amplifier output node and the other at the LDO regulator output node. To avoid ringing or to keep it at an acceptable level, the phase margin was decided to be 75° . Using equation 4.14 and substituting the values (assuming that the right half-plane zero is placed at or beyond ten times the gain-bandwidth), the relation between the compensation capacitor C_c and the load capacitor C_L can be determined

$$PM = 180^\circ - \arctan\left(\frac{\omega_u}{\omega_{p1}}\right) - \arctan\left(\frac{\omega_u}{\omega_{p2}}\right) - \arctan\left(\frac{\omega_u}{\omega_{z1}}\right) \quad (4.30)$$

Where ω_u is the unity gain frequency, ω_{p1} defines the location of the dominant pole which is the error amplifier output pole, ω_{p2} defines the location of the non-dominant pole which is the pole at the output node of the LDO regulator, $(\frac{\omega_u}{\omega_{p1}})$ is the open-loop DC gain of the LDO regulator, in this case, assumed to be ≥ 60 dB as a higher open-loop gain is desirable for a better line and load regulation of the regulator, phase margin

$PM = 75^\circ$, ω_{z1} is located at least 10 times the unity gain frequency ω_u .

$$\arctan\left(\frac{\omega_u}{\omega_{p2}}\right) = 180^\circ - PM - \arctan\left(\frac{\omega_u}{\omega_{p1}}\right) - \arctan\left(\frac{\omega_u}{\omega_{z1}}\right) \quad (4.31)$$

$$\arctan\left(\frac{\omega_u}{\omega_{p2}}\right) = 180^\circ - 75^\circ - \arctan(60) - \arctan(0.1) = 10.244 \quad (4.32)$$

$$\left(\frac{\omega_u}{\omega_{p2}}\right) = \tan(10.244) = 0.18 \quad (4.33)$$

$$\omega_u = 0.18 \times \omega_{p2} \quad (4.34)$$

Since the zero is located 10 times the unity gain frequency

$$\omega_z = 10 \times \omega_u \implies \frac{gm_{PT}}{C_c} = 10 \times \frac{gm_{in}}{C_c} \implies gm_{PT} = 10 \times gm_{in} \quad (4.35)$$

Where gm_{in} and gm_{PT} are the input stage and the output stage (in this design the pass transistor is the output stage transistor) transconductance respectively.

From 4.34

$$\omega_u = 0.18 \times \omega_{p2} \implies \frac{gm_{in}}{C_c} = 0.18 \times \frac{gm_{PT}}{C_L} \quad (4.36)$$

$$\frac{gm_{in}}{C_c} = 0.18 \times \frac{10 \times gm_{in}}{C_L} \quad (4.37)$$

$$\frac{C_L}{C_c} = 1.8 \implies C_L = 1.8 \times C_c \quad (4.38)$$

$$C_c \geq 0.55 \times C_L \quad (4.39)$$

The values of C_L and C_c were chosen as 1pF and 500fF respectively. Finally, in the simulation, it was observed that the C_c value of 100fF resulted in better a phase margin for the maximum supply voltage of 5V. Moreover, the line transient simulation showed better response with the updated C_c value. Thus, the compensation capacitor value used for the final design was 100fF.

The value of compensation resistor R_z using equation 3.10 has to be set in a way to move the zero to the left-half of the s-plane. If the value of R_z is increased keeping $R_z < (1/gm_{PT})$, the zero will move further to the right-half side of the s-plane. If $R_z > (1/gm_{PT})$, the zero can be moved to the left-half side of the s-plane and its value can be increased in a way that it cancels out the non-dominant pole, which will ensure better stability. Figure 4.10 from [19] shows pole zero location of a two-pole system. We can see that by varying the value of R_z , we can move the zero further away to the right-half side of the s-plane or move the zero to the left-half side of the s-plane and even compensate the non-dominant pole.

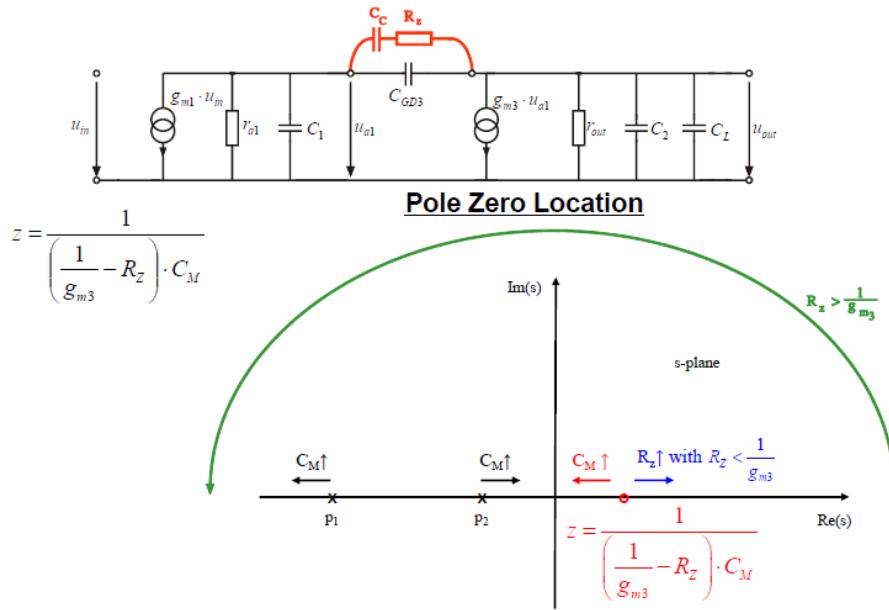


Figure 4.10: Location of the zero in a two-pole system for a varying zero nulling resistor

In this LDO regulator design, the value of R_z was set as $R_z = 1/gm_{PT}$. In this way, the zero can be placed way beyond the unity gain frequency of the LDO regulator, ensuring the stability of the regulator. From the simulation, the value of gm_{PT} for $V_{in} = 2V$ at $25\mu A$ load current was found to be $70.65\mu S$. Thus, the value of R_z resulted in $1/70.65\mu S = 14.15K\Omega$. One important point is, the pass-transistor transconductance changes with varying supply and load conditions. For $V_{in} = 5V$ with the maximum load current, the pass-transistor transconductance results in $107.3\mu S$, for $V_{in} = 2V$ with minimum load current of $6.7\mu A$, the pass-transistor transconductance is $49.2\mu S$ and for $V_{in} = 5V$ with $I_{load} = 6.7\mu A$, the pass-transistor transconductance results in $52.3\mu S$.

The goal of R_z is to set the zero way beyond the unity gain frequency. Having a fixed R_z value of $14.15K\Omega$ in the final design satisfies all other conditions as well. If we substitute the values of gm_{PT} for the conditions mentioned above in equation 3.10 and have R_z and C_c as $14.15K\Omega$ and $100fF$ respectively, the frequency of zero results in $7.76EHz$ for $V_{in} = 2V$ with $I_{load} = 25\mu A$, $329.2MHz$ for $V_{in} = 5V$ with $I_{load} = 25\mu A$, $257.91MHz$ for $V_{in} = 2V$ with $I_{load} = 6.7\mu A$ and $320.47MHz$ for $V_{in} = 5V$ with $I_{load} = 6.7\mu A$. From the AC simulation in the next chapter, we will see that the zeros are placed way beyond the unity gain frequency in all the cases, ensuring the stability of the system.

Table 4.5 summarizes the parameters for the frequency compensation.

Parameter	Value
Compensation Capacitor C_c	$100fF$
Load Capacitor C_L	$1pF$
Zero-nulling resistor R_z	$14.15K\Omega$

Table 4.5: Parameters for frequency compensation

Chapter 5

LDO Regulator Simulation Results

In this section, the whole LDO regulator will be tested and the performance of the regulator will be evaluated.

5.1 Input-output voltage characteristics

The input-output characteristic of the whole LDO regulator was obtained by a DC sweep of the Input voltage from 2V to 5V. The maximum load current $I_{load} = 25\mu A$ was used to verify the dropout voltage value.

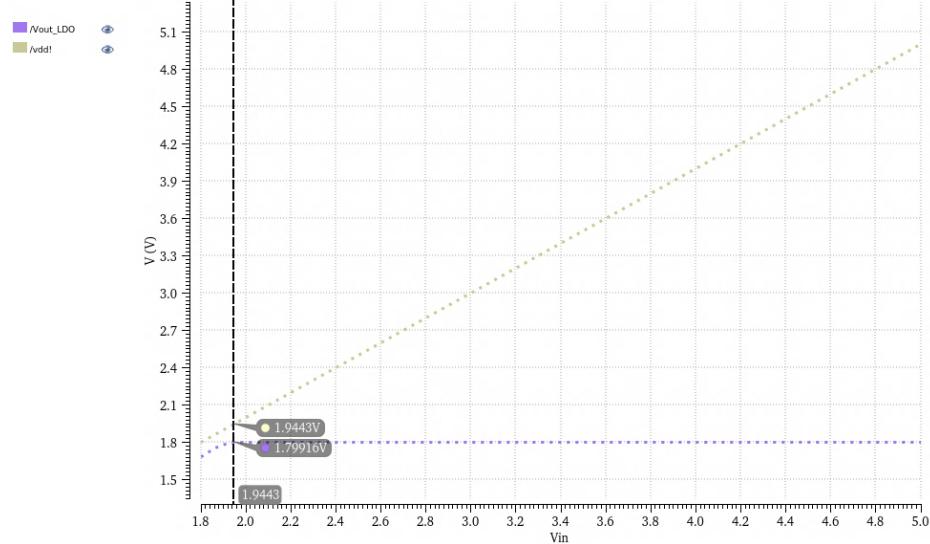


Figure 5.1: Input-output characteristics

It can be observed that the output voltage remains regulated at 1.8V for an input voltage in the range of 1.9443V to 5V. The dropout voltage value obtained from the simulation was 145mV. The Dropout voltage is one of the main parameters in defining the LDO regulator efficiency. Figure 5.1 shows how the regulator ceases to regulate when the input voltage falls below 1.9443V.

5.2 AC Analysis

The open-loop gain and the phase margin were achieved through an AC simulation. As we know from Chapter 3 section 3.1, the closed-loop gain is given by the feedback factor β_{FB} if the open-loop gain is high enough. Therefore, the higher the open-loop gain, the better the regulatory capacity of the LDO regulator will be. Moreover, the unity gain frequency is another important parameter that defines how fast the circuit reacts to changes at the output or input.

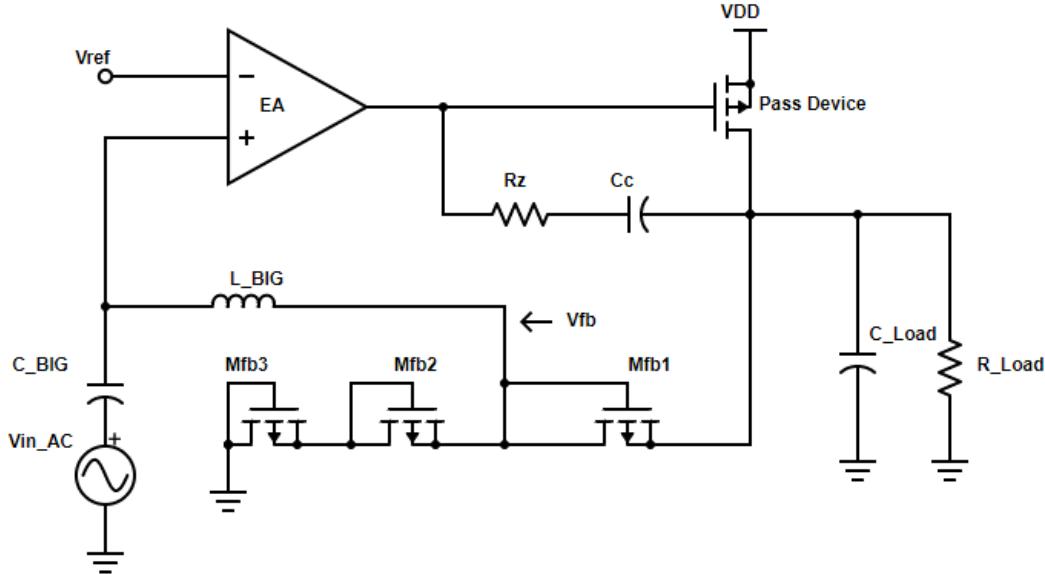


Figure 5.2: AC simulation schematic

Figure 5.2, reproduced from [4] was used as the test bench for the AC simulation. Some extra components such as the AC voltage supply, a capacitor, and an inductor are needed to analyze the open-loop gain and the phase margin. The capacitor serves as DC-decoupling between the V_{INP} node and the AC voltage supply and the inductor serves as a DC coupling and AC-decoupling between the V_{INP} and V_{fb} node. Figures 5.3a and 5.3b show the LDO regulator frequency response at an input voltage of (a) 2V and (b) 5V for $25\mu A$ load current.

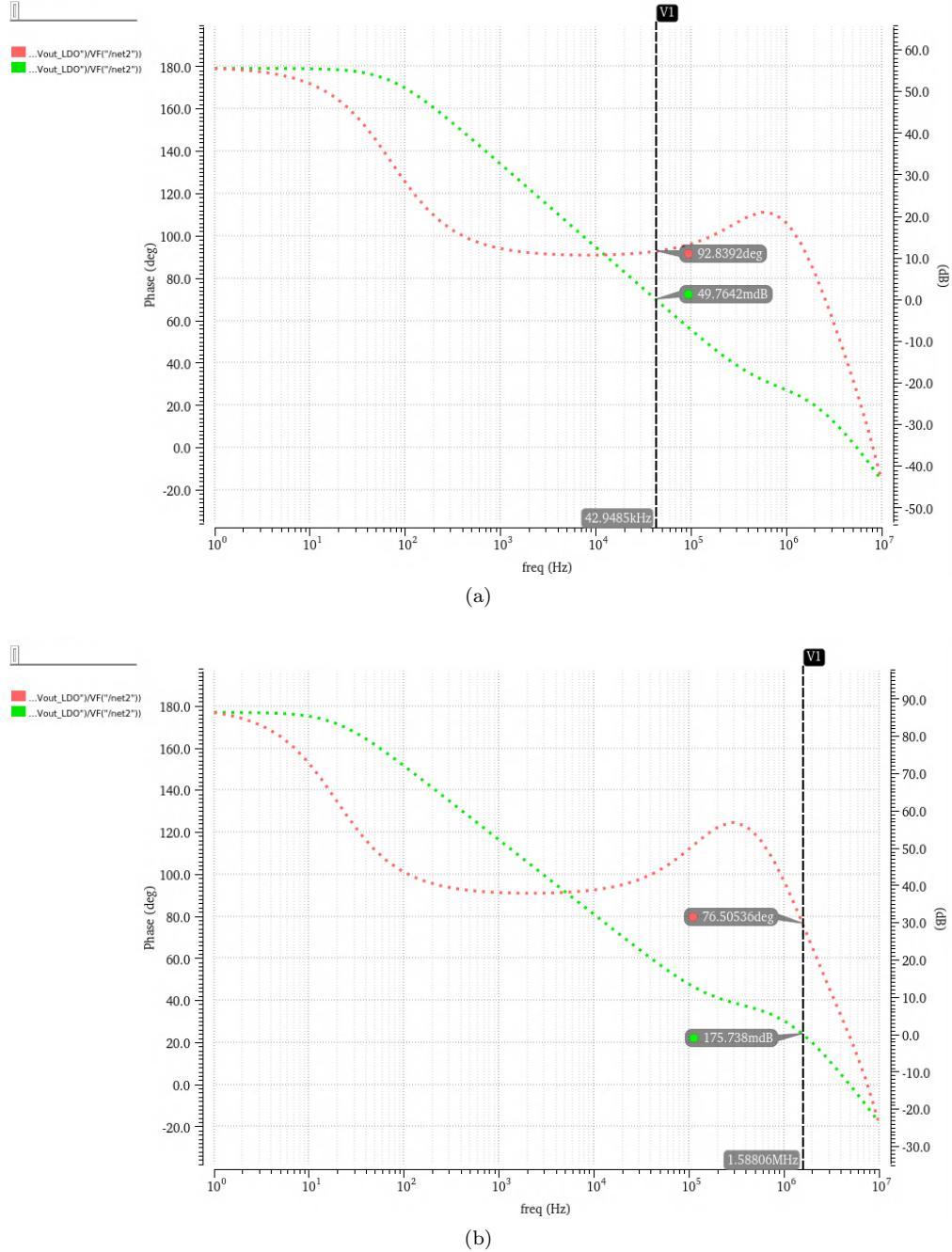


Figure 5.3: LDO regulator frequency response at (a) $V_{in} = 2V$ (b) $V_{in} = 5V$ for $I_{load} = 25\mu A$

Figure 5.4a and 5.4b shows the LDO regulator frequency response at an input voltage of (a) 2V and (b) 5V for $6.7\mu A$ load current

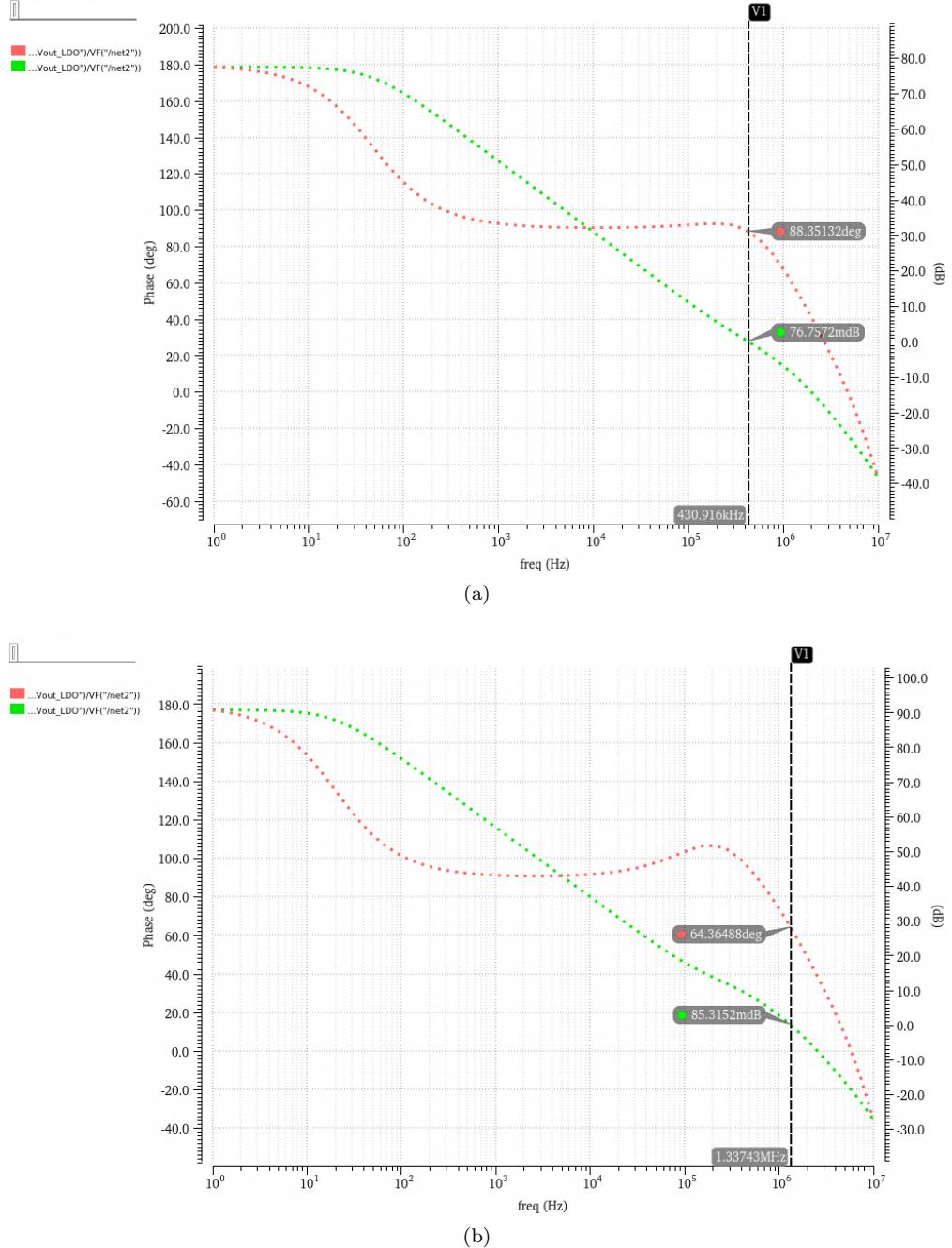


Figure 5.4: LDO regulator frequency response at (a) $V_{in} = 2V$ (b) $V_{in} = 5V$ for $I_{load} = 6.7\mu A$

Parameter	$V_{in} = 2V$		$V_{in} = 5V$	
	$I_{load} = 6.7\mu A$	$I_{load} = 25\mu A$	$I_{load} = 6.7\mu A$	$I_{load} = 25\mu A$
DC gain $A_{DC}(dB)$	77.5	55.5	90.7	86.3
Bandwidth BW (Hz)	18	26	12.8	11.5
Unity gain frequency UGF (Hz)	$430.916k$	$42.94k$	$1.34M$	$1.58M$
Phase margin PM (<i>Degrees</i>)	88.35	92.8	64.36	76.5

Table 5.1: Important parameters from the AC simulation

We can observe the frequency responses for maximum and minimum input voltages from Table 5.1. We can see that the open-loop gain is reduced at the maximum load currents for both the minimum and maximum input voltage of the LDO regulator. For $V_{in} = 2V$ the gain reduces from 77.5dB to 55.5dB for an increase of load current from $6.7\mu A$ to $25\mu A$. For $V_{in} = 5V$, the open-loop DC gain at $6.7\mu A$ load current is 90.7dB and for a load current of $25\mu A$, the gain reduces to 86.3dB. This is because the load current affects the gain-bandwidth of the error amplifier feedback loop [16]. At lower load currents, the output impedance of the pass transistor is high. The LDO regulator output behaves like an ideal current source due to the negative feedback of the control loop. The pole formed by the pass element and the output capacitor occurs at a relatively lower frequency. Whereas, for higher load currents, the LDO regulator output behaves less like an ideal current source. The output impedance of the pass transistor decreases which lowers the gain of the output stage.

The unity gain frequency (UGF) for $V_{in} = 2V$ at $I_{load} = 6.7 \mu A$ is $430.9kHz$ and for $V_{in} = 2V$ at $I_{load} = 25 \mu A$, it is $42.94kHz$. For the maximum supply voltage of this LDO regulator, the unity gain frequency for $I_{load} = 6.7 \mu A$ and $I_{load} = 25 \mu A$ are $1.34MHz$ and $1.58MHz$ respectively. In general, the unity gain frequency depends on the frequency of the output pole [16]. The output stage bandwidth increase as the frequency of the output pole increase. We can see that the unity gain frequency increases with higher input voltages for the same load condition. The worst-case unity gain frequency in the above mentioned cases are for $V_{in} = 2V$ at $I_{load} = 25 \mu A$ as $42.94kHz$. With the maximum input voltage, the UGF for the same load current increases to $1.58MHz$.

The phase margin increases for higher load currents for both the minimum and the maximum input voltages of the LDO regulator. For $V_{in} = 2V$, the phase margin at the minimum load current of $6.7\mu A$ is 88.35° and for the maximum load current of $25\mu A$ defined by the specifications of the LDO regulator, the phase margin is 92.8° . For the maximum input voltage of $5V$, the phase margin at the minimum load current is 64.36° and for $25\mu A$, the phase margin is 76.5° . We can see that the worst-case phase margin in the above mentioned cases is 64.36° . In general, a lower phase margin results in more ringing of the output signal in the transient simulations [3]. However, as the lowest phase margin in this case is above 60° , it will be seen in the transient simulations described in the following sections that the overshoot and ringing in the output signal are in an acceptable range.

5.2.1 Power Supply Rejection

Power Supply Rejection (PSR) defines the regulator's ability to prevent fluctuation of the output voltage due to the changes in the input supply voltage. PSR can be described by the following equation

$$PSR = \frac{V_{out}}{V_{in}} \quad (5.1)$$

Figures 5.5 and 5.6 exhibit the PSR behavior of the designed LDO regulator at $V_{in} = 2V$ and $V_{in} = 5V$ respectively.

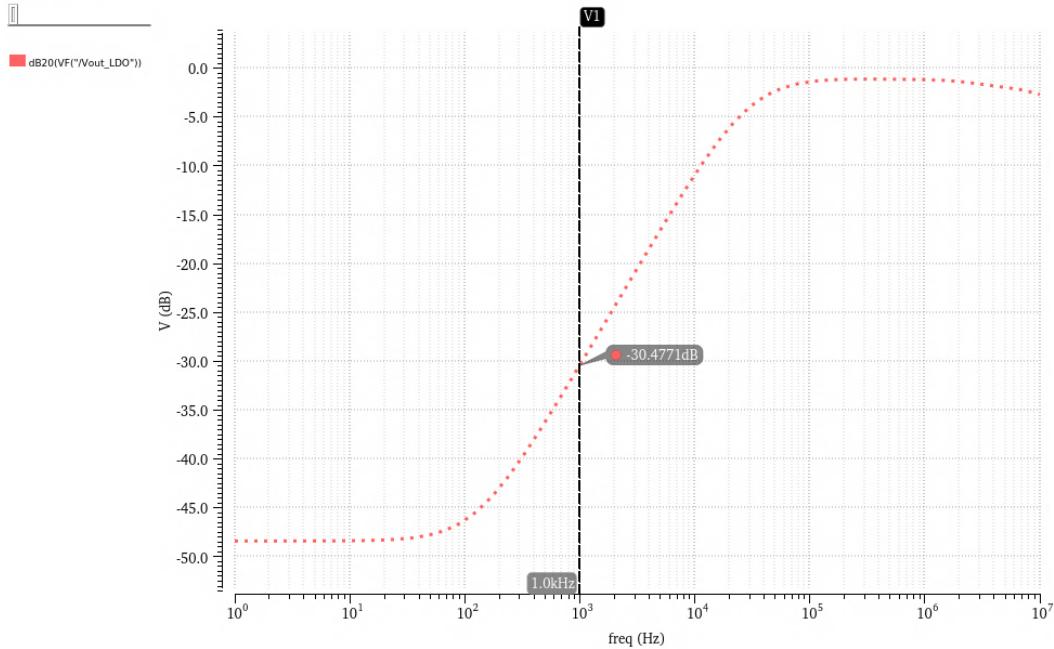


Figure 5.5: LDO regulator Power Supply Rejection at $V_{in} = 2V$

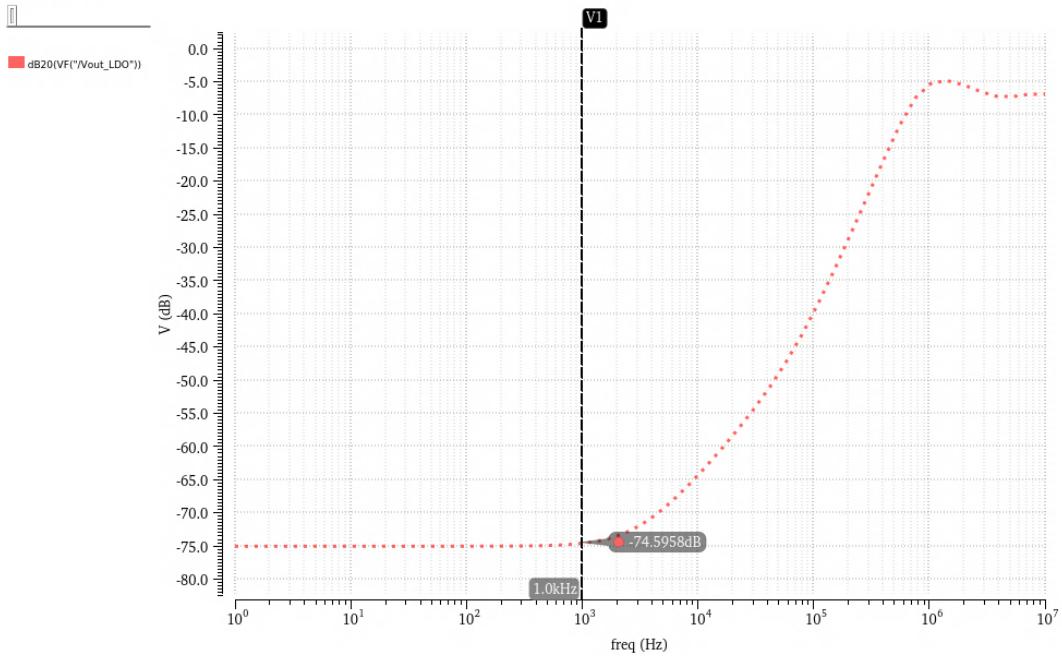


Figure 5.6: LDO regulator Power Supply Rejection at $V_{in} = 5V$

It can be observed that the LDO regulator demonstrates a PSR value of -30.4771dB at 1kHz for $V_{in} = 2V$ for a regulated output voltage of 1.8V . The PSR value increases up to -74.5958dB at 1kHz for the LDO regulator's maximum input voltage of 5V .

5.3 Transient Analysis

Although the open-loop AC and DC response of the system gave satisfying results, they are mostly helpful approximations of the behavior of the circuit. To test how the circuit behaves in real-time with varying signals, a transient simulation is necessary. Two key parameters of the LDO regulator in the transient domain are line and load transient responses. Line transient response is measured as how the LDO regulator output voltage settles with a varying input voltage whereas the load transient response is analyzed as the settling behavior of the output with varying load current.

5.3.1 Line Transient

An important parameter while setting up the line transient simulation was to measure the input signal rise time and fall time. As we know, the input signal of this LDO regulator is the output signal coming out of the supercapacitor bank of the energy management unit. So the worst-case rise time and fall time of the LDO regulator can be estimated by analyzing the rate of change of the charging and discharging voltage of the supercapacitor bank over time.

To calculate the rise time, an ideal 44mF capacitor in series with a 40Ω resistor connected to a 3.3V supply was used as a representation for the supercapacitor bank. We know the capacitor charging equation

$$V_c(t) = V_s[1 - e^{\frac{-t}{\tau}}] \quad (5.2)$$

where $V_c(t)$ is the voltage across the capacitor at a certain time, V_s is the source voltage of 3.3V, and τ the time constant calculated as $\tau = R \times C = 44mF \times 40\Omega = 1.76$ seconds. The capacitors in the supercapacitor bank can be fully discharged before charging. Thus, the capacitors will charge from initial 0V to the maximum supply voltage of 3.3V. The voltage across the capacitor is charged up to 99% of the source voltage when the time taken for charging is roughly 5τ [1]. The voltage across the capacitor after 5τ can be found by equation 5.3 [1]

$$change = (Final - Initial)(1 - \frac{1}{e^{\frac{5\tau}{\tau}}}) \quad (5.3)$$

Where *change* is the capacitor voltage after certain time constant, *Final* is the desired value after charging, which is, in this case 3.3V, *Initial* is the initial voltage of the capacitor 0V, t is time in seconds, τ is the time constant and e is Euler mathematical constant ≈ 2.71828 . Substituting the values in equation 5.3 gives us the capacitor voltage after $t = 5\tau$

$$change = (3.3 - 0)(1 - \frac{1}{e^{\frac{5\tau}{\tau}}}) = 3.2777V \quad (5.4)$$

So we can say that the time it takes for charging from 0V up to 3.3V is approximately $5 \times \tau = 5 \times 1.76 = 8.8$ seconds.

The voltage change over time can be estimated by taking the time derivative of the capacitor charging equation

$$\frac{dV_c(t)}{dt} = \frac{V_s}{\tau} e^{\frac{-t}{\tau}} \quad (5.5)$$

By substituting the known parameters in the equation, the rate of change of the charging voltage over time was found to be 12.63mV/s. As we know, the rate of change of voltage over time is known as the slew rate SR and as the input voltage of the LDO regulator will rise from 2V to 5V, the worst-case rise time can be calculated as

$$t_r = \frac{\Delta V}{SR} = \frac{3V}{12.63mV/s} \approx 237s \quad (5.6)$$

The worst-case fall time of the input signal was calculated in a similar way. In the worst-case scenario, the fastest discharging of the supercapacitor bank was possible when all the capacitors were in series connection. So, the time constant of discharging was calculated by using an equivalent capacitance of 2.75mF, a minimum load resistance of $3.6k\Omega$ and an equivalent series resistance of 160Ω as $\tau = C_{eq}(R_{Load} + 4.R_{ESR}) = 11.66$ seconds [13]. The capacitor discharge equation is

$$V(t) = V_{init} e^{-\frac{t}{\tau}} \quad (5.7)$$

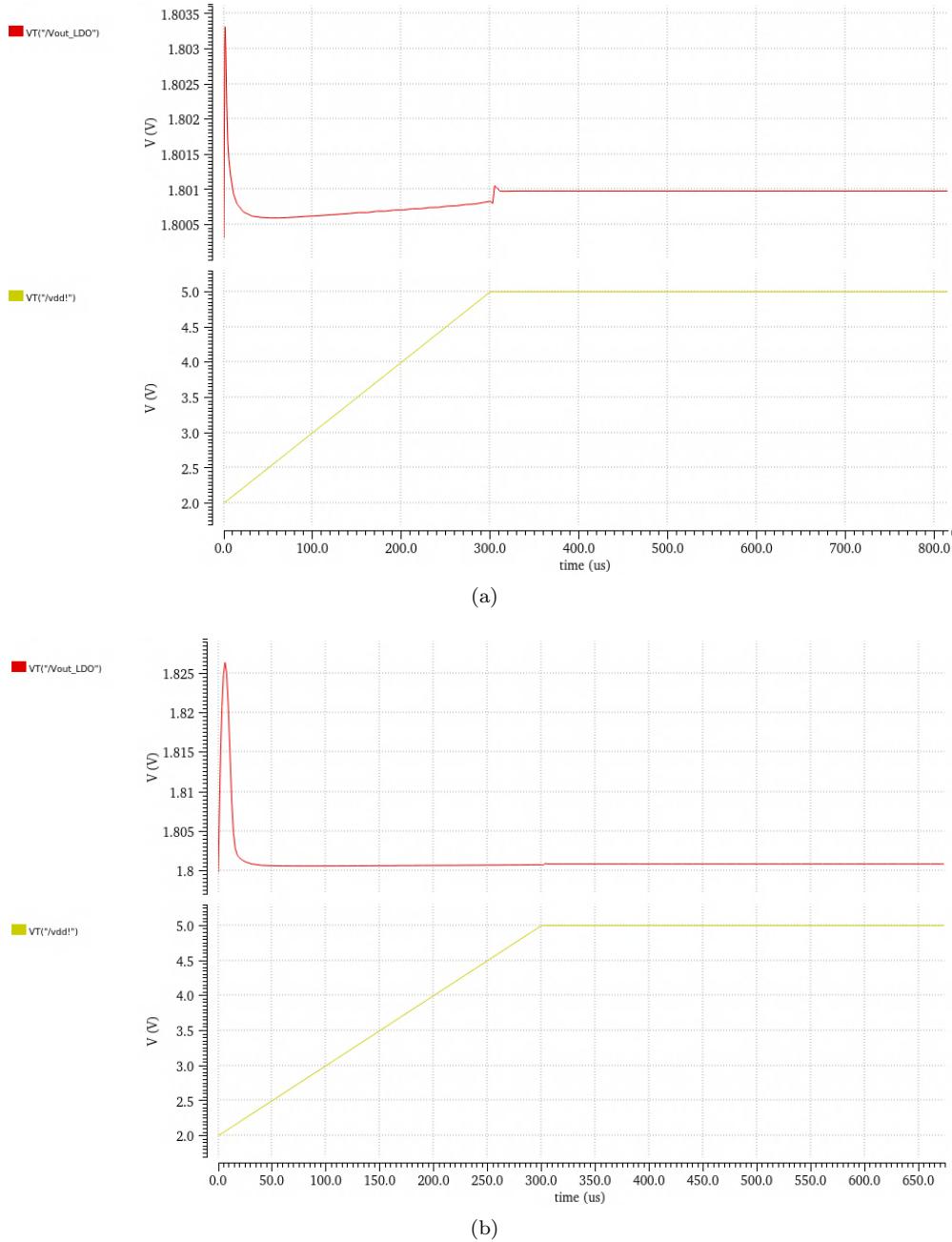
$V(t)$ is the minimum discharge voltage of the capacitor bank of 2V and V_{init} is the maximum voltage the supercapacitors rise to after changing from topology 2 to topology 3 as 5V [13]. Using equation 5.7, the time t for the voltage to reduce from 5V to 2V was found 10.68 seconds. The time derivative of equation 5.7 gives us voltage change over time.

$$\frac{dV}{dt} = -\frac{V_{init}}{\tau} e^{-\frac{t}{\tau}} \quad (5.8)$$

Replacing the known parameters in equation 5.8, the voltage change over time was calculated as -171.58mV/s . Since, the rate of change of voltage over time is known as the slew rate SR and the voltage step of the input signal of the LDO regulator is $5\text{V}-2\text{V}=3\text{V}$, the worst-case fall time was calculated as

$$t_f = \frac{\Delta V}{SR} = \frac{3\text{V}}{171.58\text{mV/s}} \approx 17.48\text{s} \quad (5.9)$$

The calculated rise time and fall time are the worst-case estimated rise time and the worst-case estimated fall time. As we are looking for the sharpest momentarily increase or decrease of the capacitor voltage, the system can be much faster than the values obtained from dividing the voltage range by the voltage change over time. To set up the transient simulation, a pulse signal was used with a rise time and fall time of $300\mu\text{s}$ seconds, which is significantly smaller than the estimated worst-case rise time and the estimated worst-case fall time values. Figures 5.7a and 5.7b show the result of the line transient simulation for the load current of (a) $6.7\ \mu\text{A}$ and (b) $25\ \mu\text{A}$.

Figure 5.7: LDO regulator line transient response at (a) $I_{load} = 6.7\mu A$ (b) $I_{load} = 25\mu A$

It can be observed that for the minimum load current of the LDO regulator, the output signal has an initial overshoot of $3.3mV$ before settling into a stable regulated output voltage. For the maximum load current ($25\mu A$) of the LDO regulator, the output has an initial overshoot of roughly $25mV$ before settling into the regulated output voltage.

The line transient simulation was also performed with a lower input rise time and fall time, in this case 50μ s. The results shown in Figures 5.8a and 5.8b show that the output has an overshoot of roughly $12mV$ when the load current is $6.7\mu A$ and an overshoot of roughly $78mV$ for $I_{load} = 25\mu A$. Comparing the overshoots numbers from the simulation with $t_{rise} = t_{fall} = 300\mu s$, the LDO regulator transient performance is in an acceptable for $50\mu s$ rise time and fall time but exhibits better performance with higher input rise and fall times.

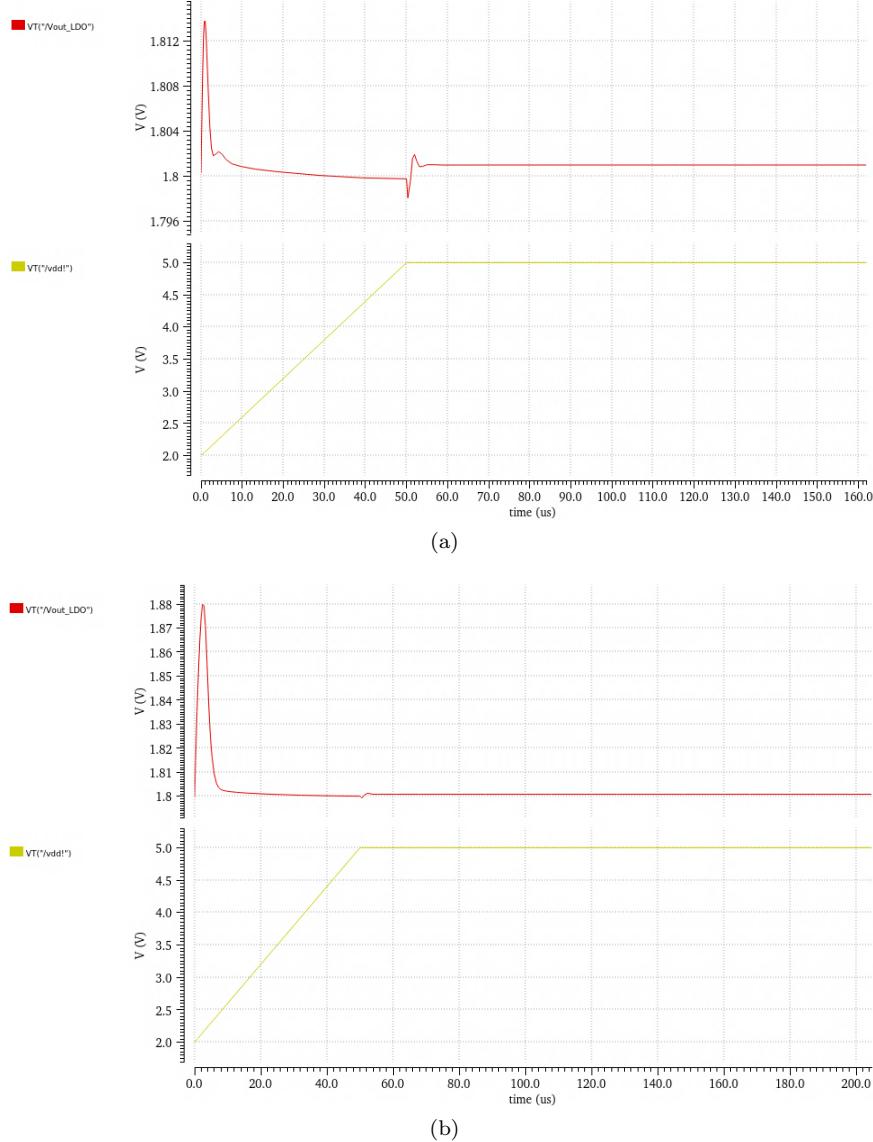


Figure 5.8: LDO regulator line transient response at (a) $I_{load} = 6.7\mu A$ (b) $I_{load} = 25\mu A$ with $t_{rise} = t_{fall} = 50\mu s$

5.3.2 Load Transient

Load transient response is also another important parameter that shows the settling behavior of the output voltage for a varying load current. A pulse generator signal was used for varying the load current from $6.7\mu A$ to $25\mu A$ with the input signal rise and fall time as $60\mu s$. The input rise time and fall time were calculated from the energy management unit [13]. The activation of the comparator is the main reason for a change in the load current in the energy management unit. Thus, it was analyzed how fast the supply current of the comparator increases and decreases when it is turned on and off. For simulation, the isolated comparator circuit of the energy management unit using the same values for the clock signal and the control signal was used [13]. The rise time and fall time of the comparator supply current from a transient simulation was found to be approximately $60\mu s$. Appendix A.3 shows the schematic used for the simulation and Figures 5.9a and 5.9b shows the rise time and fall time of the comparator supply current.

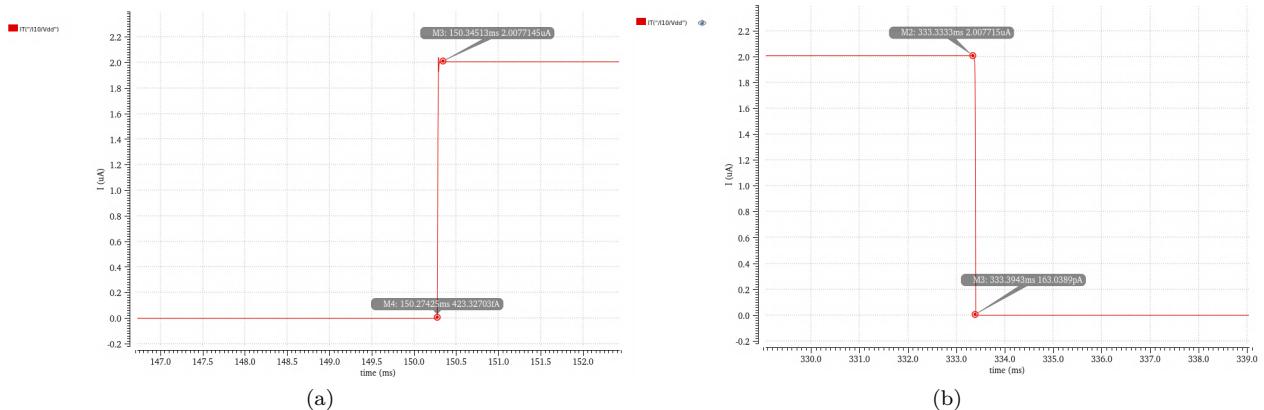


Figure 5.9: Transient response of the comparator supply current from the energy management unit to analyze its (a)rise time (b) fall time

Hence, having an input rise time and fall time of $60\mu s$ for the load transient simulations was inside the boundaries of the energy management unit.

Figures 5.10a and 5.10b represent the results from the load transient simulations of the LDO regulator.

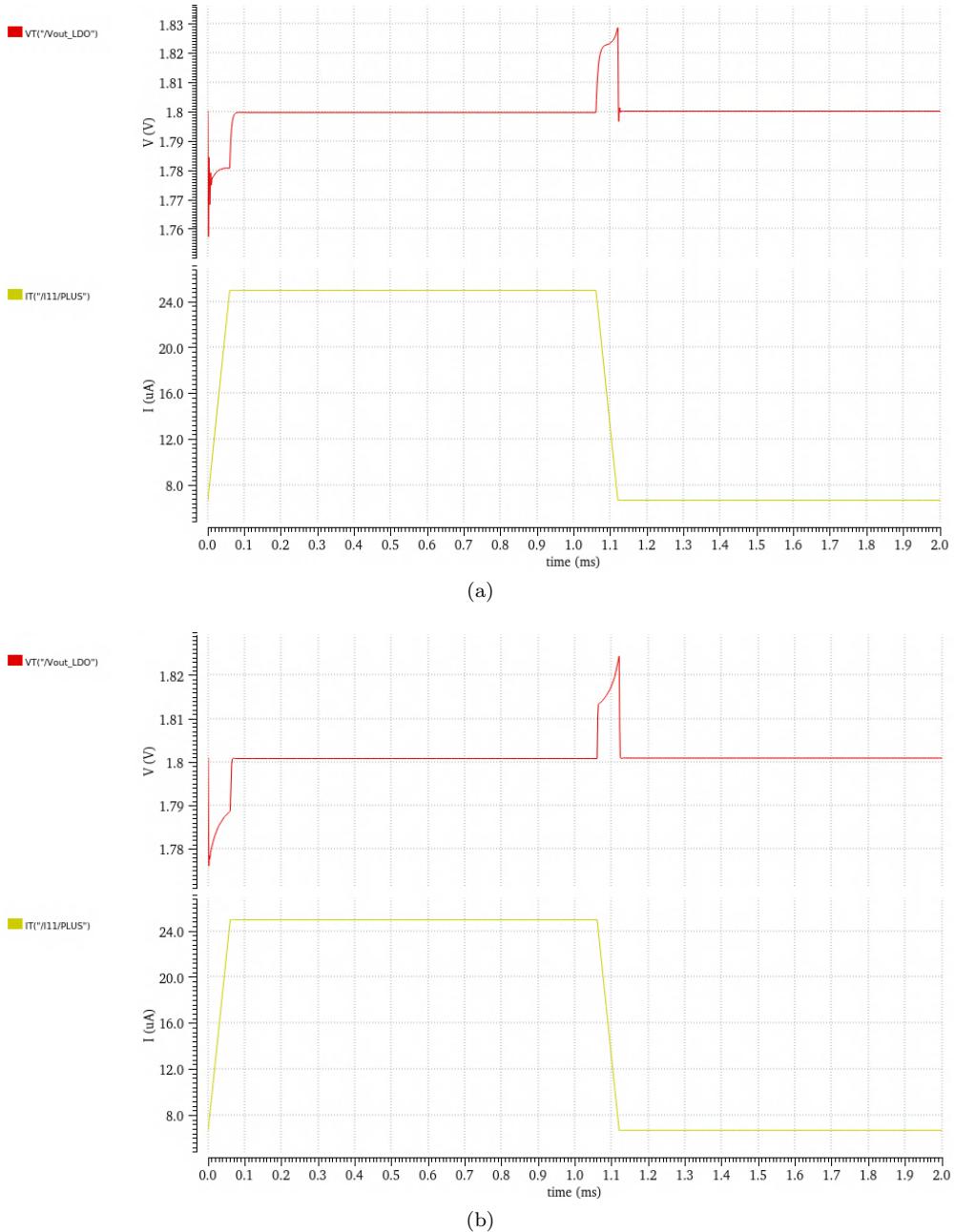


Figure 5.10: Load transient response at (a) $V_{in} = 2V$ (b) $V_{in} = 5V$ for $I_{load} = 6.7\mu A$ to $25\mu A$

It can be observed that the output signal for $V_{in} = 2V$ has a maximum overshoot of roughly 28mV and a maximum undershoot of approximately 43mV. The signal settles down within the rise time of the input signal. Similarly, for $V_{in} = 5V$, maximum overshoot and undershoot are roughly 24mV and 23.9mV respectively. The output signal in this case also settles into a regulated voltage within the rise and fall time of the input signal.

5.4 Transient behavior under process variation

Another important parameter for the characterization of the LDO regulator performance is verifying it under process variations. The process corners typical (normal NMOS and normal PMOS), worst power WP (fast NMOS and fast PMOS), and worst speed WS (slow NMOS and slow PMOS) were taken as simulation parameters to verify the LDO regulator transient performance. The simulations were performed for both $V_{in} = 2V$ and $V_{in} = 5V$ from I_{load} varying from the minimum load current defined by the energy management unit [13] of $6.7\mu A$ to the maximum load current of $25\mu A$ and are displayed in Figures 5.11a to 5.11f.

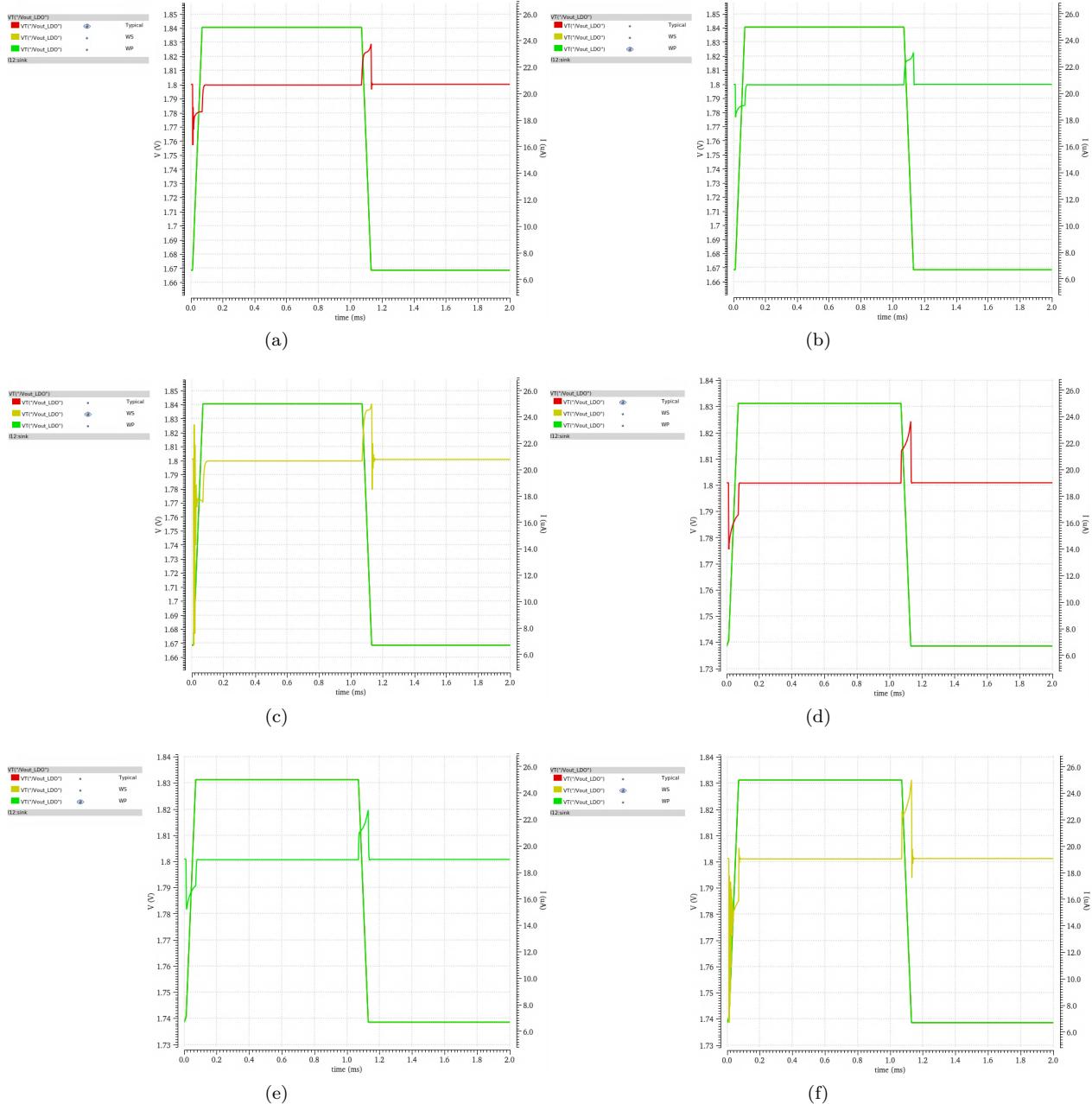


Figure 5.11: LDO regulator performance at $V_{in} = 2V$, (a) Typical corner (b) Worst power corner (c) Worst speed corner, $V_{in} = 5V$, (d) Typical corner (e) Worst power corner (f) Worst speed corner for $I_{load} = 6.7\mu A$ to $25\mu A$

The results show that the LDO regulator transient performance doesn't seem to be affected by the process variations. The only case of concern could be the worst speed WS (slow NMOS and slow PMOS) corner which exhibits the largest undershoot, overshoot, and ringing from low to high and high to low current transitions.

Table 5.2 shows the maximum overshoot and undershoot for all the corners

Parameter	$V_{in} = 2V$		$V_{in} = 5V$	
	undershoot(mV)	overshoot(mV)	undershoot(mV)	overshoot(mV)
Typical corner	43	29	23.9	24.4
Worst power corner	23	22.8	18.3	20
Worst speed corner	125.5	40.8	63.2	31.7

Table 5.2: Maximum undershoot and overshoot for process corner simulations

5.5 Transient behavior under temperature variation

The LDO regulator performance was also tested under varying temperatures. Temperatures of $-40^{\circ}C$, $0^{\circ}C$, $60^{\circ}C$ and $120^{\circ}C$ were taken into consideration. The simulations were performed for both $V_{in} = 2V$ and $V_{in} = 5V$ from I_{load} varying from $6.7\mu A$ to $25\mu A$ and are displayed in Figures 5.12a to 5.13d.

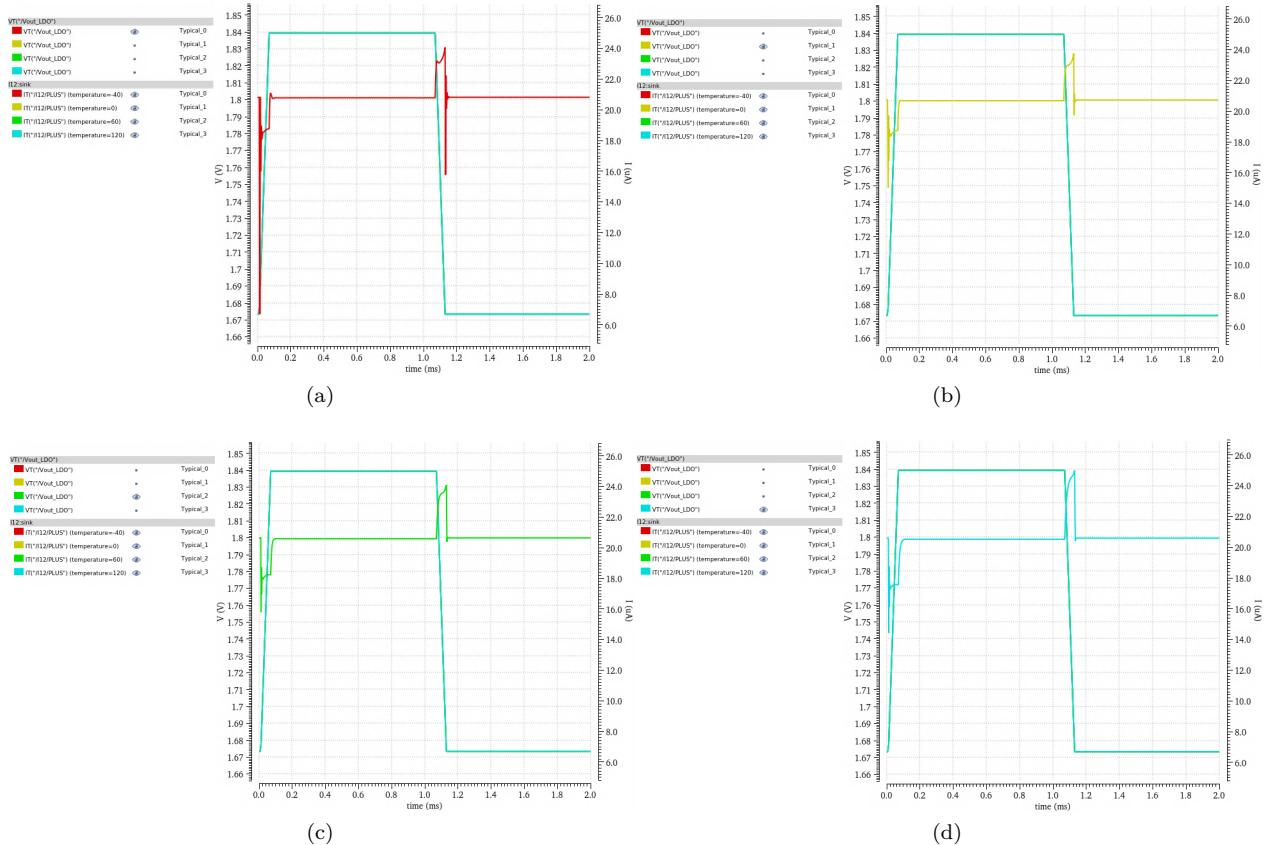


Figure 5.12: LDO regulator performance at $V_{in} = 2V$ for (a) $-40^{\circ}C$ (b) $0^{\circ}C$ (c) $60^{\circ}C$ (d) $120^{\circ}C$ at $I_{load} = 6.7\mu A$ to $25\mu A$

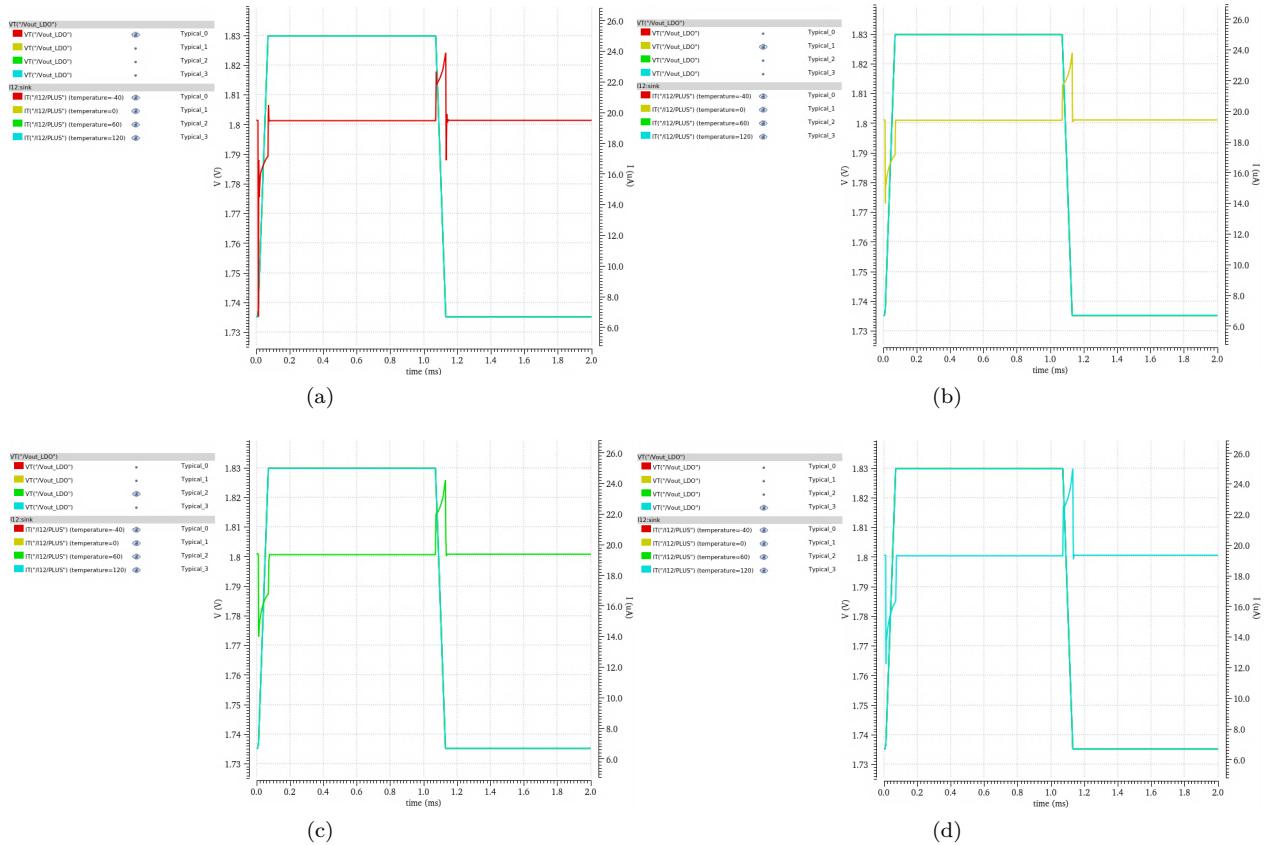


Figure 5.13: LDO regulator performance at $V_{in} = 5V$ for (a) $-40^{\circ}C$ (b) $0^{\circ}C$ (c) $60^{\circ}C$ (d) $120^{\circ}C$ at I_{load} = $6.7\mu A$ to $25\mu A$

It can be observed that the LDO regulator performance does not seem to be affected by different temperatures at varying load current conditions. The regulator experiences maximum undershoot in $-40^{\circ}C$ temperature and maximum overshoot under $120^{\circ}C$ temperature corner. Table 5.3 shows the maximum overshoot and undershoot for all the temperatures.

Parameter	$V_{in} = 2V$		$V_{in} = 5V$	
	undershoot(mV)	overshoot(mV)	undershoot(mV)	overshoot(mV)
$-40^{\circ}C$	130	30	65	25
$0^{\circ}C$	50	28	30	23
$60^{\circ}C$	45	30	30	26
$120^{\circ}C$	58	40	40	30

Table 5.3: Maximum undershoot and overshoot for transient simulations under varying temperature

5.6 Line and Load Regulation

Figure 5.14 illustrates line regulation. It is defined as the output voltage change in response to a change in the input voltage at a fixed load current. It is commonly tested under maximum load current. in this case, $25\mu A$. As we know

$$LNR = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (5.10)$$

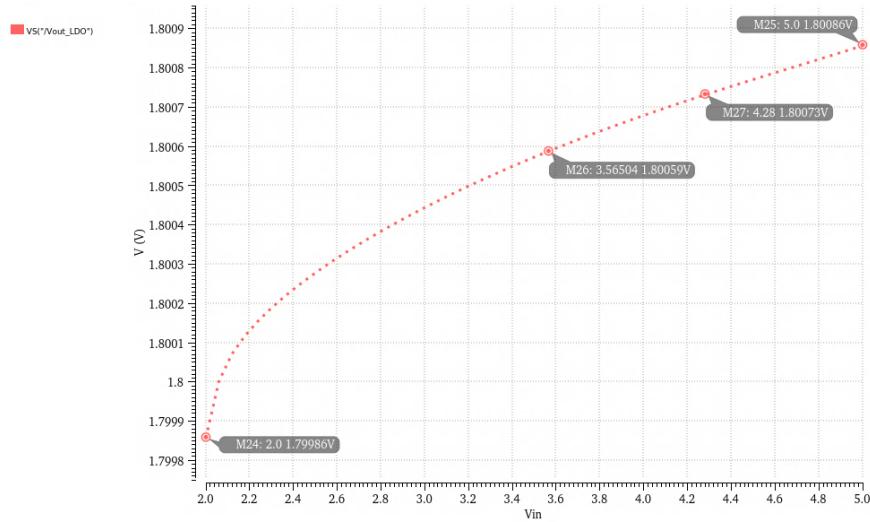


Figure 5.14: LDO regulator line regulation

Solving equation 5.10 gives the line regulation value as $0.33mV/V$ for $V_{out} = 1.8V$ and a constant load current of $25\mu A$. The value was obtained through dividing the difference between the maximum and minimum point of the output voltage by the difference between the maximum and minimum point of the input voltage. The line regulation at the point of the maximum slope is calculated as $0.20mV/V$.

Load regulation is defined as the rate of change of the output voltage in response to a change in the load current, at a constant input voltage.

$$LDR = \frac{\Delta V_{out}}{\Delta I_{load}} \quad (5.11)$$

Figure 5.15a and 5.15b represents load regulation for $V_{in} = 2V$ and $V_{in} = 5V$. The load current is varied from 0 to the maximum load current of $25\mu A$. Solving equation 5.11 with values from the curves gives a load regulation value of $0.05mV/\mu A$ for $V_{in} = 2V$ and $0.02mV/\mu A$ for $V_{in} = 5V$. These values were also obtained through diving the difference between the maximum and the minimum point of the output voltage by the difference between the maximum and minimum point of the load current in the plot. However, the load regulation was also analyzed at the point of the maximum slope and was calculated as $0.026mV/\mu A$ for $V_{in} = 2V$ and $4.78\mu V/\mu A$ for $V_{in} = 5V$.

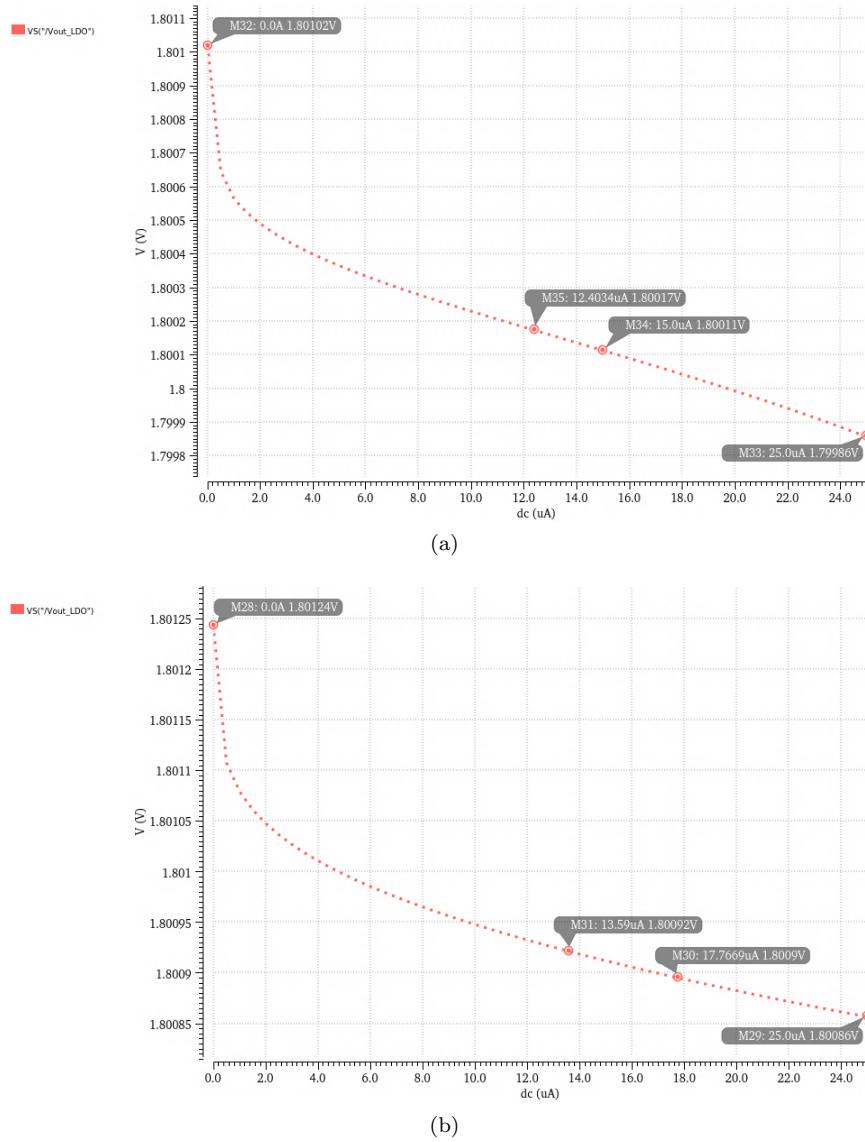


Figure 5.15: LDO regulator load regulation at (a) $V_{in} = 2V$ (b) $V_{in} = 5V$ for $I_{load} = 0$ to $25\mu A$

5.7 Efficiency

As discussed in Chapter 2, efficiency is an important parameter in the LDO regulator characterization. As we know the equation of current efficiency,

$$\eta_I = \frac{I_{load}}{I_{in}} = \frac{I_{load}}{I_{load} + I_Q} \quad (5.12)$$

As we know, the quiescent current can be defined as the current consumption of the LDO regulator's internal circuitry when the external load current is zero [16]. The current consumption of each block of the LDO

regulator under zero load condition can be observed in Table 5.4 and is shown in appendix A.5.

Parameter	Error Amplifier	Pass Transistor	Feedback Network	Total Consumption
I_Q	$3.1799\mu A$	$13.1nA$	$13.11nA$	$3.2\mu A$

Table 5.4: LDO Regulator total current consumption

Replacing $I_{load} = 25\mu A$ and $I_Q = 3.2\mu A$, the current efficiency of the designed LDO regulator results in 88.65%.

With a lower quiescent current, the LDO regulator efficiency will be maximized. As we know from the efficiency equation

$$\eta = \frac{V_{in} - V_{DO}}{V_{in}} * \eta_I = [1 - \frac{V_{DO}}{V_{in}}]\eta_I \quad (5.13)$$

substituting the values as $V_{in} = 2V$ and $V_{DO} = 145mV$ results in the LDO regulator efficiency of 82.22%.

The efficiency calculated above represents the best case scenario for the power efficiency with a load current of $25\mu A$. This $25\mu A$ load current is the maximum load current during the active stage operation of the energy management unit. It is also better to analyze the regulator efficiency with the load current calculated for the inactive stage of the energy management unit. The inactive stage load current is defined by the current consumption of the system when only the digital control unit and the counter are active and was calculated as $6.7\mu A$. Using $I_{load} = 6.7\mu A$ in equation 5.12, the current efficiency results in

$$\eta_I = \frac{6.7\mu A}{(6.7 + 3.2)\mu A} = 67.67\% \quad (5.14)$$

Substituting the current efficiency value in equation 5.13 results in a power efficiency of 62.76%.

Chapter 6

Conclusion

In this project work, a low power low dropout regulator was designed in X-fab 180nm XH018 technology for the energy management unit of an electronically instrumented osteosynthesis implant, developed at the Institute for Integrated Circuits, TUHH. The LDO regulator has to provide a 1.8V supply voltage for most of the components of the energy management unit. A low power regulator is required because of its continuous operation so the energy management unit doesn't consume more energy than it provides. Several parameters were taken into consideration during the design, but the main design considerations were the input voltage of the LDO, which is the output voltage coming out of the supercapacitor bank of the energy management unit and in the range of 2V to maximum 5V, a regulated output voltage of 1.8V and maximum load current of $25\mu A$. Firstly, the typical parameters of the LDO regulator and how they're interpreted and measured were discussed. In the LDO Regulator Components Design chapter, all the calculations of the LDO regulator components were thoroughly discussed. A PMOS transistor was chosen as the pass device due to its low dropout voltage feature. A two-stage operational amplifier was chosen as the error amplifier. The amplifier was designed with an NMOS input differential stage keeping the input transistors in sub-threshold and all the other transistors in saturation. The feedback network was composed of diode-connected PMOS transistors with a voltage divider ratio of 2:1. The LDO regulator was tested in the Cadence design environment. The simulation results showed a constant 1.8V output voltage over a 2V to 5V input voltage range. The dropout voltage of the LDO regulator was 145mV. The efficiency of the LDO regulator with maximum load current was calculated as 82.22%.

There is room for improvement in the LDO regulator. Instead of a constant voltage source, a voltage reference circuit can be used at the negative input terminal of the error amplifier. As it was seen in the AC simulation, the open-loop gain was lesser at maximum load current than the gain resulting in minimum load current for the same input voltage. To rectify this, the common source PMOS transistor at the output stage of the error amplifier could be biased in the triode region. When the load current increases, the source-gate voltage of the pass transistor which is connected at the output of the error amplifier will increase. Thus, the output voltage of the error amplifier will reduce and the common source PMOS transistor at the error amplifier output stage will enter into saturation region. Therefore, the open-loop gain for higher load current would increase.

Moreover, if the miller capacitor value for the frequency compensation is too large; a current amplifier could be used as a capacitance multiplier [15]. The capacitor would react to changes in the output voltage due to changes in the load current, resulting in generating an equivalent current change flowing through the capacitor. The generated current would then be injected into the gate capacitance of the pass transistor. This approach allows using a small capacitor value and saves chip area. Table 6.1 shows the specification defined by the energy management unit and the final results from the simulation of the designed LDO regulator.

Parameter	Specification	Nominal results
V_{out}	1.8V	1.8V
V_{DO}	< 0.2V	145mV
I_Q	-	$3.2\mu A$
Gain (worst case)	-	55.5dB
Unity Gain Frequency (worst case)	-	$42.94kHz$
Phase Margin (worst case)	$>45^\circ$	64.36°
Efficiency (with the maximum load current)	-	82.22%

Table 6.1: Comparison between specification and final result of the designed LDO regulator

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Appendix A

Appendix

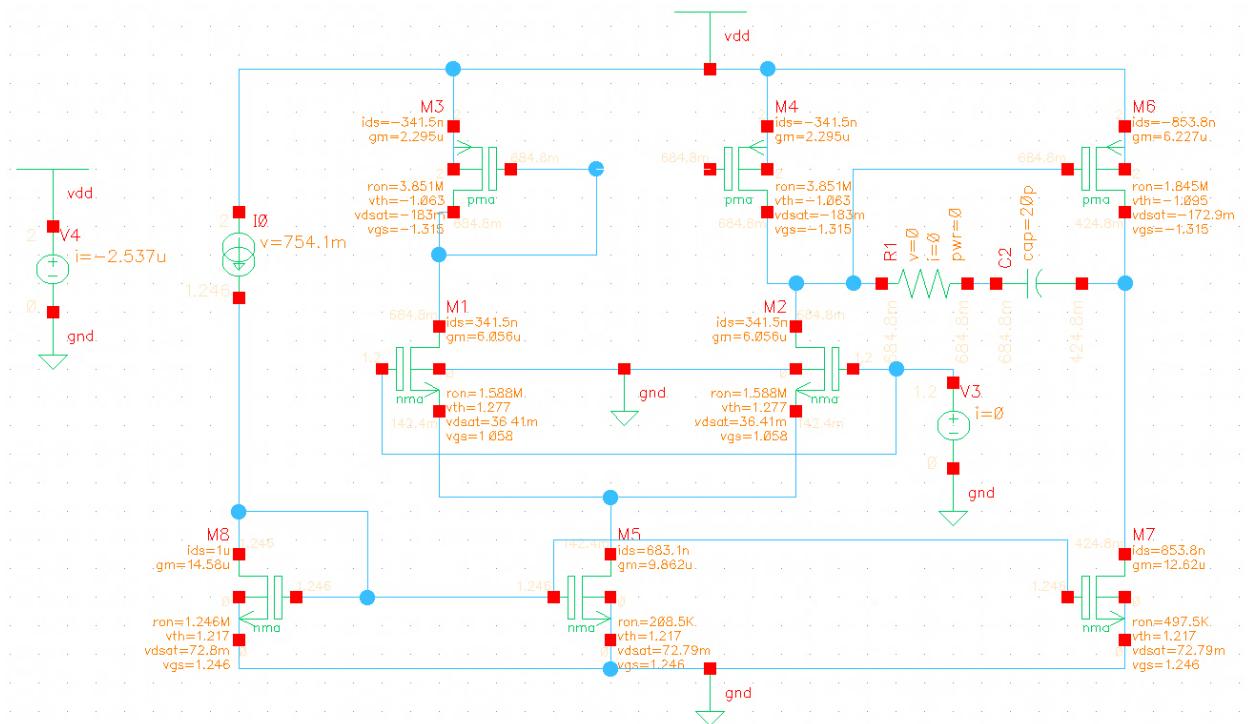


Figure A.1: Schematic and the dc operating points of the Error Amplifier with $1\mu\text{A}$ bias current

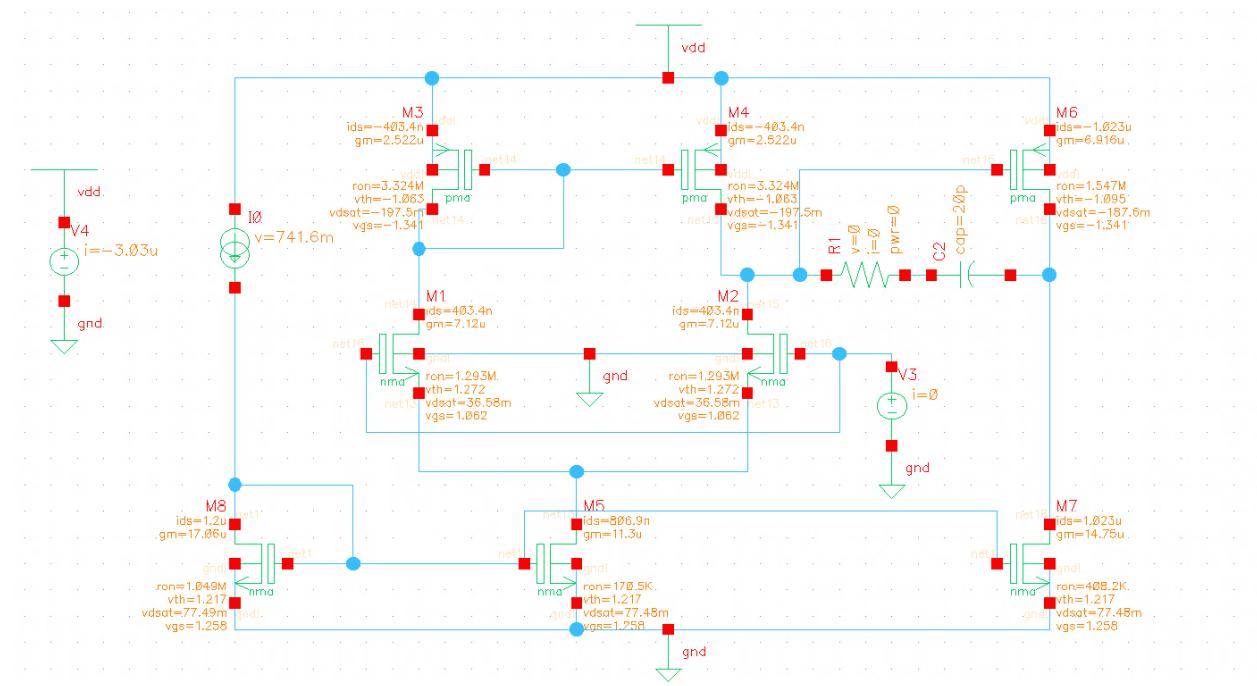


Figure A.2: Schematic and the dc operating points of the Error Amplifier with $1.2\mu\text{A}$ bias current

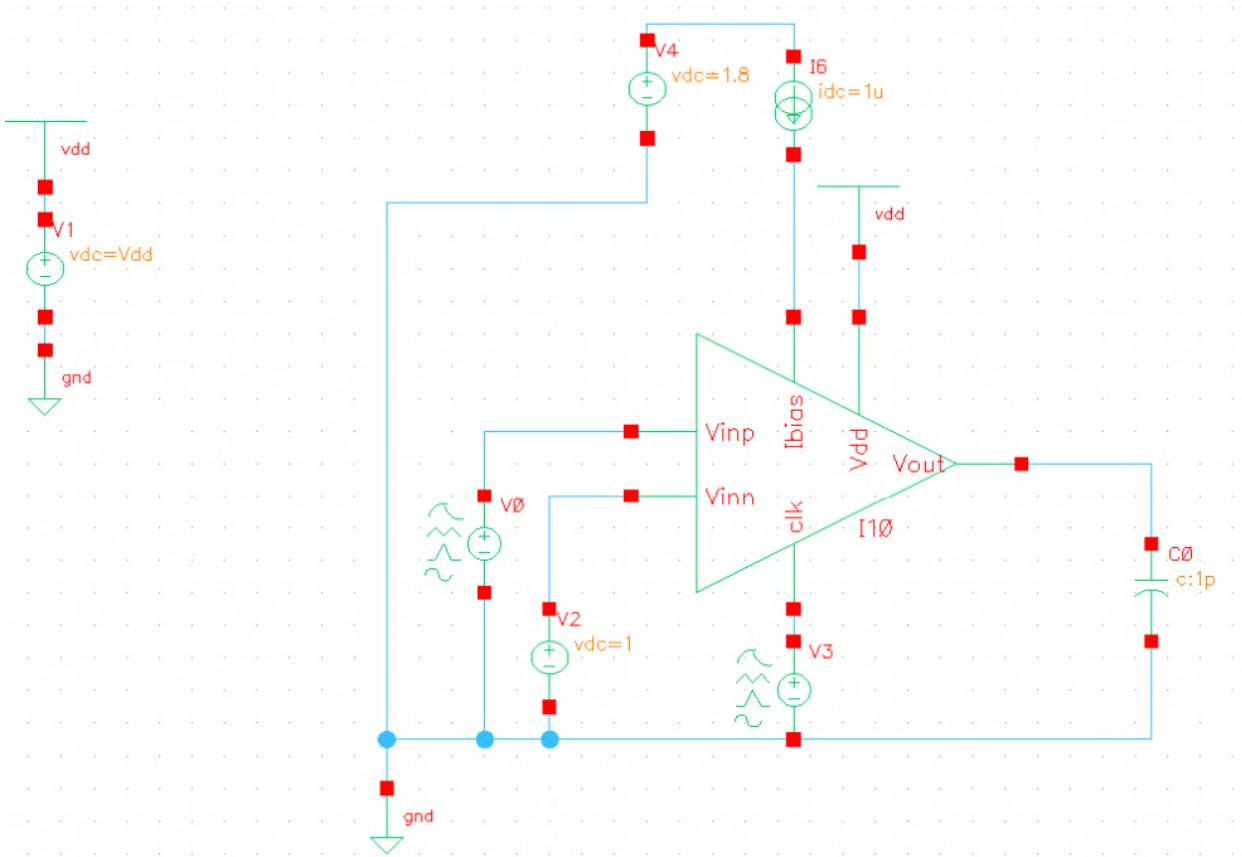


Figure A.3: Transient simulation schematic of the isolated comparator from the energy management unit

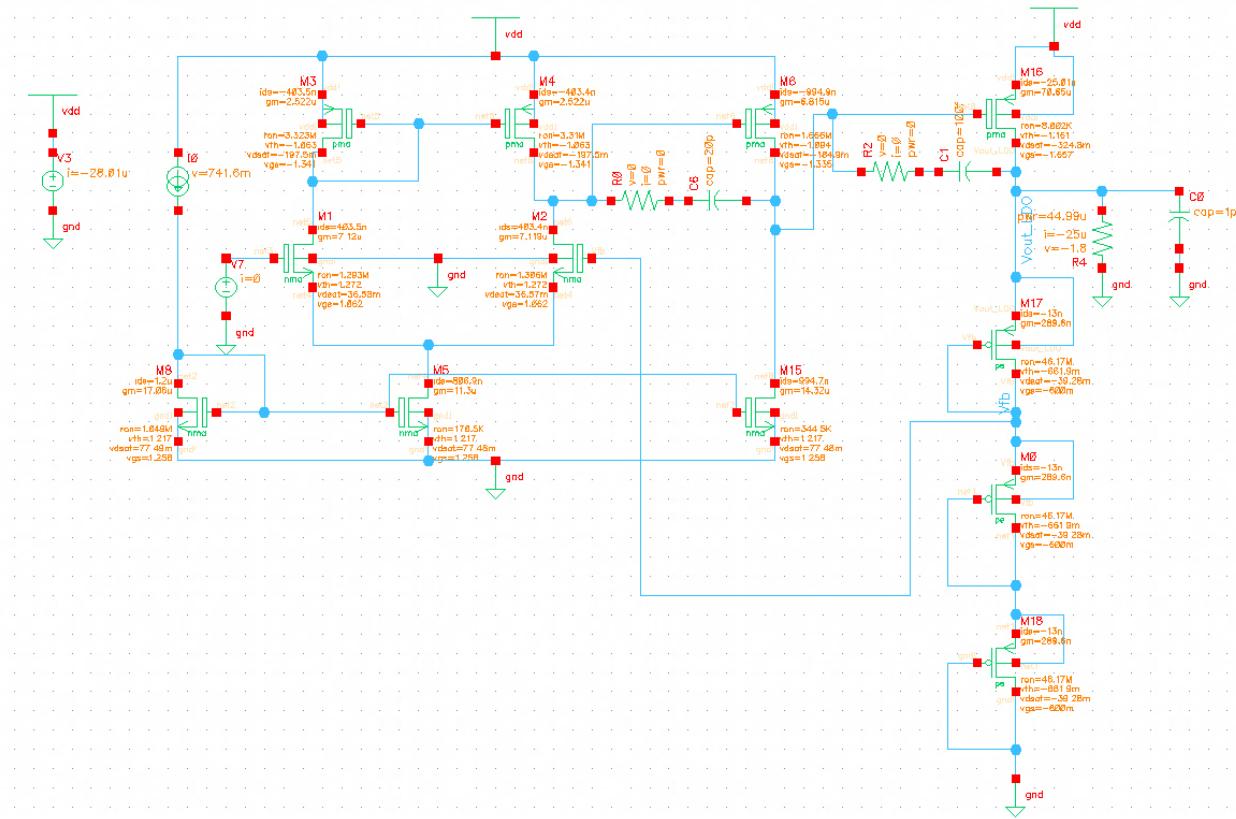


Figure A.4: Schematic of the designed LDO Regulator

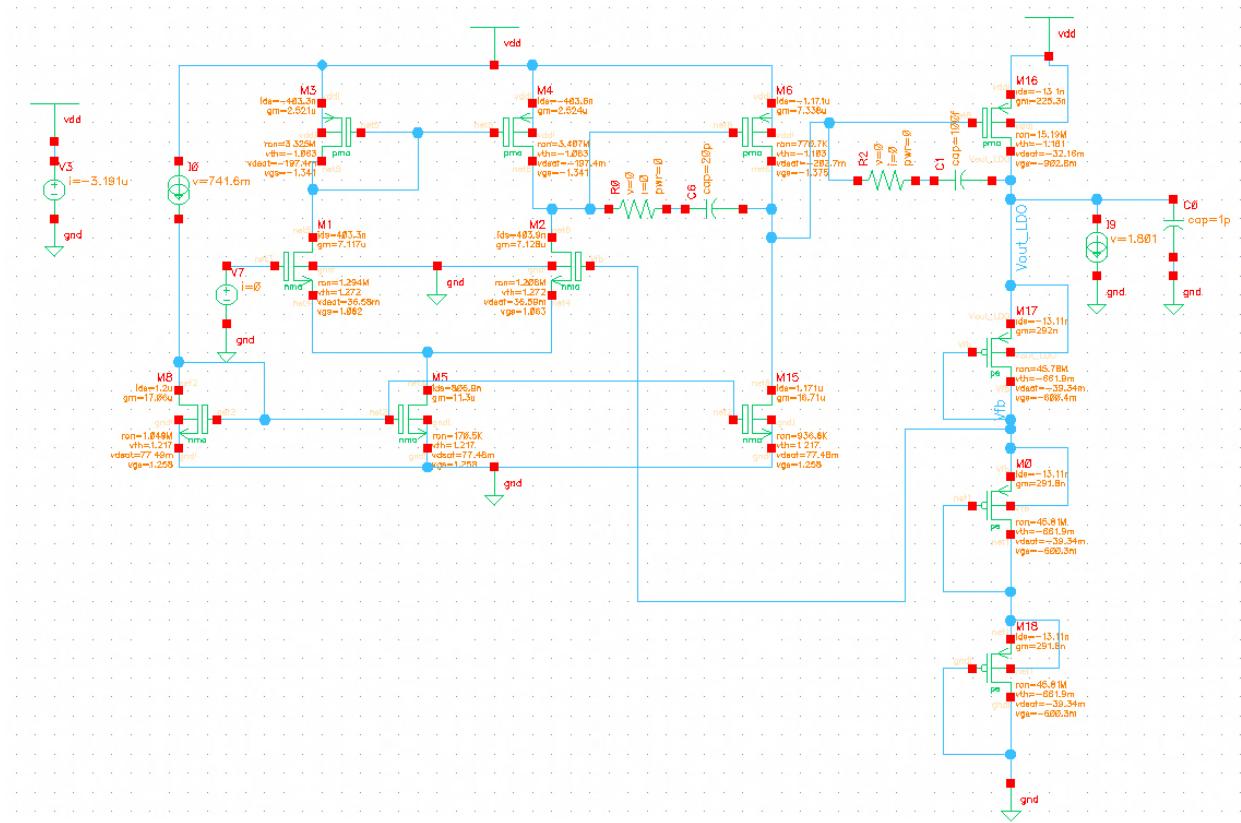


Figure A.5: LDO regulator dc operating points at zero load current