Layout plan of a Lateral BJT Input Stage Folded Cascode Amplifier

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Transistors	Width(W)	Length(L)	Multiplier	W_total
M0,M5	12.5µm	350nm	16	200µm
M15,M16	5.5µm	1µm	6	33µm
M17	5.5µm	1µm	8	44µm
M13,M11	5.5µm	1µm	15	80µm
M14,M12	5.5µm	1µm	15	80µm
M10,M6,M7	2.5µm	1µm	12	30µm
M18,M8,M9	2.5µm	1µm	12	30µm

Table: Dividing the transistors into multipliers for layout

Matched Trasistors	Multiplier Ratio	Matching Technique	Matching Pattern
M15,M16,M17	6:6:8	Common-Centroid	AAACCCCBBB BBBCCCCAAA
M13,M11	16:16	Common-Centroid	ABBAABBA BAABBAAB BAABBAAB ABBAABBA
M14,M12	16:16	Common-Centroid	Same as M13,M11
M10, M6,M7	12:12:12	Common-Centroid	ABCCBAABC CBAABCCBA CBAABCCBA ABCCBAABC
M18, M8,M9	12:12:12	Common-Centroid	Same as M10, M6,M7

Table: Matching technique and pattern for the layout

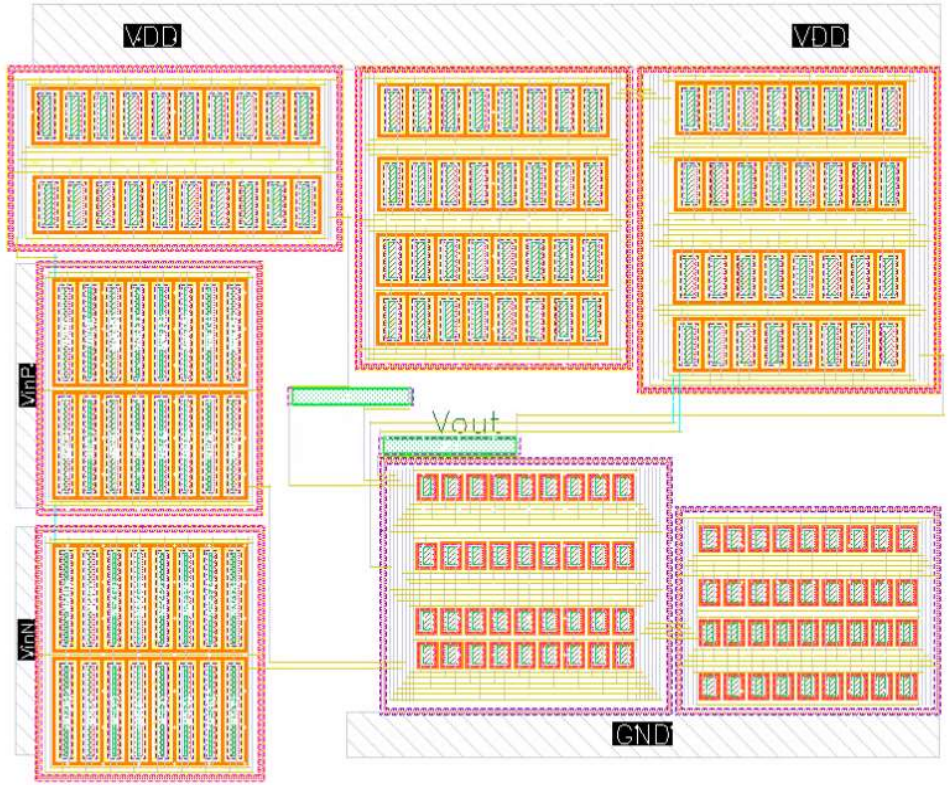

Figure: Layout of the lateral bjt-input folded cascode amplifier

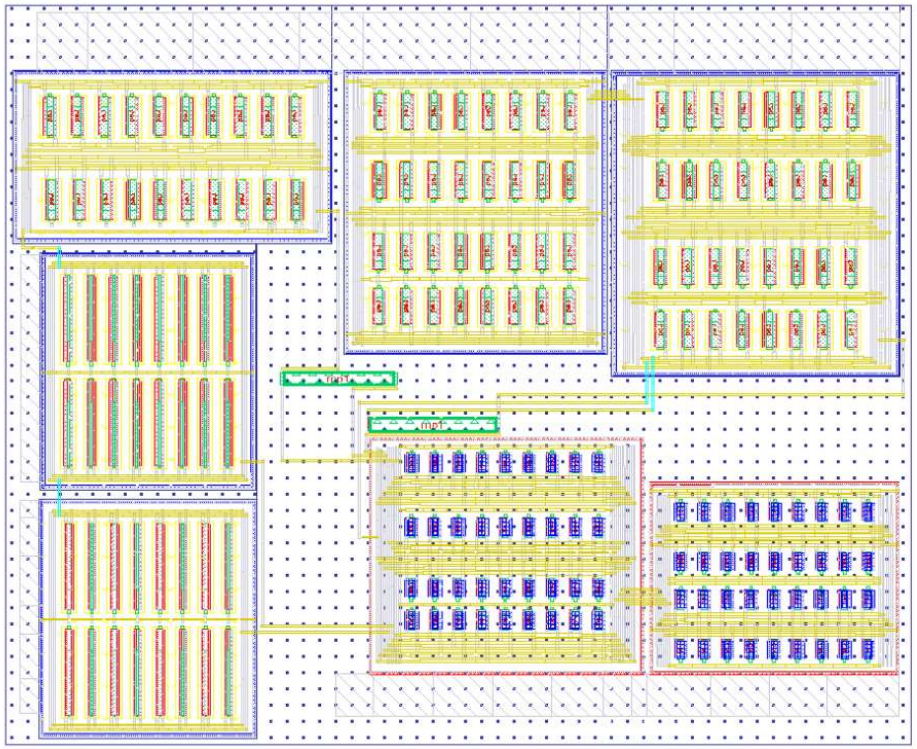

Figure: Parasitic extracted view of the layout

Thank You