Investigation of CMOS Amplifiers for Low-Noise Application

M K Akif Alvi Arnab

Examiner : Prof. Dr.-Ing. Andreas Bahr

Supervisor: Ing. Johan Arbustini, M.Sc.

Magneto-Electric Sensor and Amplifier Design Specifications

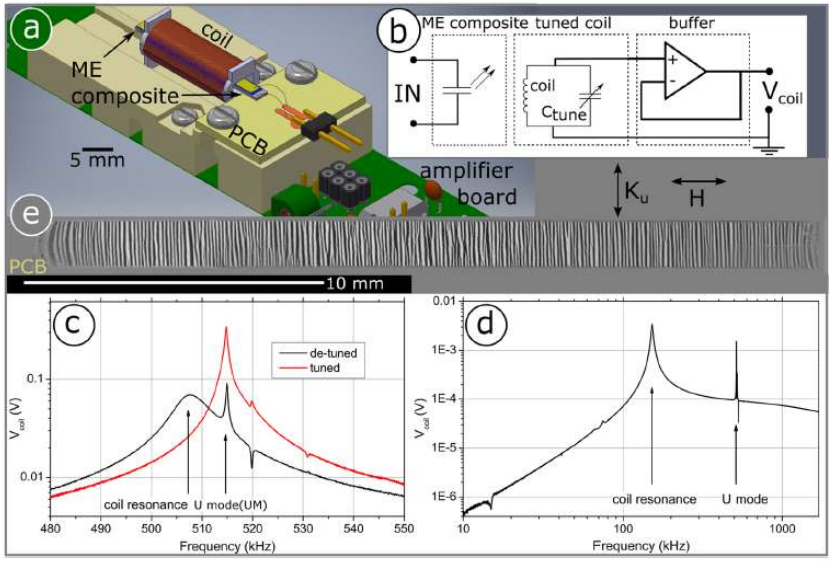


Figure: Sensor setup and tuning

Parameter	Value
VDD	3.3V
Gain (single stage amplifiers)	20dB
Gain (Differential, 2-stage and folded cascode amplifiers)	50dB
Gain-bandwidth (single stage amplifiers)	25MHz
Gain-bandwidth ((Differential, 2-stage and folded cascode amplifiers)	70MHz
C_{Load}	1pF
Frequency of interest	500KHz

Table : Amplifier design specifications

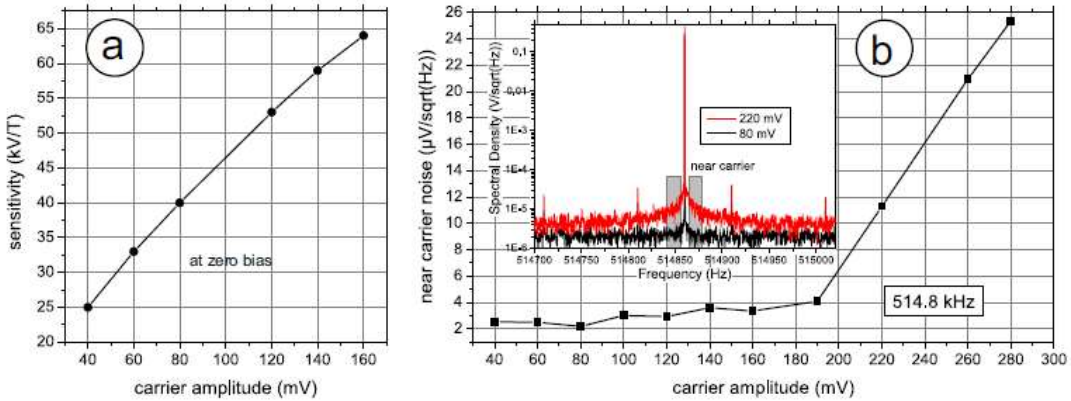


Figure: Sensor sensitivity and noise dependency on the applied carrier amplitude

Amplifier	**Ibias (µA)**	Gain (dB)	PM (◦)	GBW (MHz)	IRN (V /√Hz)
Common-Source Amplifier	1	20	89.7	25.36	108.147n
Common-Source Cascode Amplifier	5	26.8	87.5	25.33	87.233n
Common-Gate Amplifier	3.58	29	92.12	25.22	113.2364n
Common-Drain Amplifier	1	-	-	-	1.30629µ
Common-Bulk Amplifier	R=920KΩ	-	-	-	603.805n

Table: Summary of the designed basic single stage amplifiers

Common-Source Amplifier with cascode PMOS Current Source Load

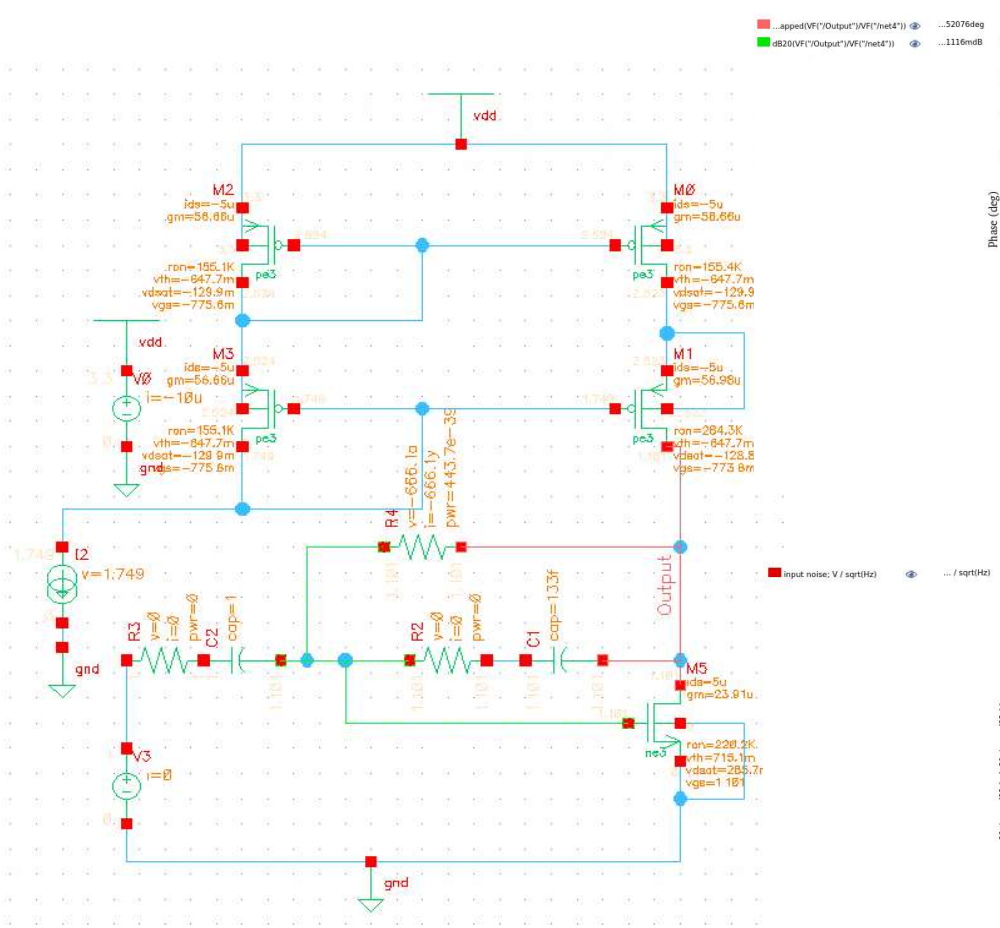


Figure : Schematic of the common-source amplifier with cascode PMOS current source load

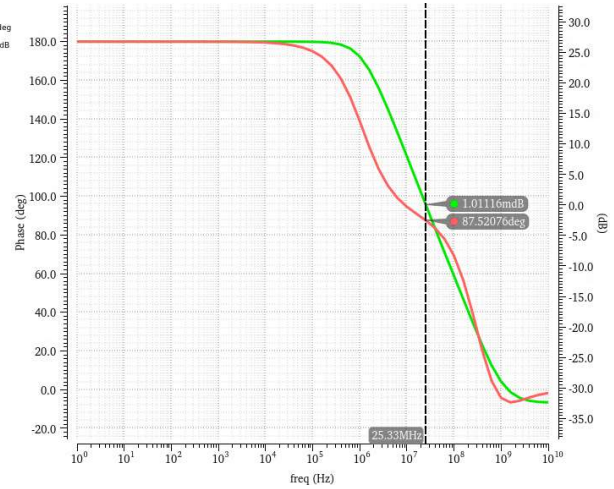


Figure: AC Response

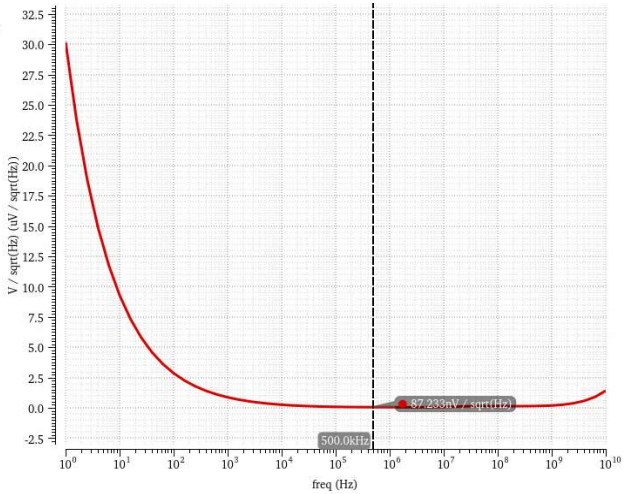


Figure: Input Noise

Parameter	Value
Ibias (µA)	5
R2	41.8kΩ
C1	133fF
Gain (dB)	26.8
GBW (MHz)	25.33
PM (◦)	87.5
IRN @ 500 KH	87.233 nV/sqrt(Hz)

Table: Parameter Values

Amplifiers	Folded PMOS	Folded NMOS	2-Stage NMOS	2-Stage PMOS	Diff NMOS	Diff PMOS	Bulk Driven NMOS
Technology	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS	180nm CMOS
V_{DD} (V)	3.3	3.3	3.3	3.3	3.3	3.3	3.3
C_{Load} (pF)	1	1	1	1	1	1	1
Gain (dB)	50.77	50.42	51.78	50.18	50.17	45.38	40.22
GBW (MHz)	70.91	70.55	70.15	70.34	70.99	70.12	71.1
Ibias (µA)	200	250	150	150	98	117	400
Voffset (V)	986.4µ	662.3µ	17.33m	-21.75m	-683.2µ	-47.64µ	-6.274m
PM (^{0})	67.48	69.58	50.79	60.05	74.49	84.8	72.74
CMRR (dB)	114.7	99.48	33.02	33.59	71.78	91.21	46.06
PSRR (dB)	-67.01	-73.40	-27.91	-49.77	-50.95	-97.34	-43.92
$ICMR_+$ (V)	2.56	2.85	2.11989	3.04	3.0	3.0	1.25
$ICMR_-$ (V)	560m	768m	320m	826.468m	303m	221.7m	363.7m
IRN (nV /√Hz)	27.96	36.38	38.9	90.95	16.13	20.04	23.45
Power (W)	3.05m	3.89m	4.3m	3.01m	0.57m	0.72m	2.22m
Slew Rate +(V/µs)	113.8	194.2	273.1	253.4	90.82	68.71	1.639
Slew Rate -(V/µs)	162.8	132.8	198.2	514.6	69.09	102.5	171.5
Settling time+ (ns)	26.04	12.94	7.511	41.03	29.29	66.85	305.5
Settling time- (ns)	15.92	25.77	12.66	5.592	66.05	22.54	2.504

Table: Performance summary of the designed folded cascode, 2-stage and differential amplifiers

Folded Cascode Amplifier with PMOS Input Stage

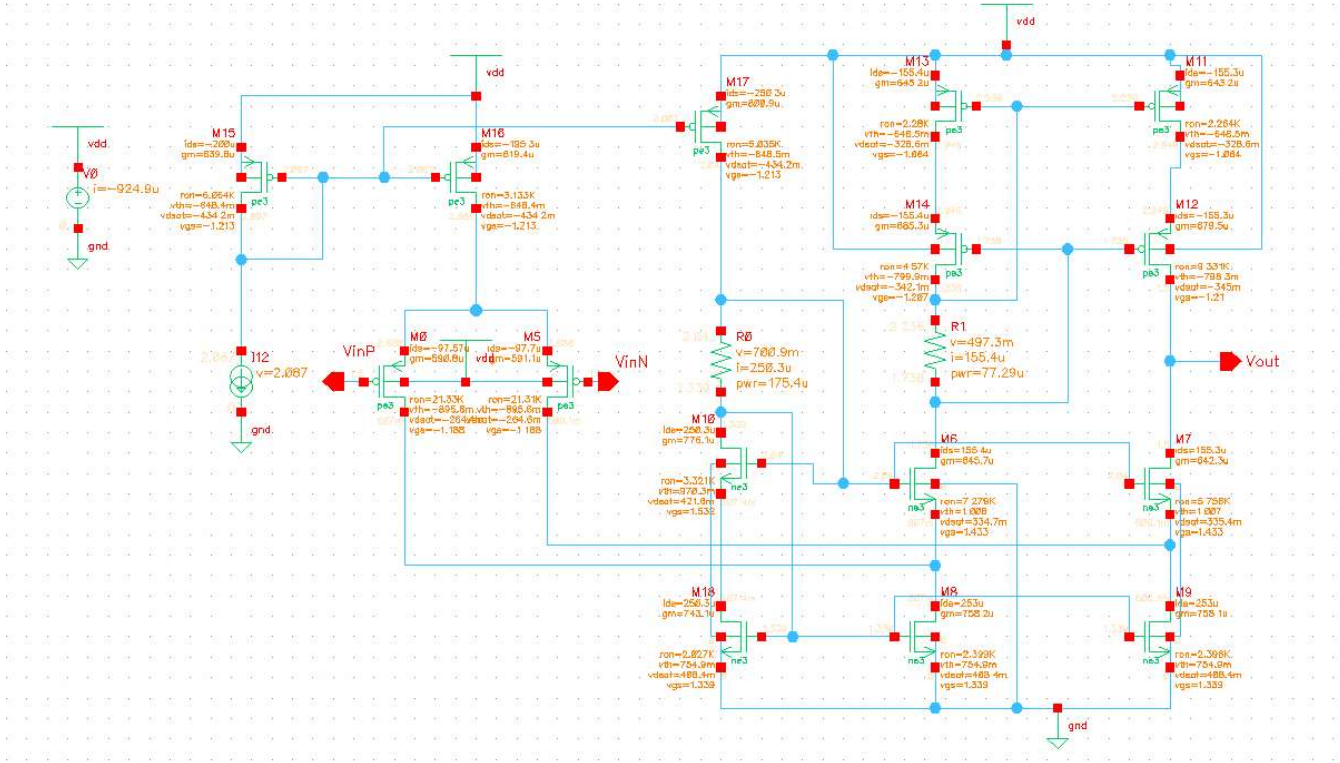
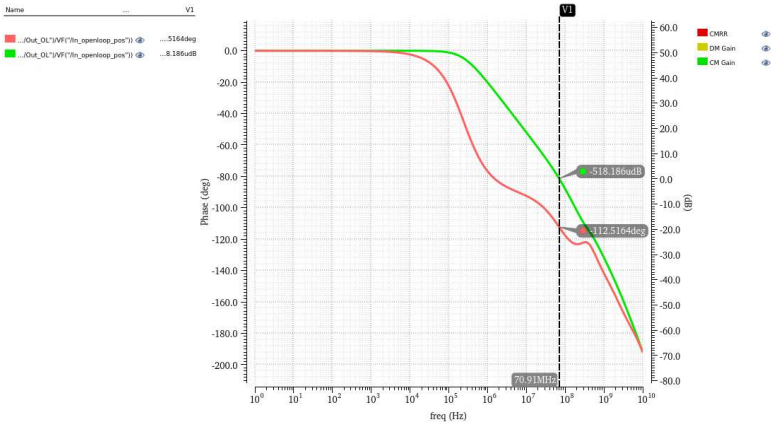


Figure: Schematic of the folded cascode amplifier with PMOS-input stage

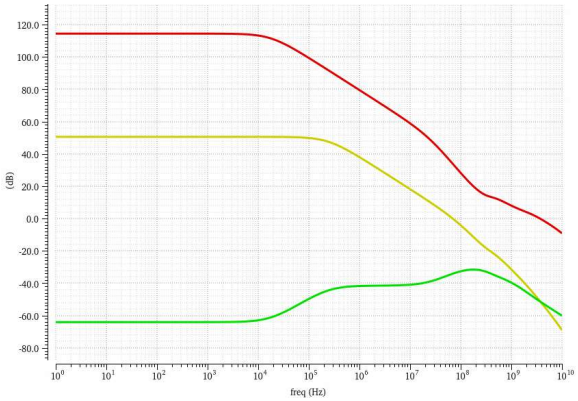
Parameters	Values
Ibias	200µA
Vcm	1.5V
R0	2.8kΩ
R1	3.2kΩ

Table: Parameter Values

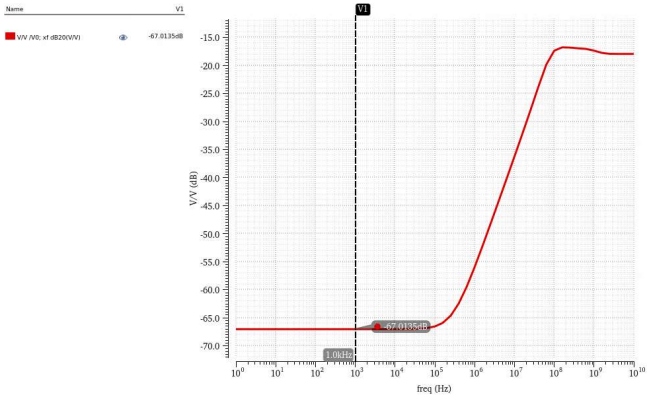
Folded Cascode Amplifier with PMOS Input Stage



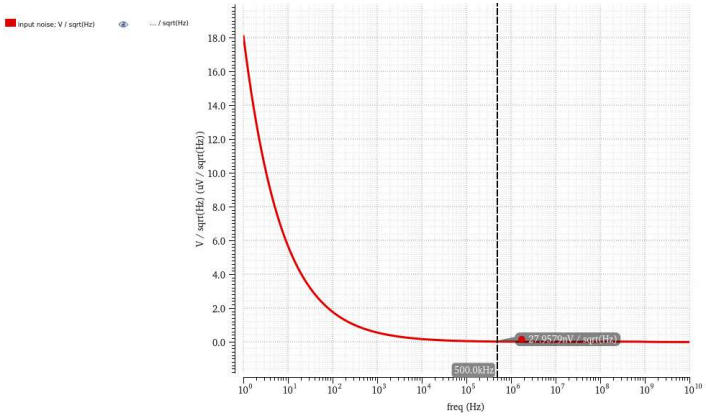
(a) Gain and Phase



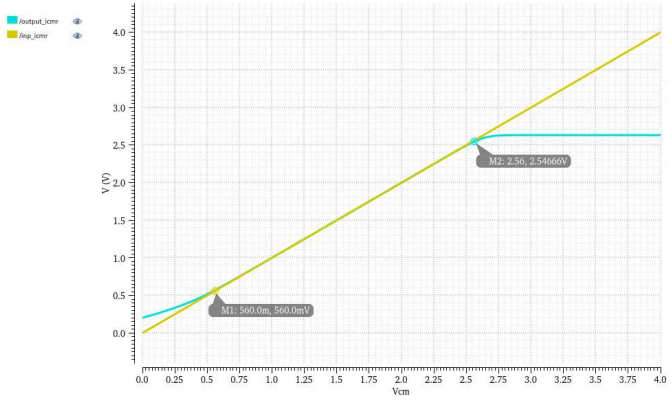
(b) CMRR



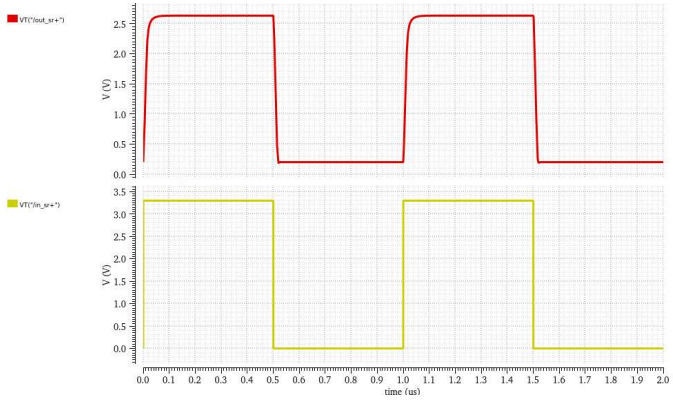
(c) PSRR



(d) IRN



(e) ICMR



(f) Transient Response

Figure: Simulation results of the folded cascode amplifier with PMOS-input stage

Thank You