Noise performance analysis of common-source, common-drain, common-gate and common-source cascode amplifiers

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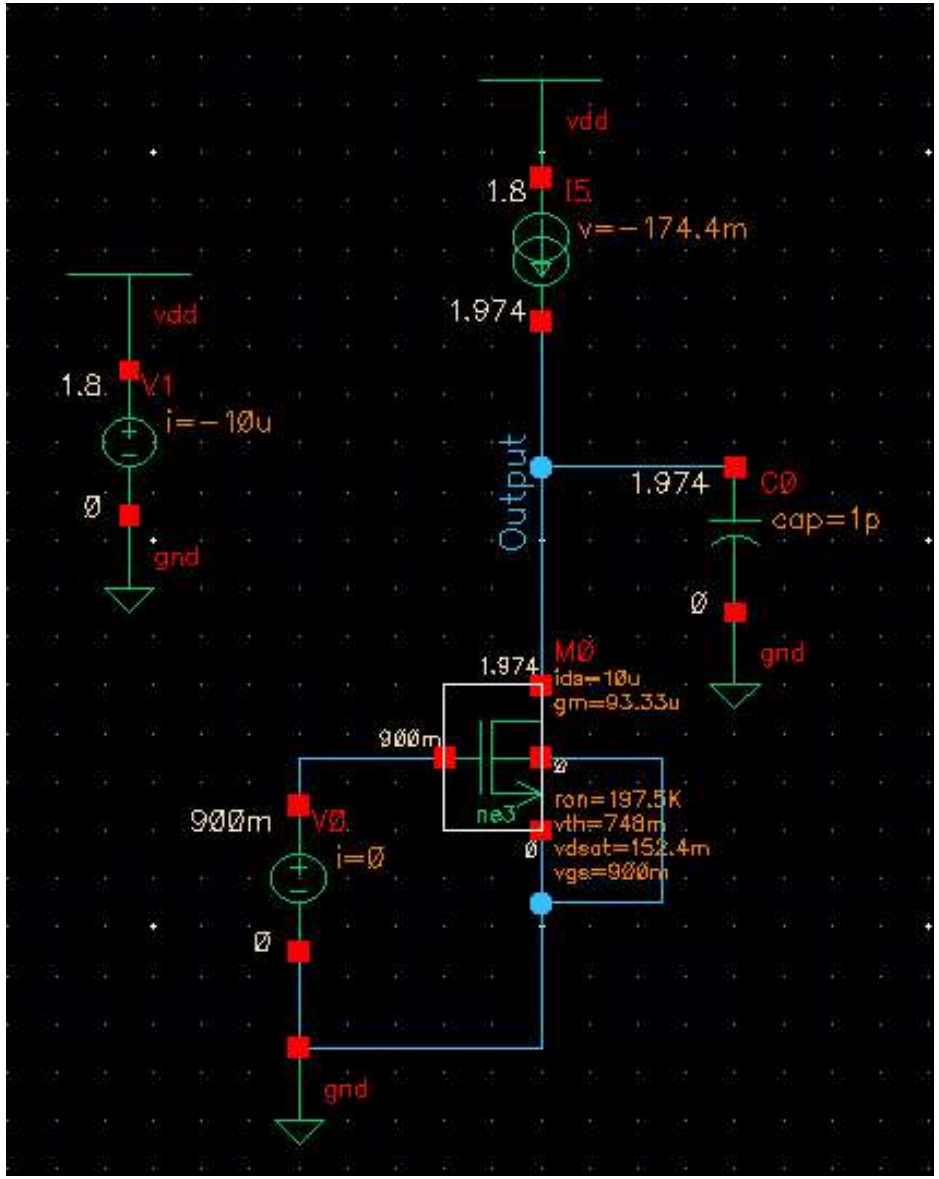
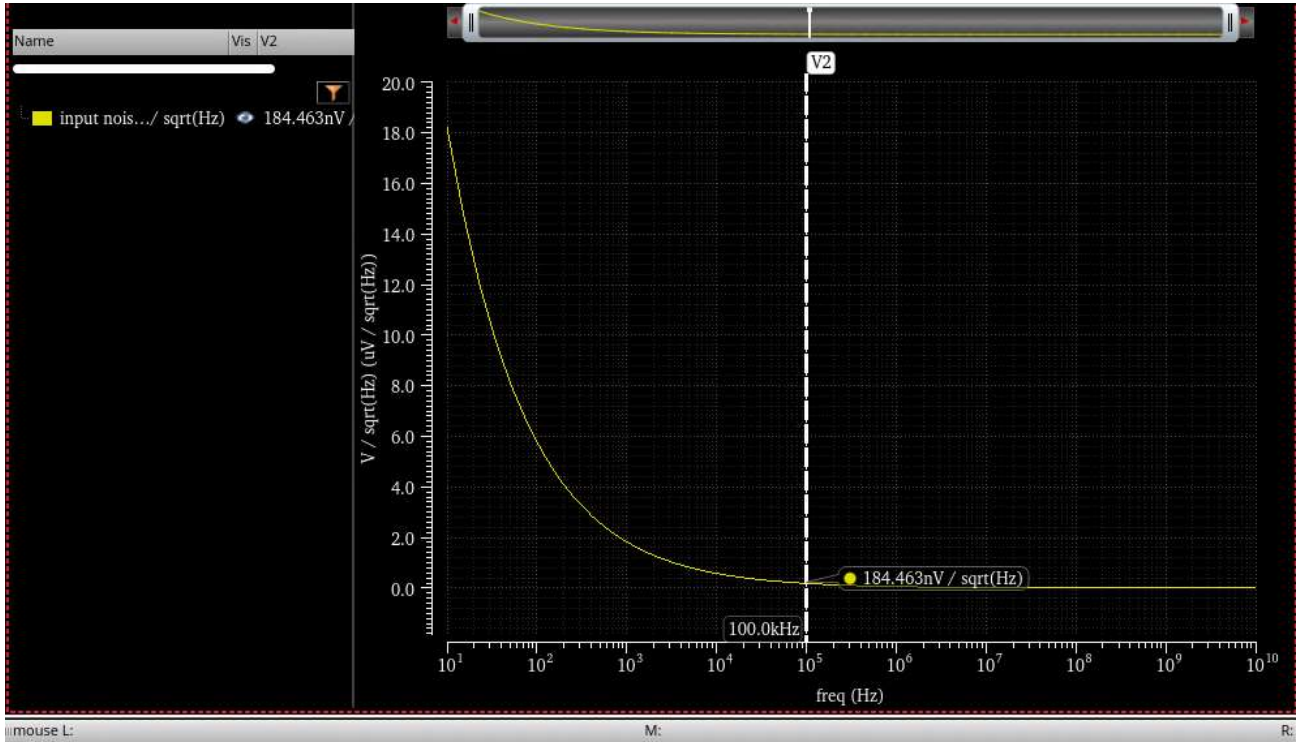
TUHH

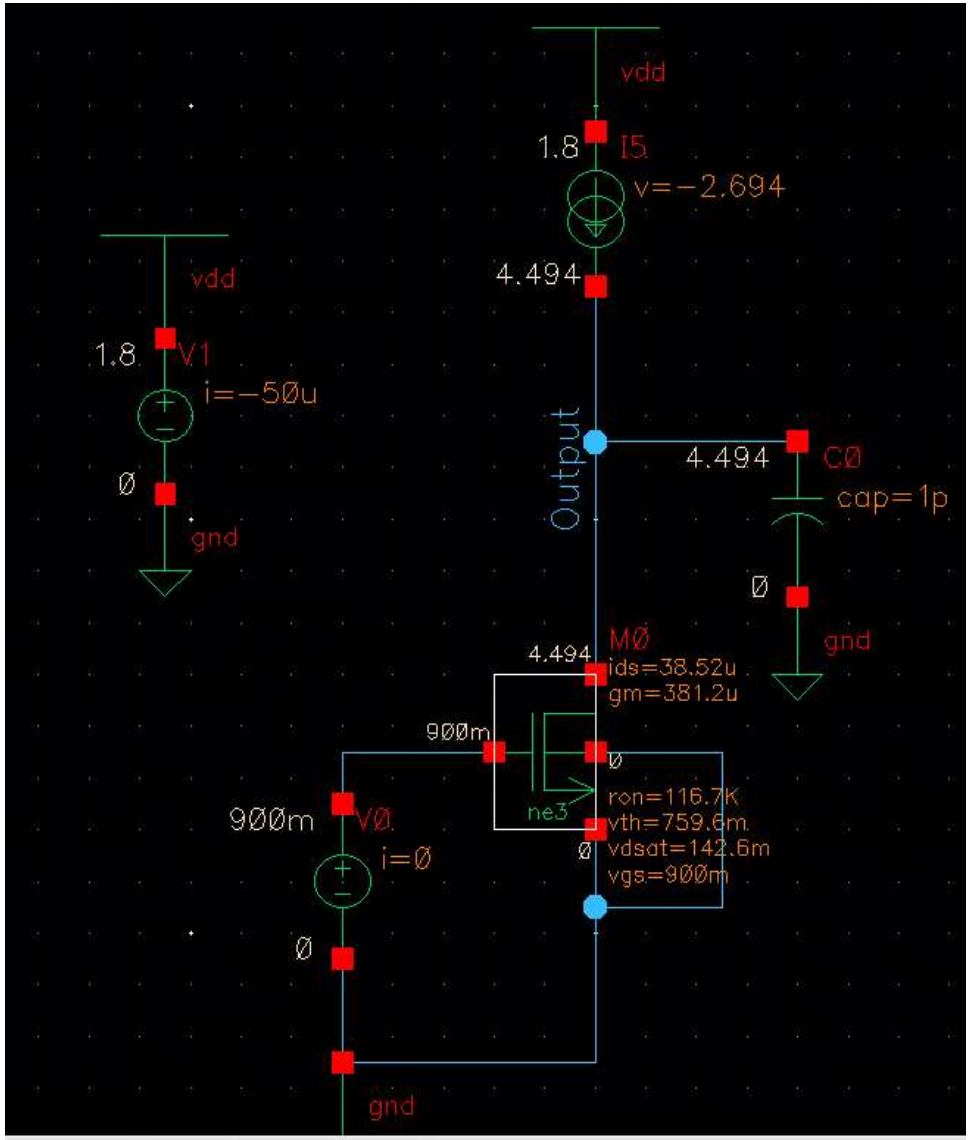
Common-source amplifier with ideal current source load, ID = 10uA

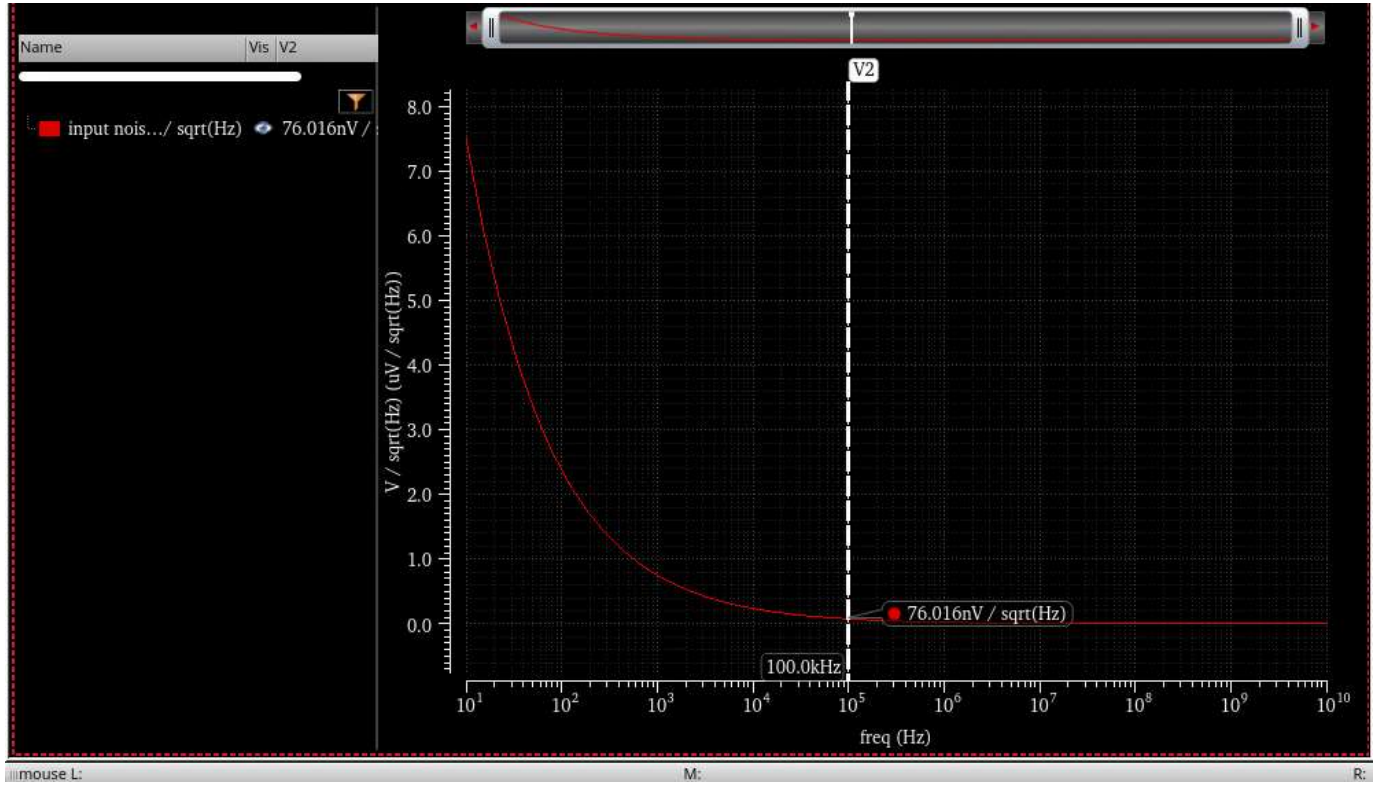




Parameter	Value
ID	10uA
gm	93.33uS
IRN	184.463nV/sqrt(Hz)

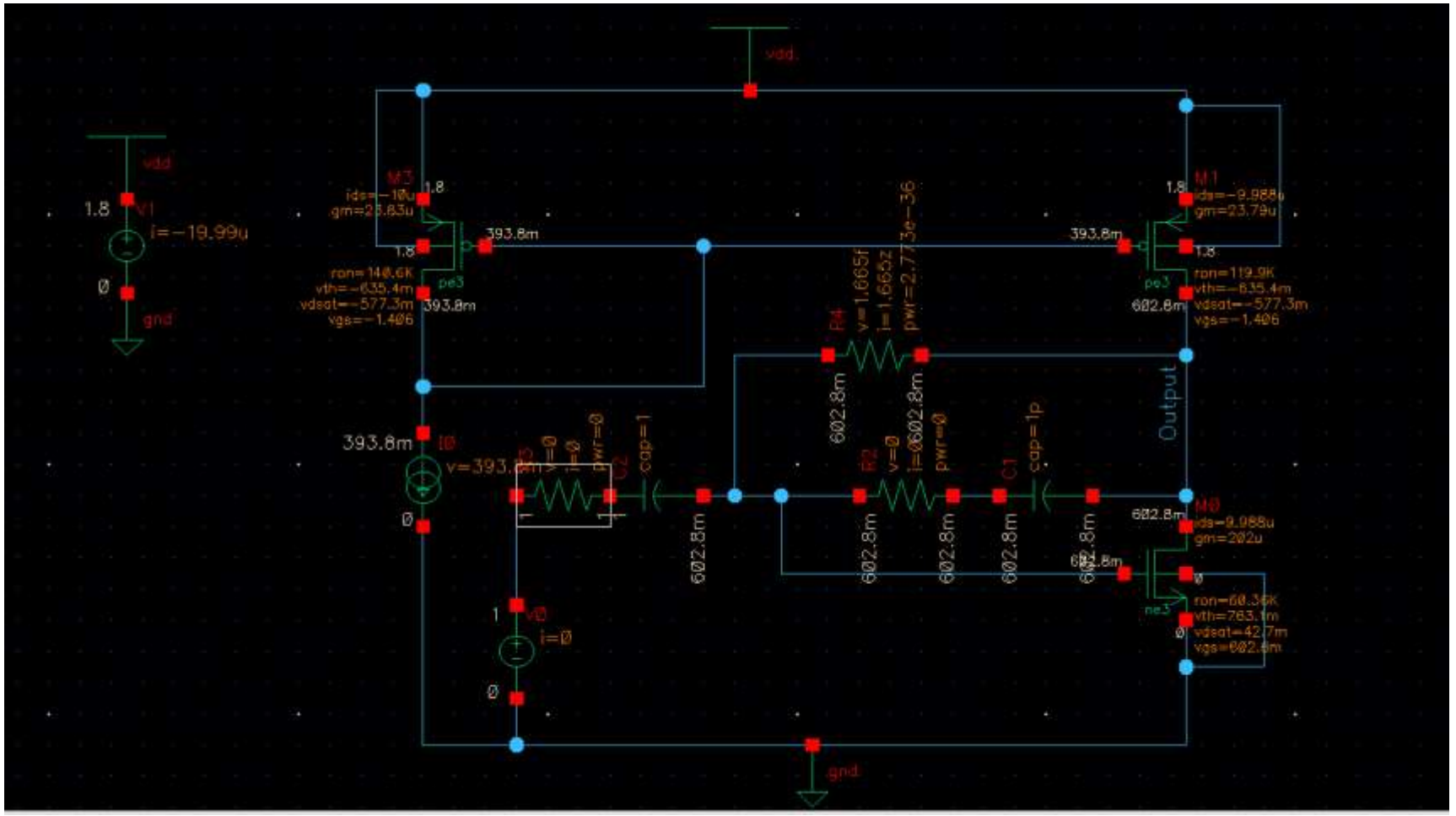
Common-source amplifier with ideal current source load, ID = 50uA





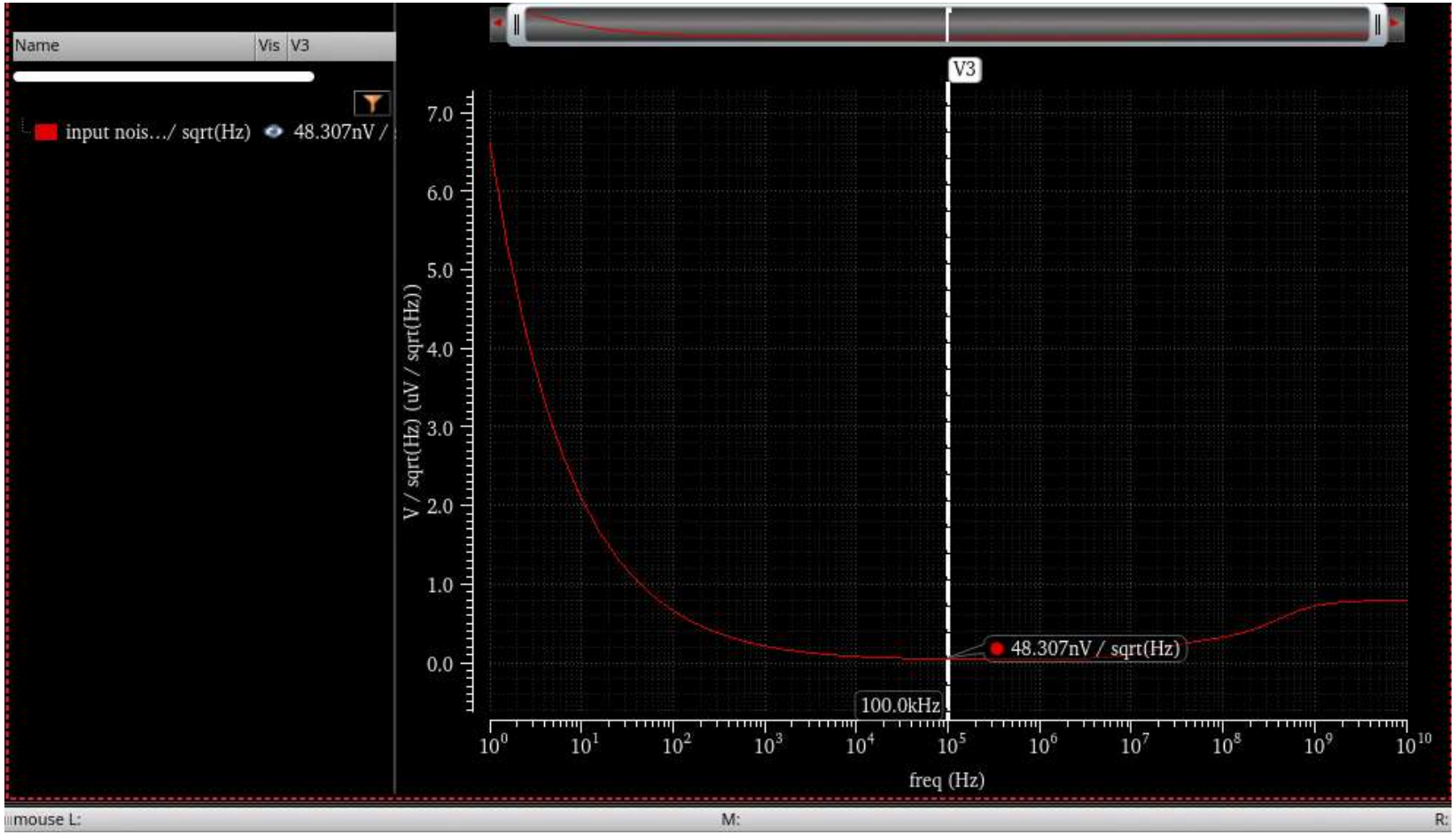
Parameter	Value
ID	50uA
gm	381.2uS
IRN	76.016nV/sqrt(Hz)

Common-source amplifier with PMOS-current source load, ID = 10uA



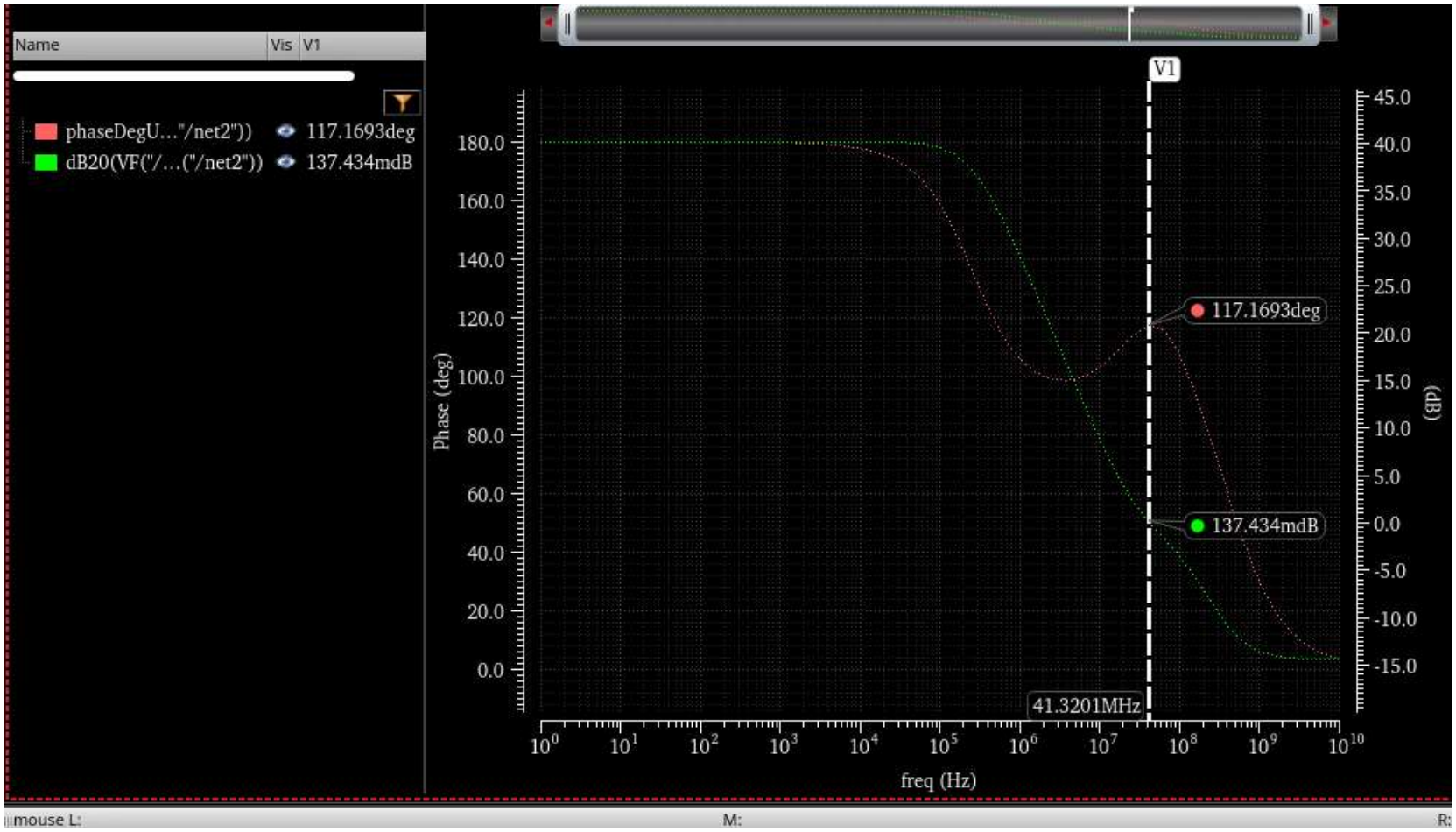
Parameter	Value
ID	10uA
gm	202uS

Common-source amplifier with PMOS-current source load : Input noise curve



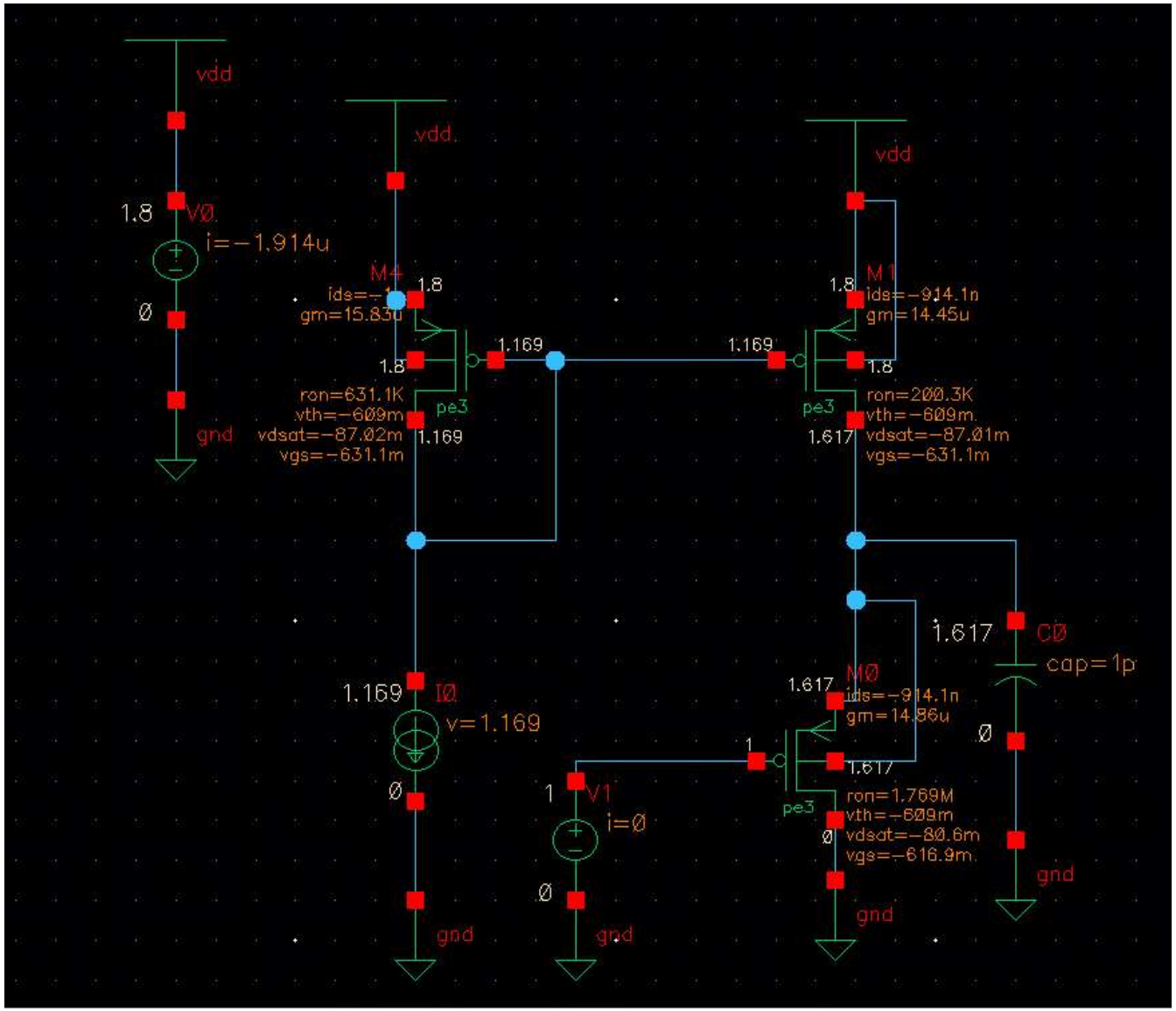
Parameter	Value
ID	10uA
gm	202uS
IRN	48.307nV/sqrt(Hz)

Common-source amplifier with PMOS-current source load: Gain and Phase margin



Parameter	Value
gain	40dB
PM	117.1693 degrees

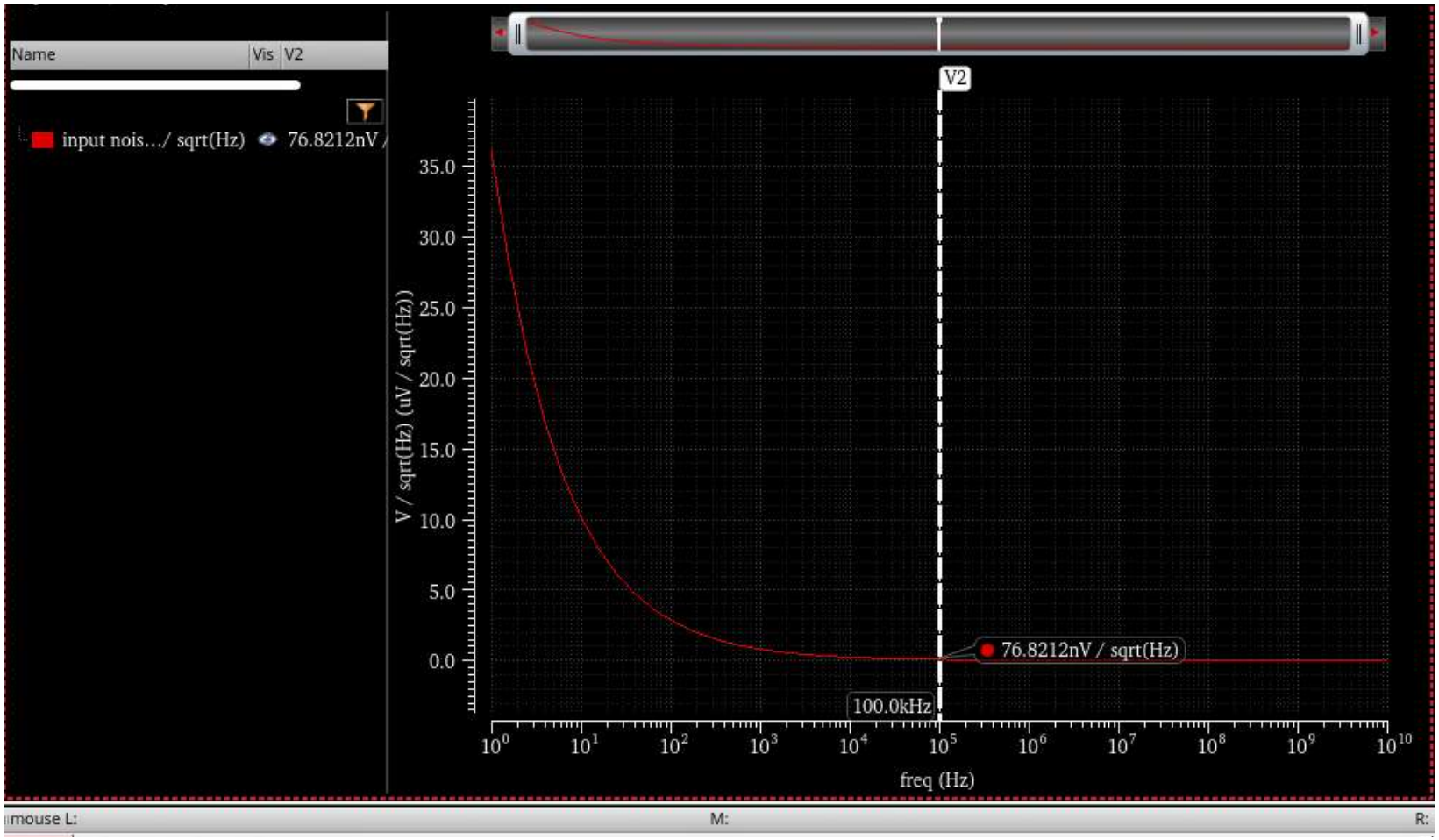
Common-drain amplifier with PMOS-current source load



- Voltage gain Av = 0.9 (Buffer Circuit)
- PMOS input stage used to reduce body effect

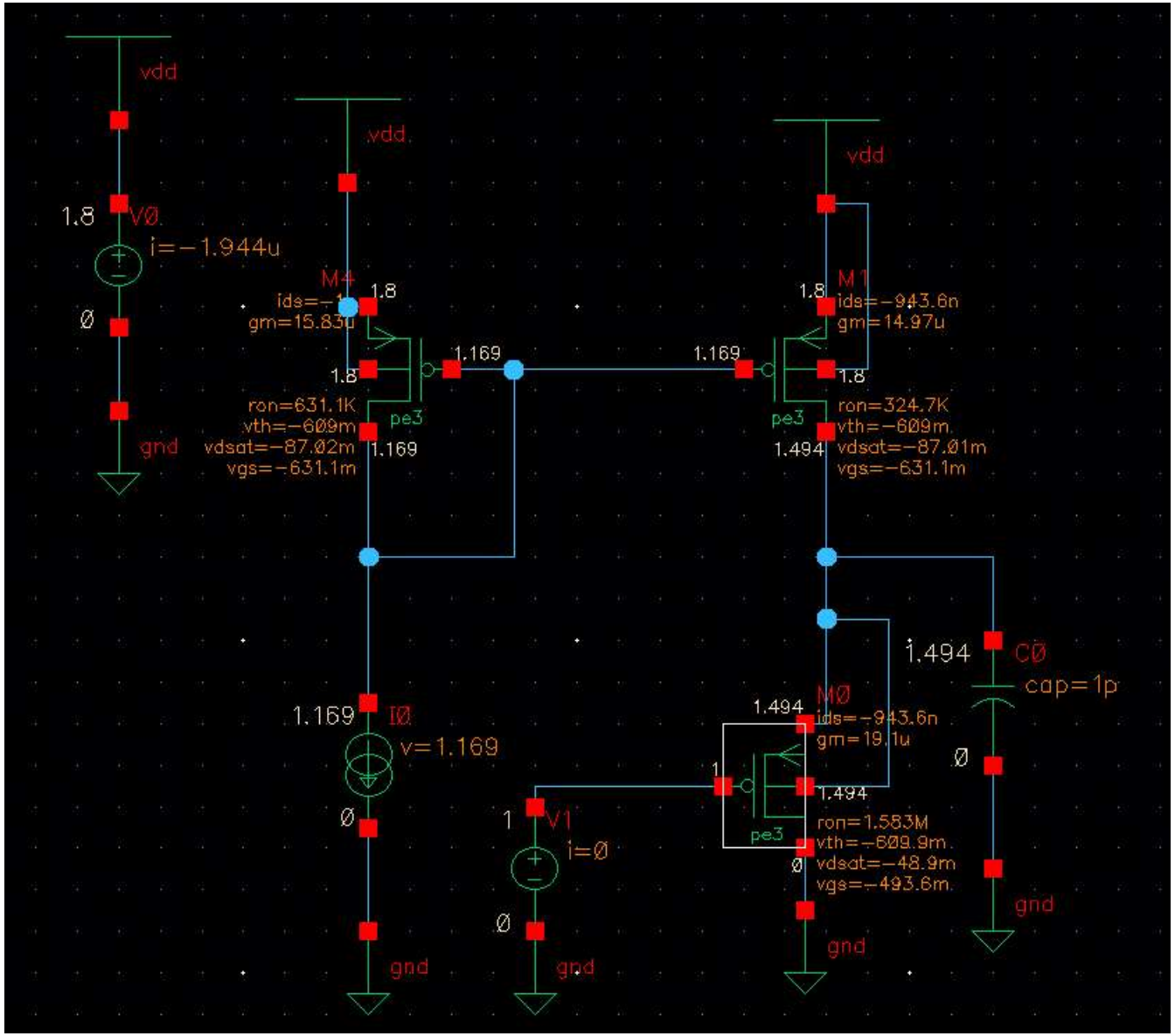
Parameter	Value
ID	1uA
gm	14.86uS

Common-drain amplifier with PMOS-current source load : Input noise curve



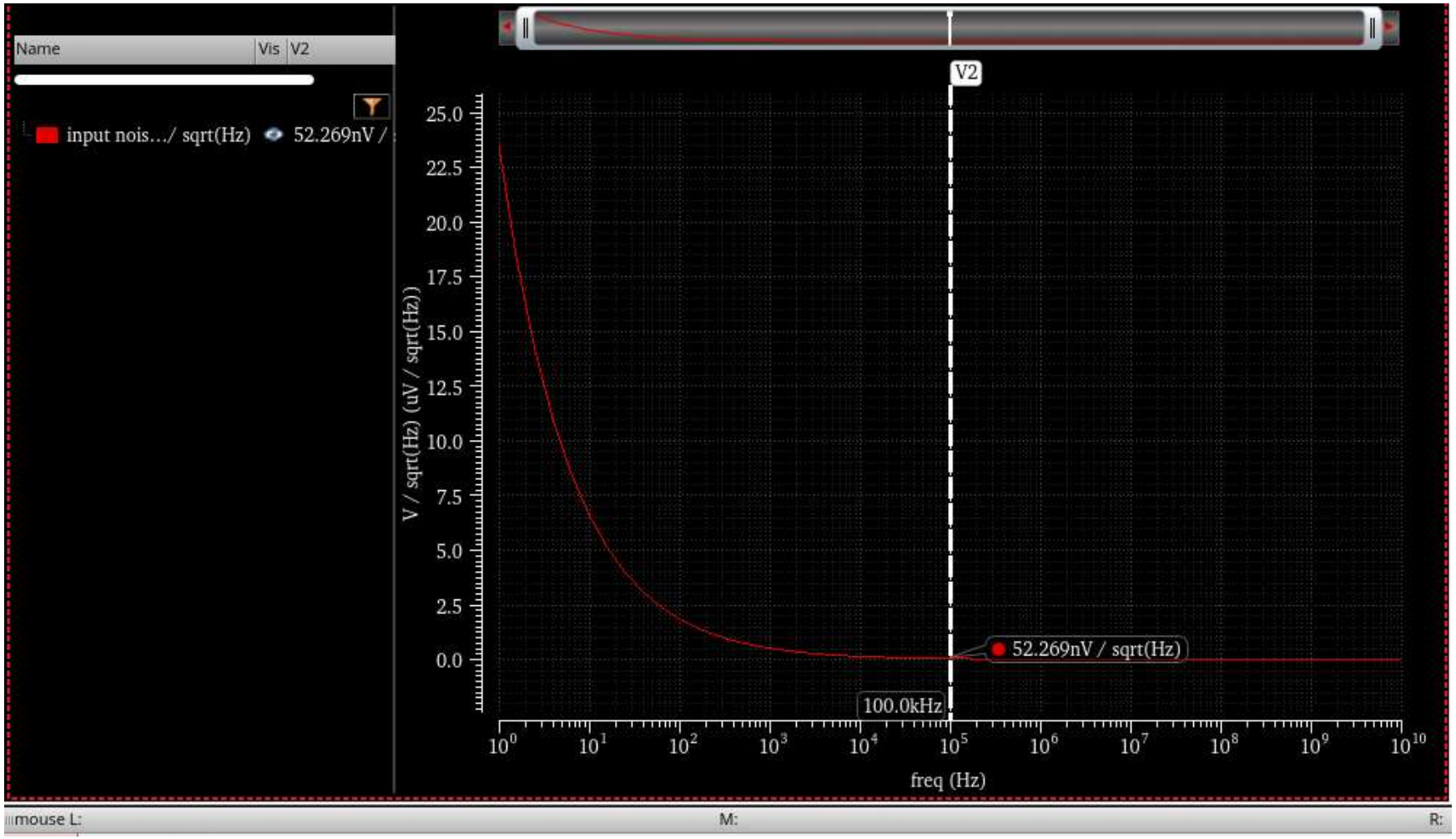
Parameter	Value
IRN	76.82812nV/sqrt(Hz)

Common-drain amplifier with PMOS-current source load : Increasing Gm



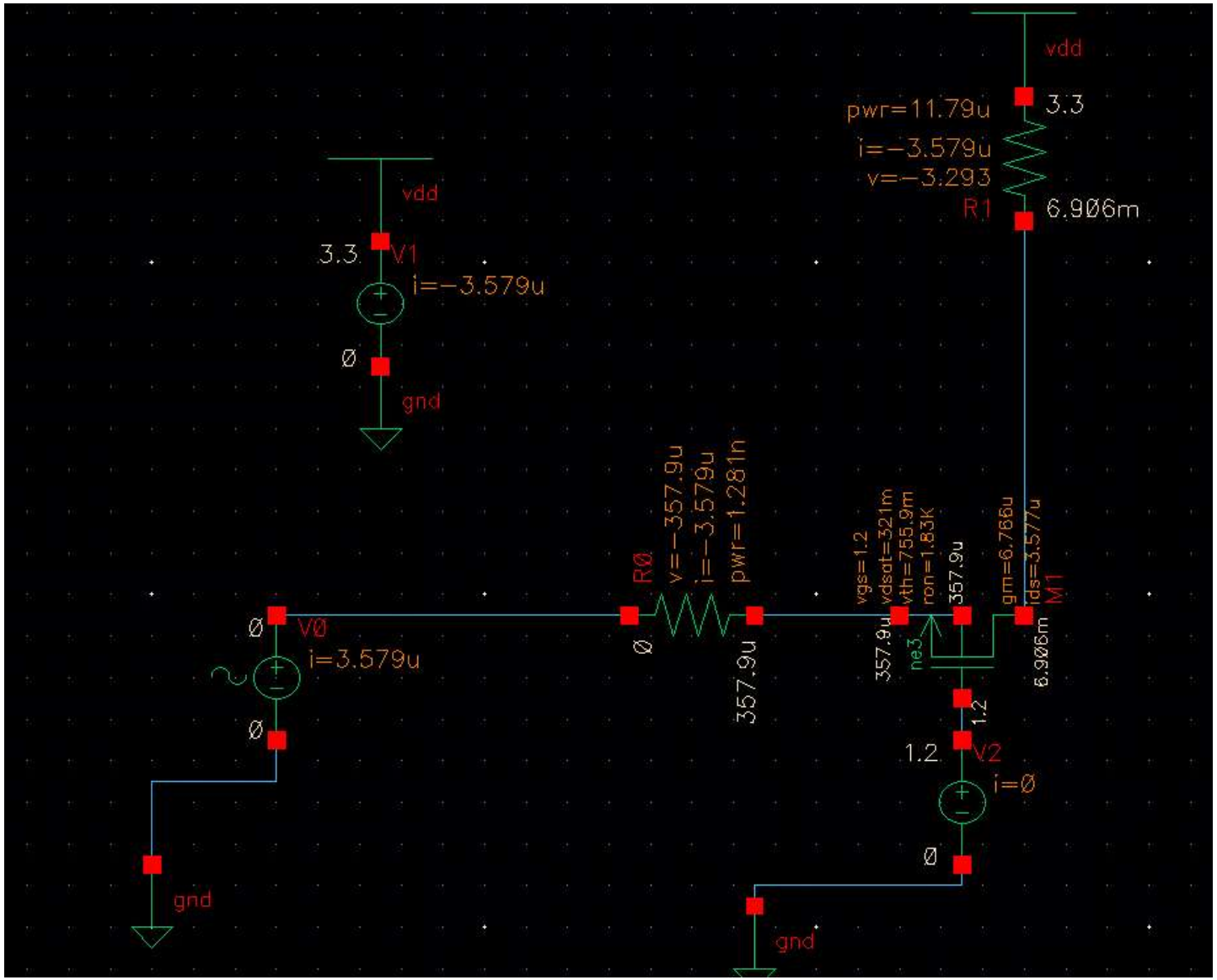
- Increasing W of Input transistor to increase gm.
- Gm = 19.1uS

Common-drain amplifier with PMOS-current source load : Input noise curve with increased gm



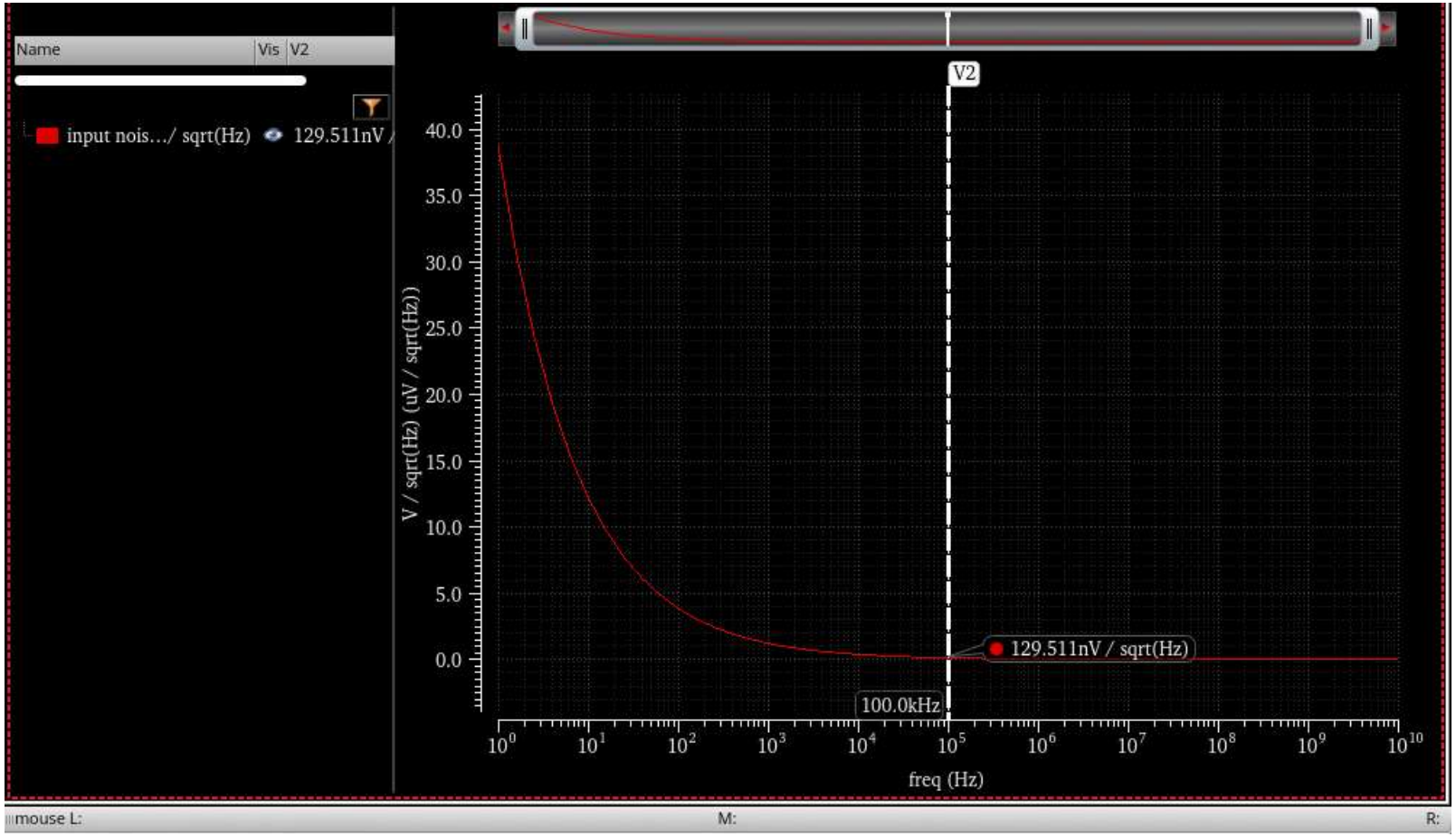
Parameter	Value
IRN	52.269nV/sqrt (Hz)

Common-Gate amplifier with Resistive load, Rload = 920kΩ



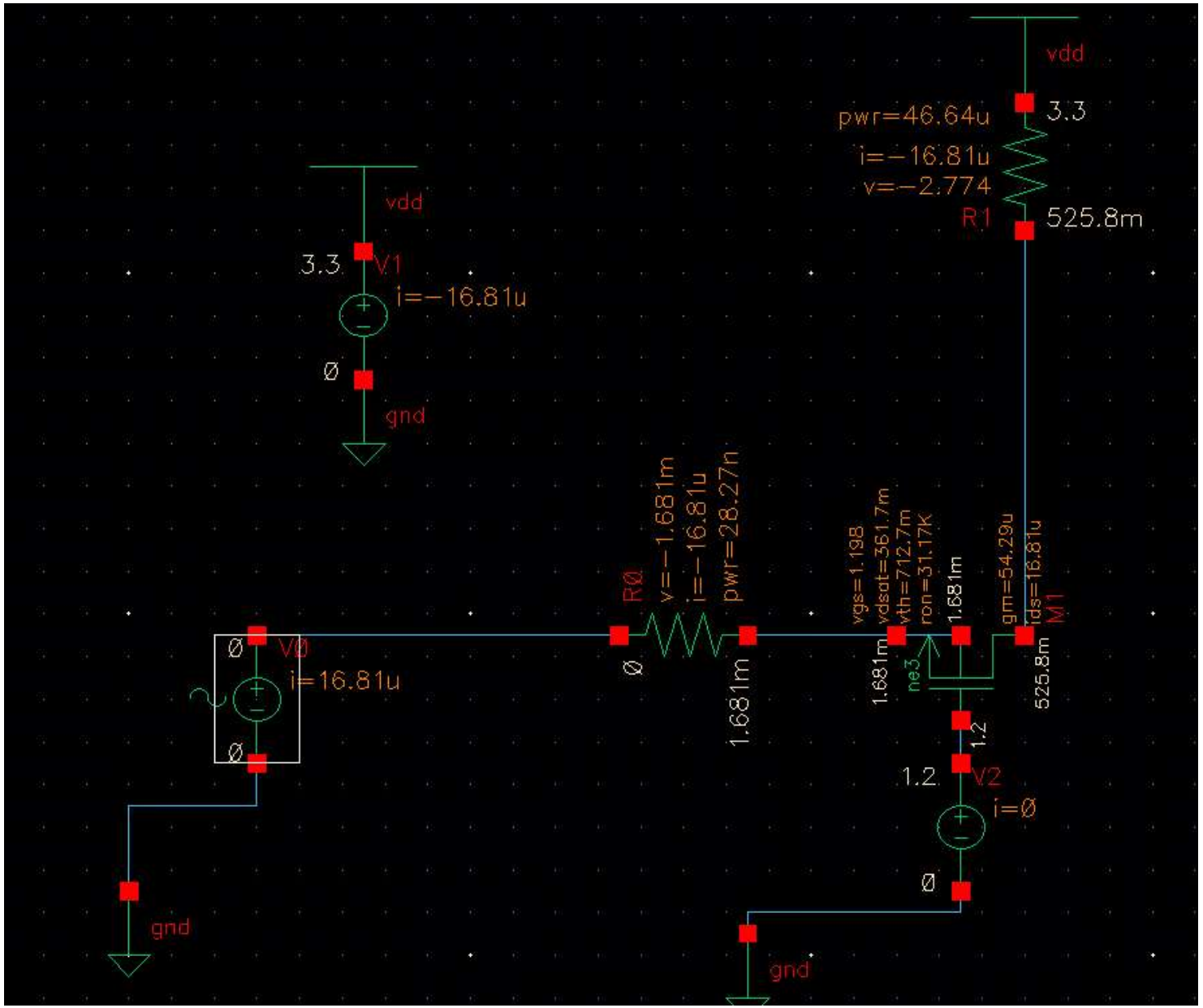
Parameter	Value
ID	3.58uA
gm	6.766uS

Common-Gate amplifier with Resistive load : Input noise curve



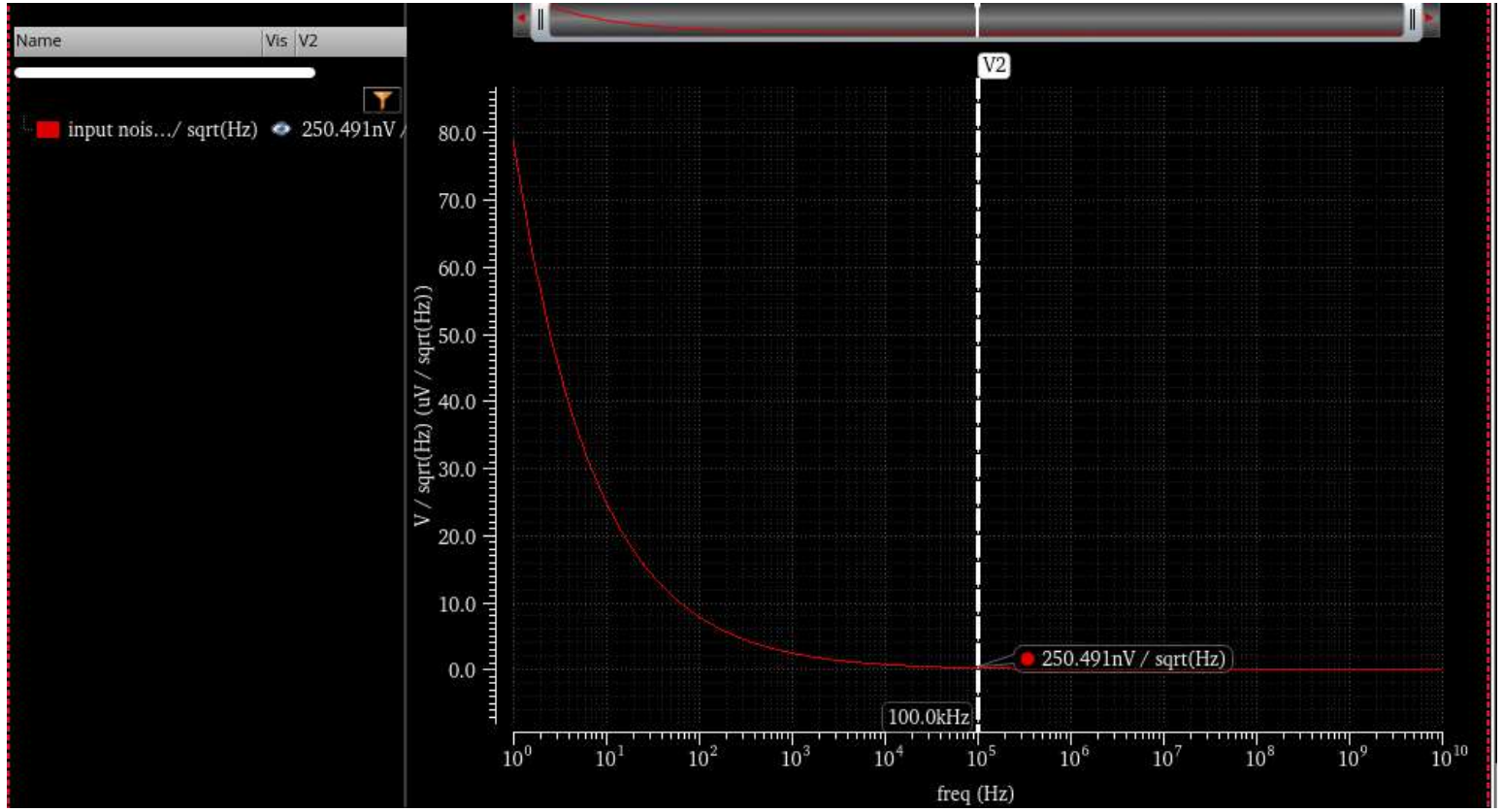
Parameter	Value
IRN	129.51nV/sqrt(Hz)

Common-Gate amplifier with Resistive load, Rload = 165kΩ



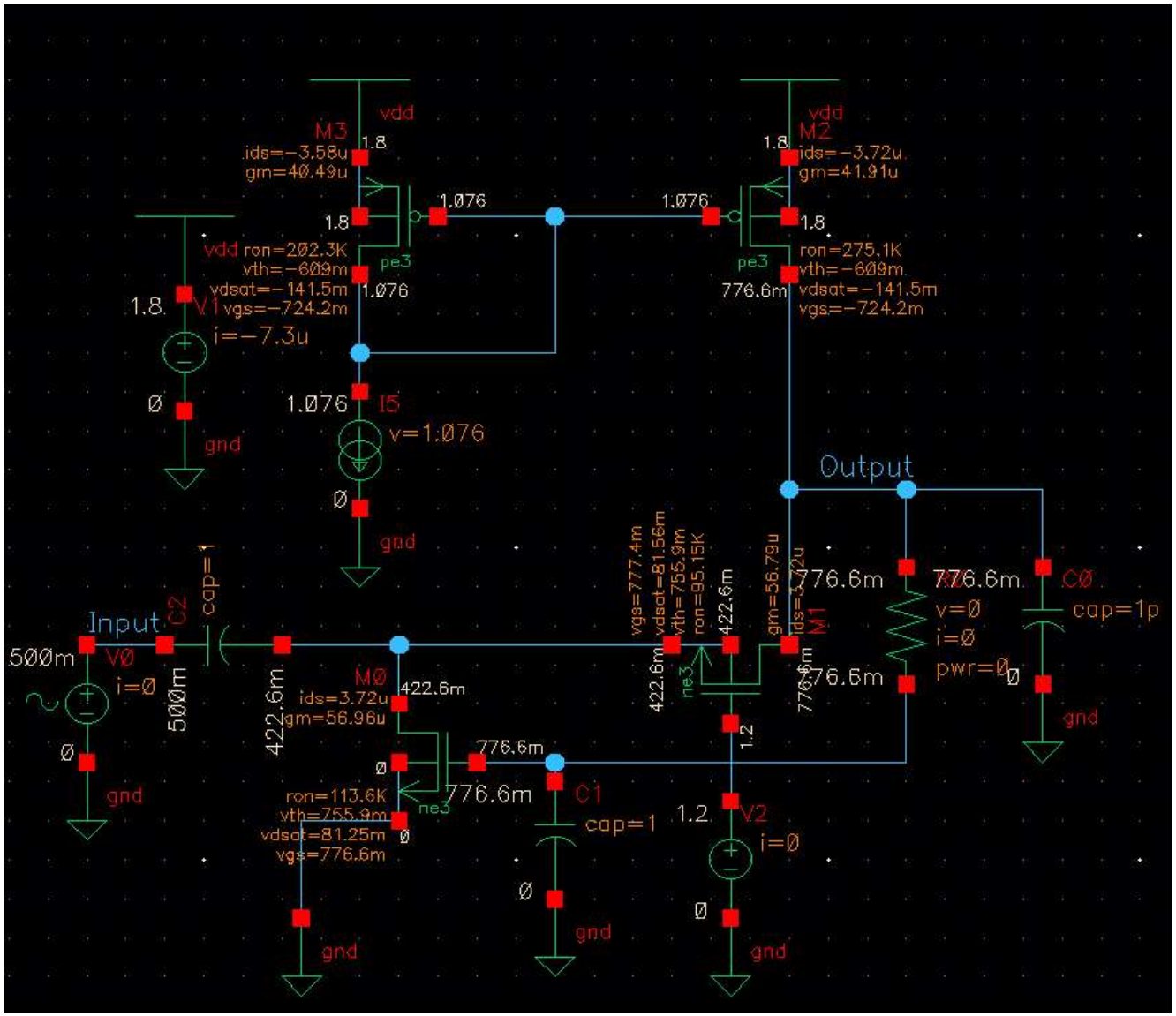
Parameter	Value
ID	16.81uA
gm	54.29uS

Common-Gate amplifier with Resistive load: Input noise curve



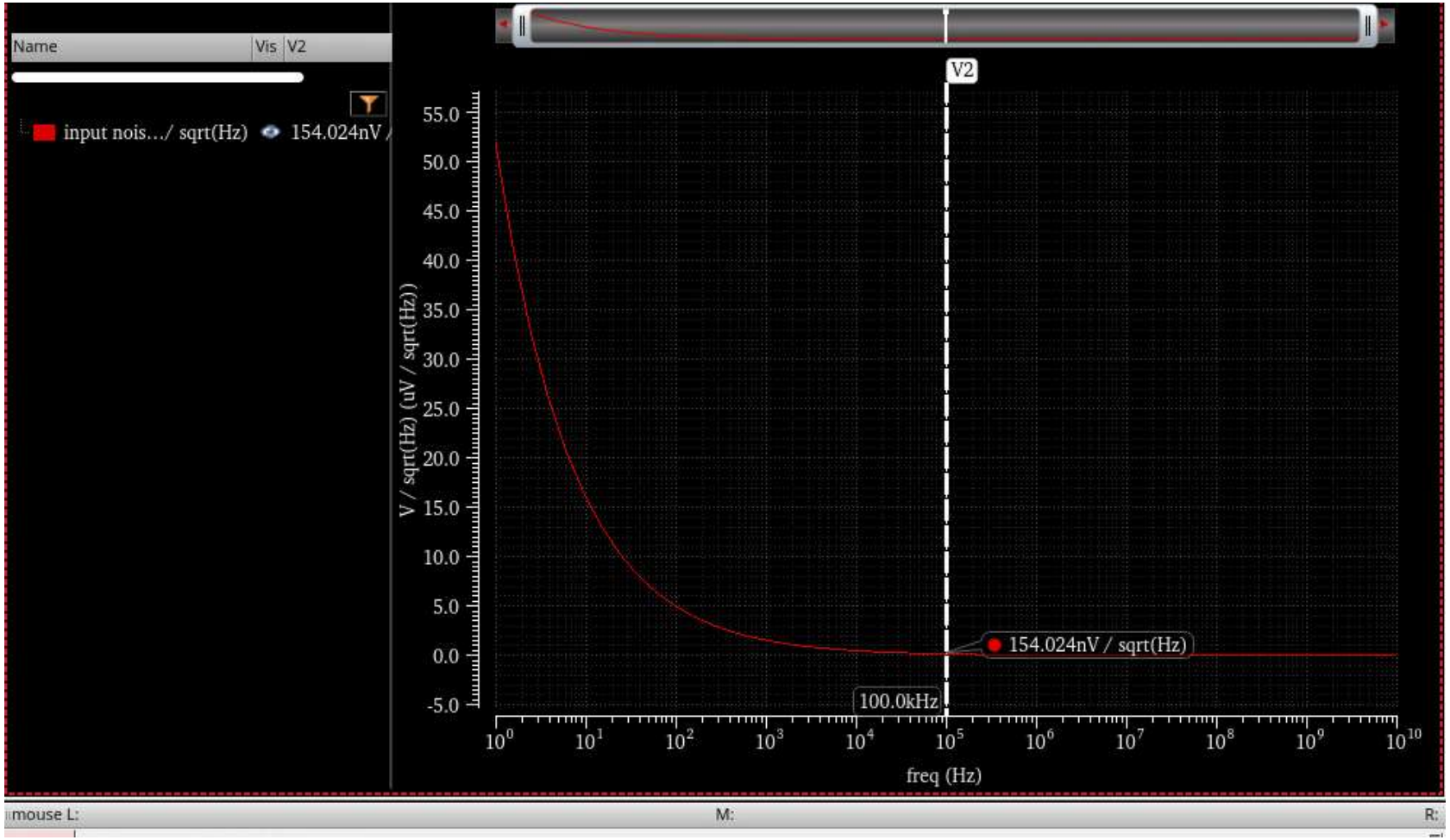
Parameter	Value
IRN	250.491nV/sqrt (Hz)

Common-Gate amplifier with current-source load



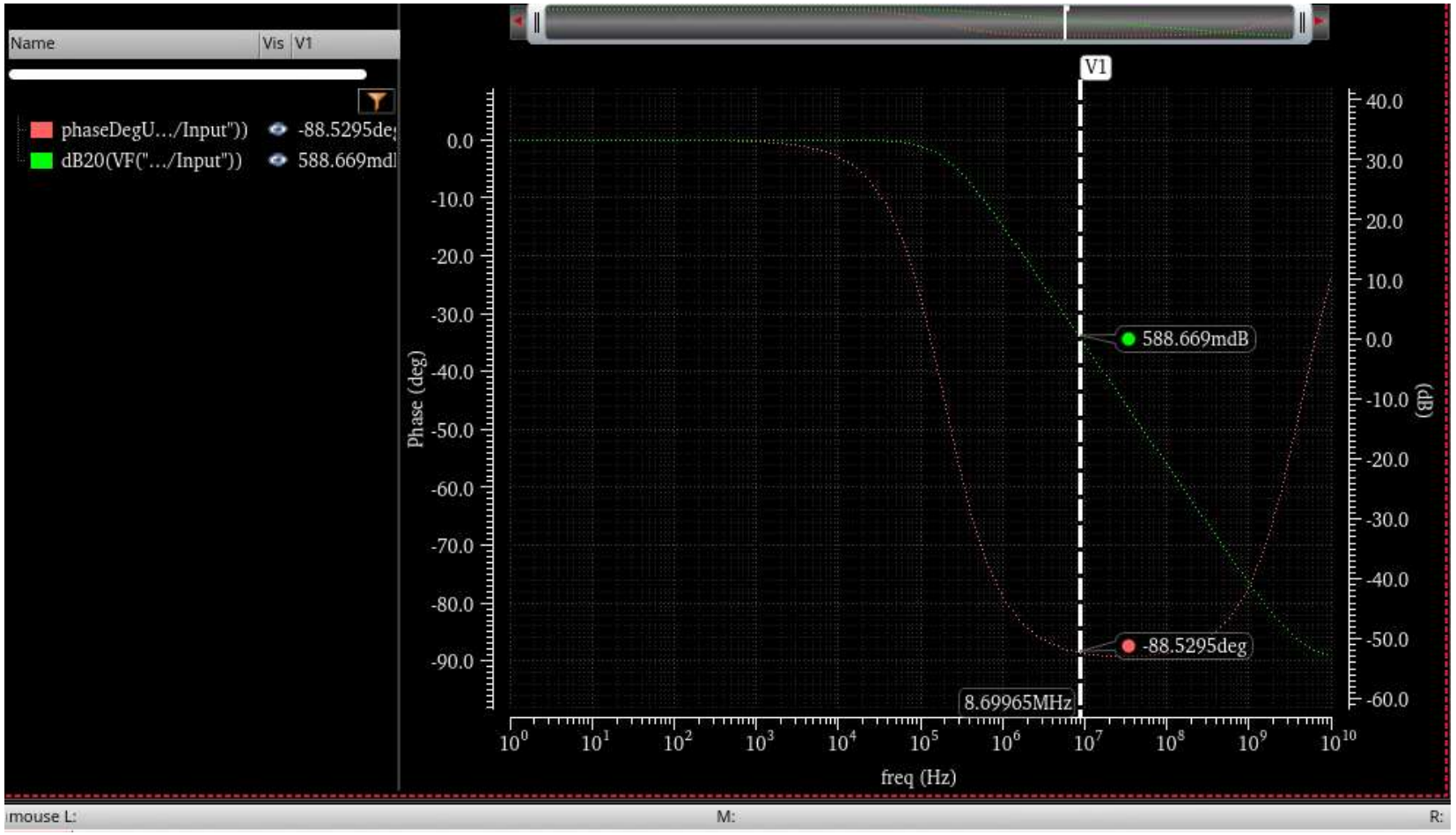
Parameter	Value
ID	3.58uA
gm	56.79uS

Common-Gate amplifier with current-source load : Input noise curve



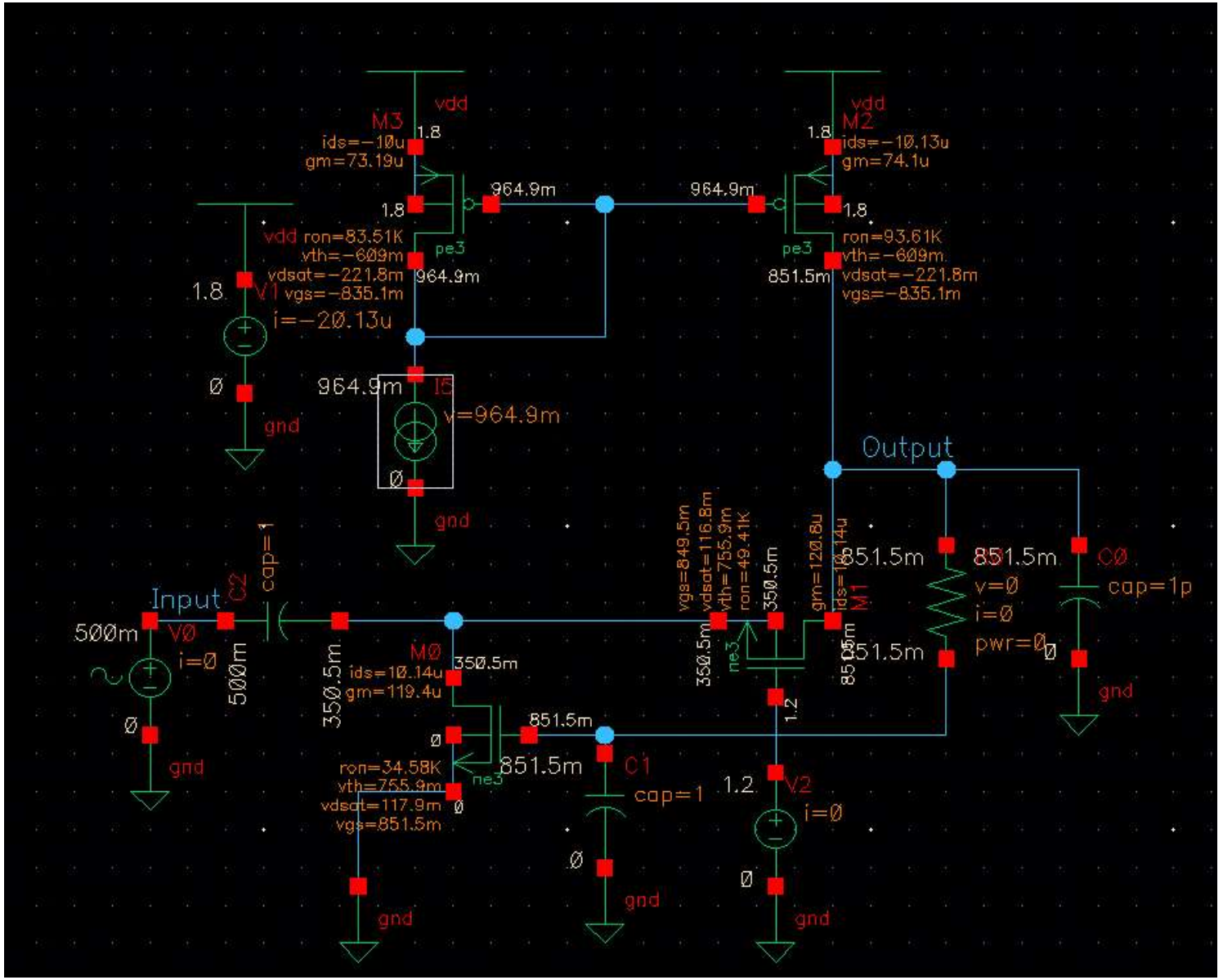
Parameter	Value
IRN	154.024nV/sqrt(Hz)

Common-Gate amplifier with current-source load: Gain and phase margin



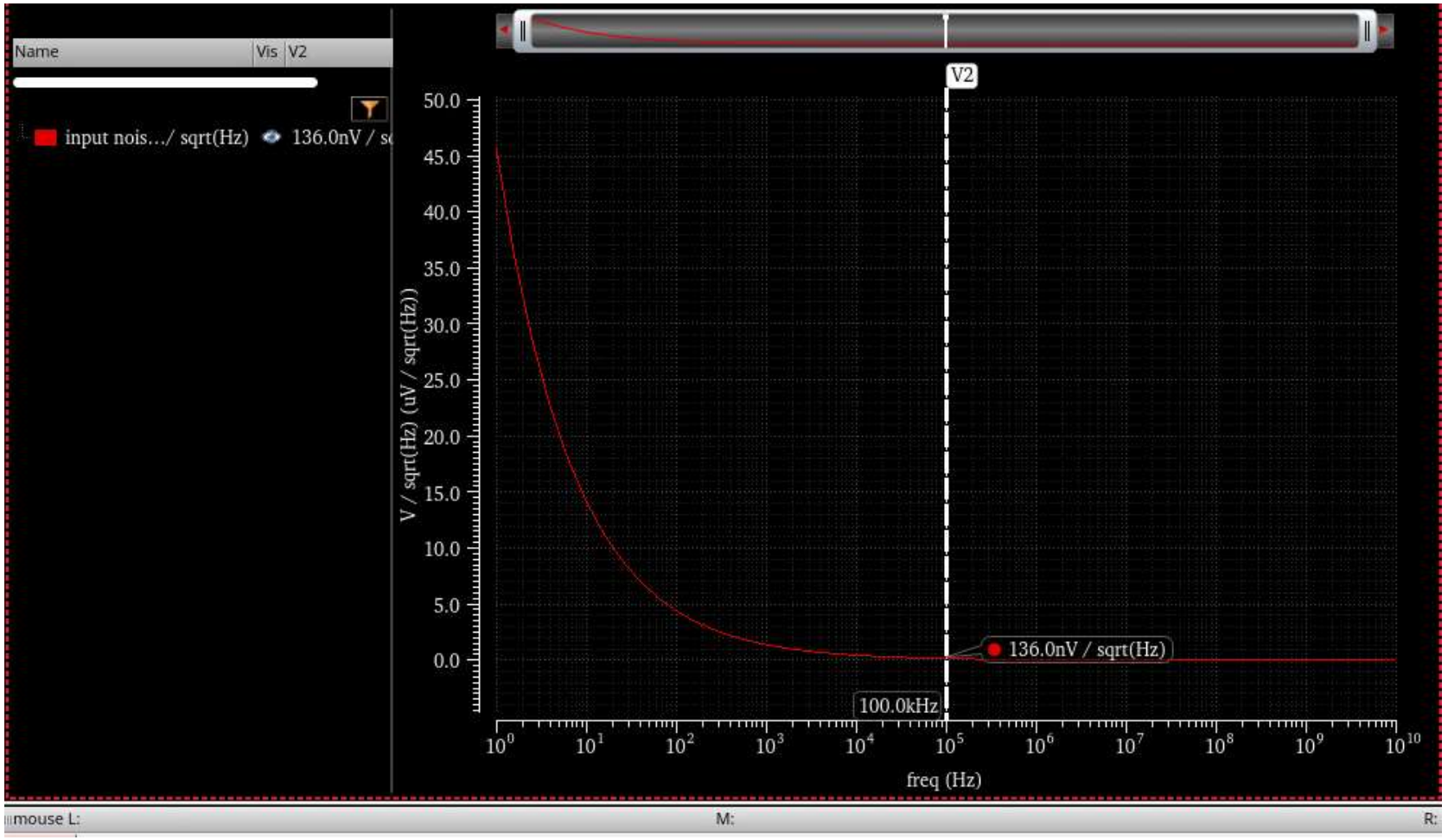
Parameter	Value
Gain	32dB
PM	90 degrees

Common-Gate amplifier with current-source load : Increasing gm by increasing ID to 10uA



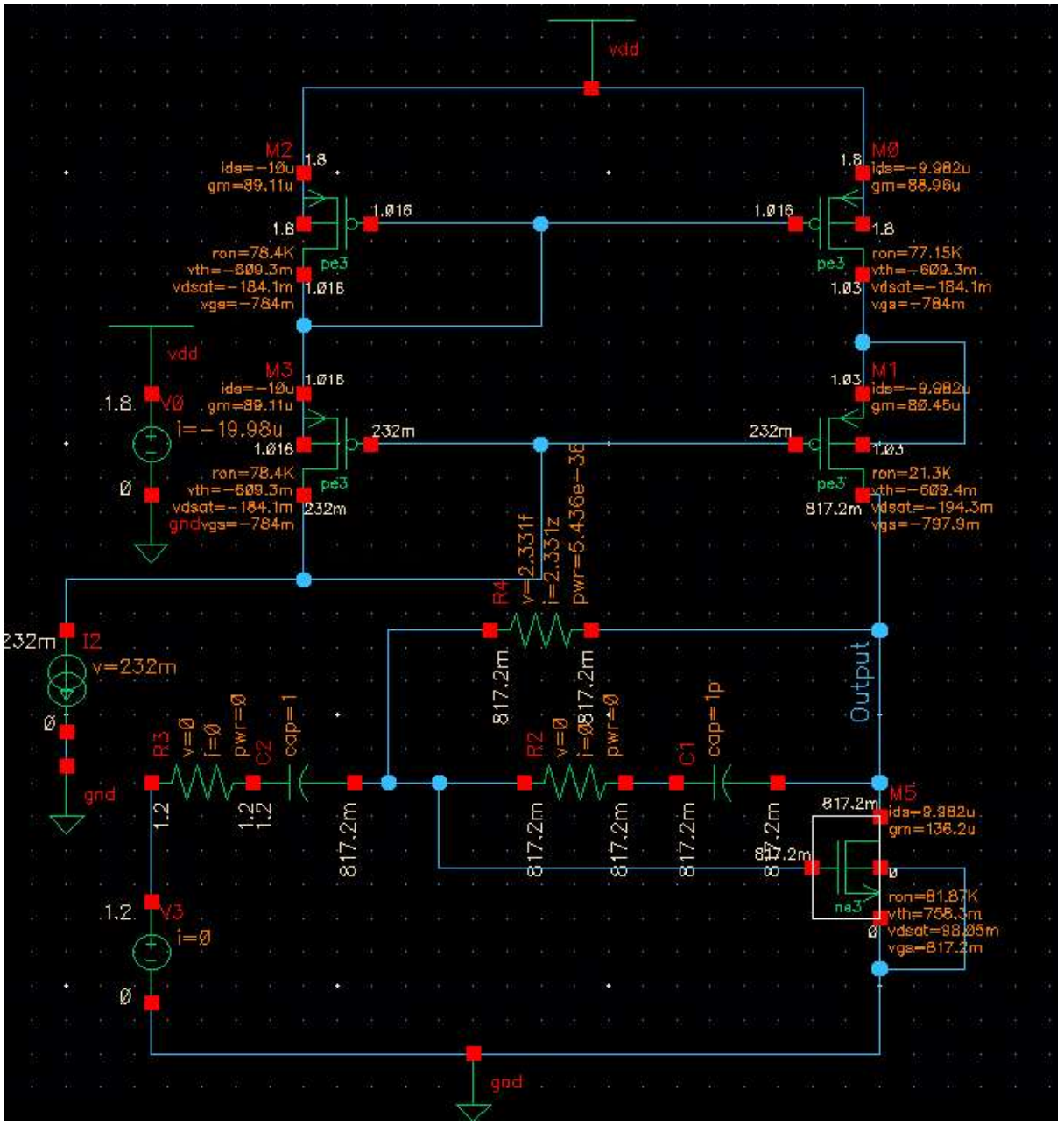
Parameter	Value
ID	10uA
gm	120.6uS

Common-Gate amplifier with current-source load: Input noise curve



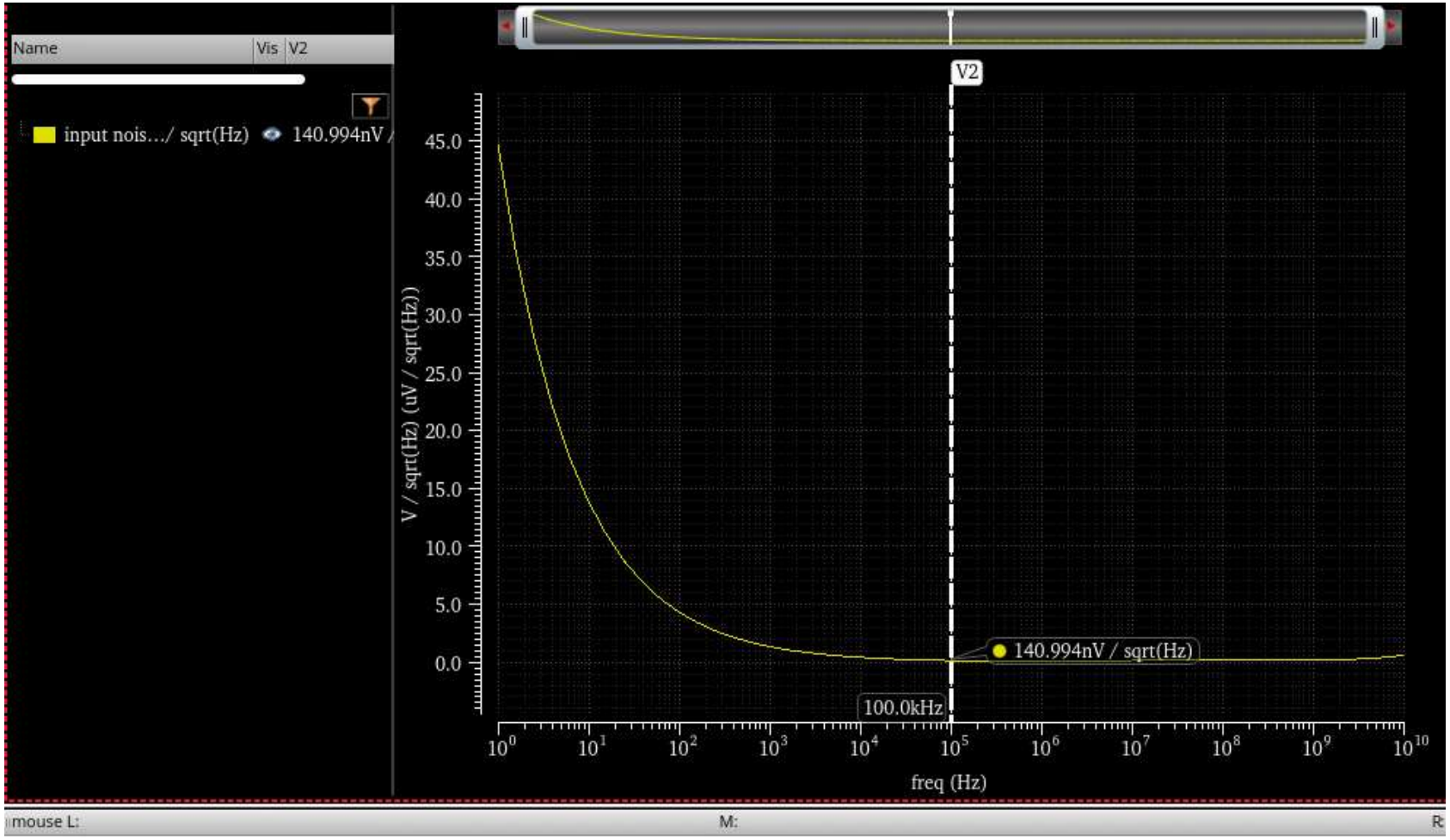
Parameter	Value
IRN	136nV/sqrt(Hz)

Cascode Amplifiers : cascode current source



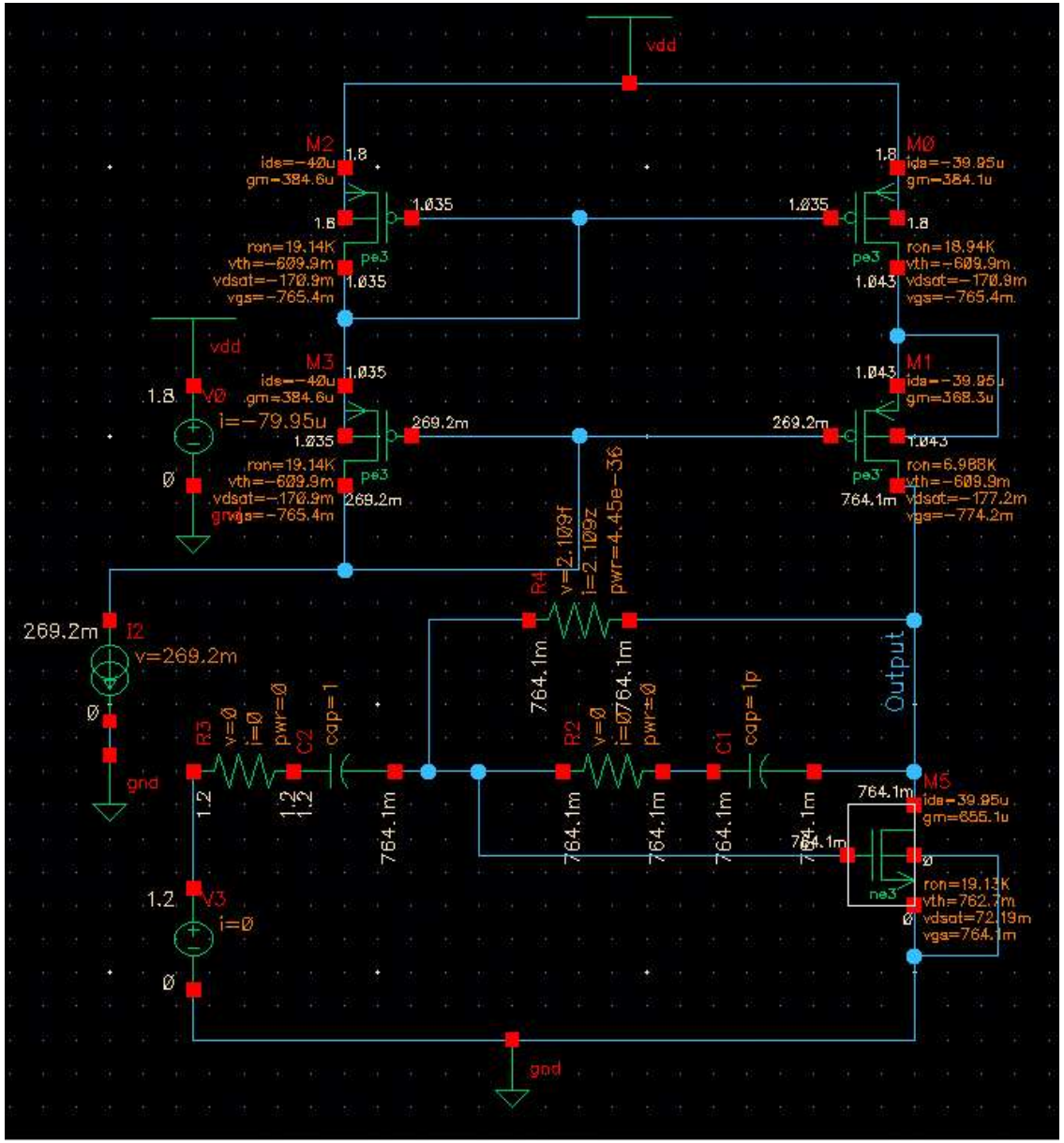
Parameter	Value
ID	10uA
gm	136.2uS

Cascode Amplifiers : cascode current source: Input noise curve



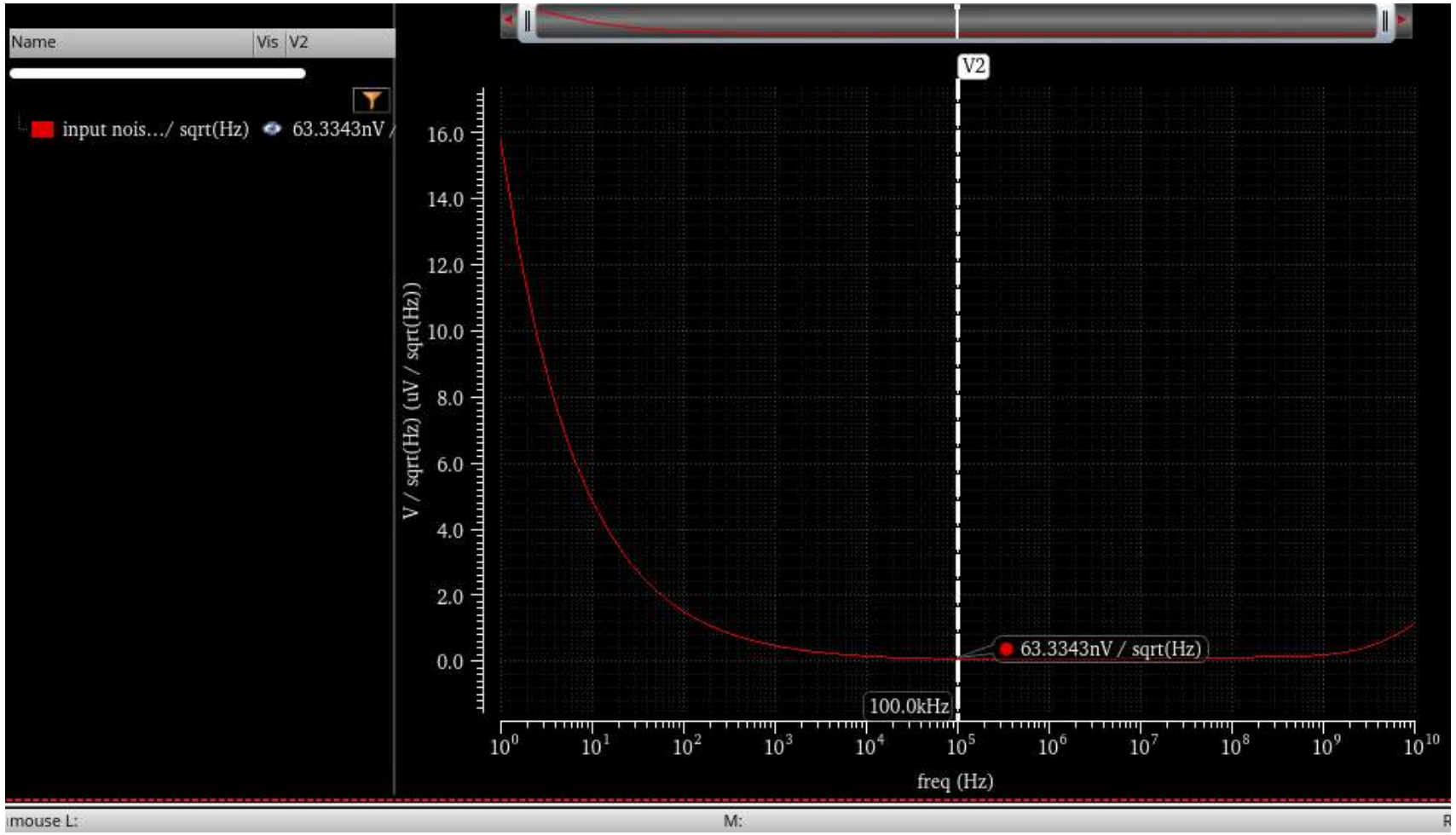
Parameter	Value
IRN	140.994nV/sqrt (Hz)

Cascode Amplifiers : cascode current source : Increased gm



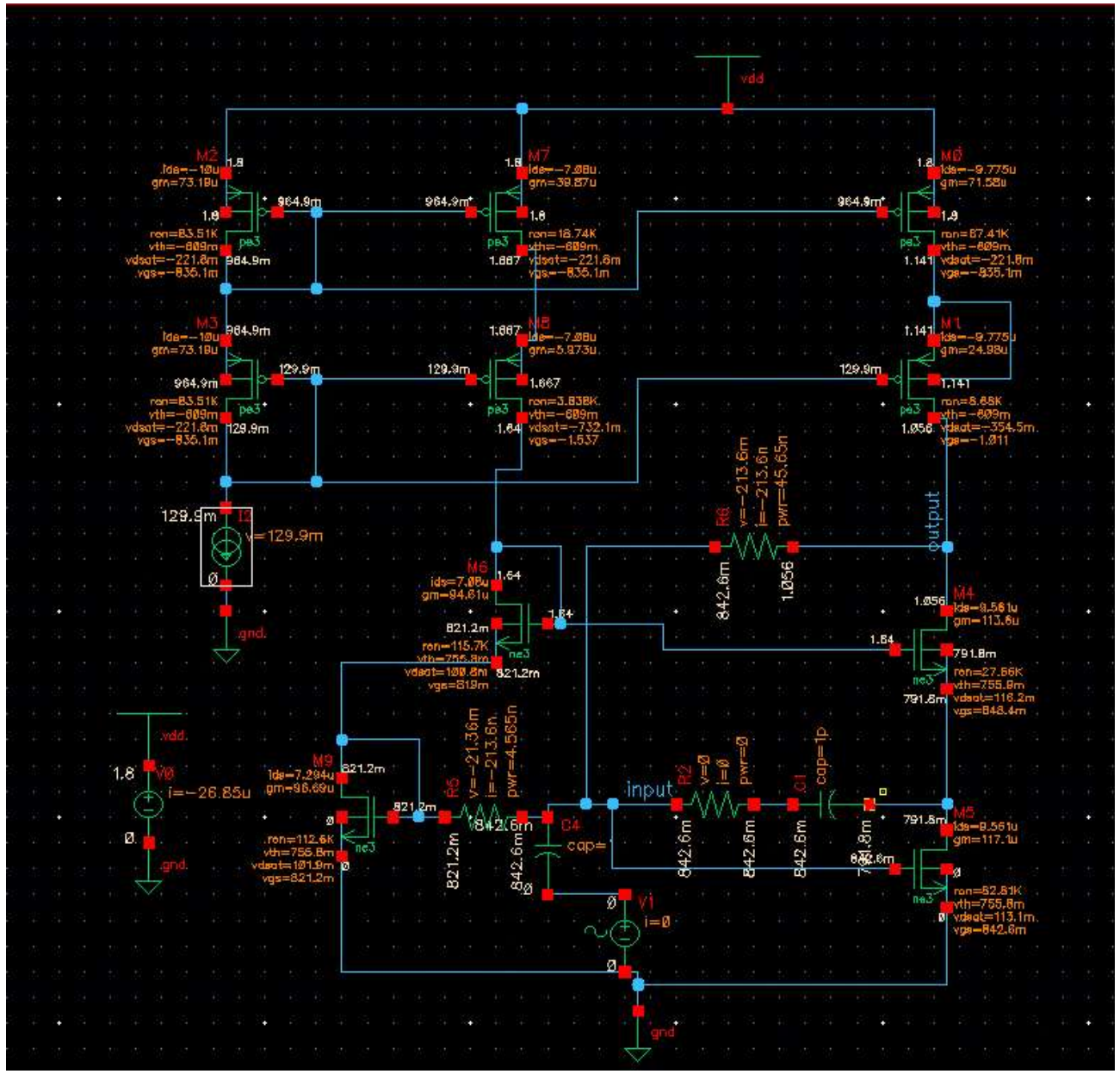
Parameter	Value
ID	40uA
gm	655.1uS

Cascode Amplifiers : cascode current source Input noise curve with increased gm



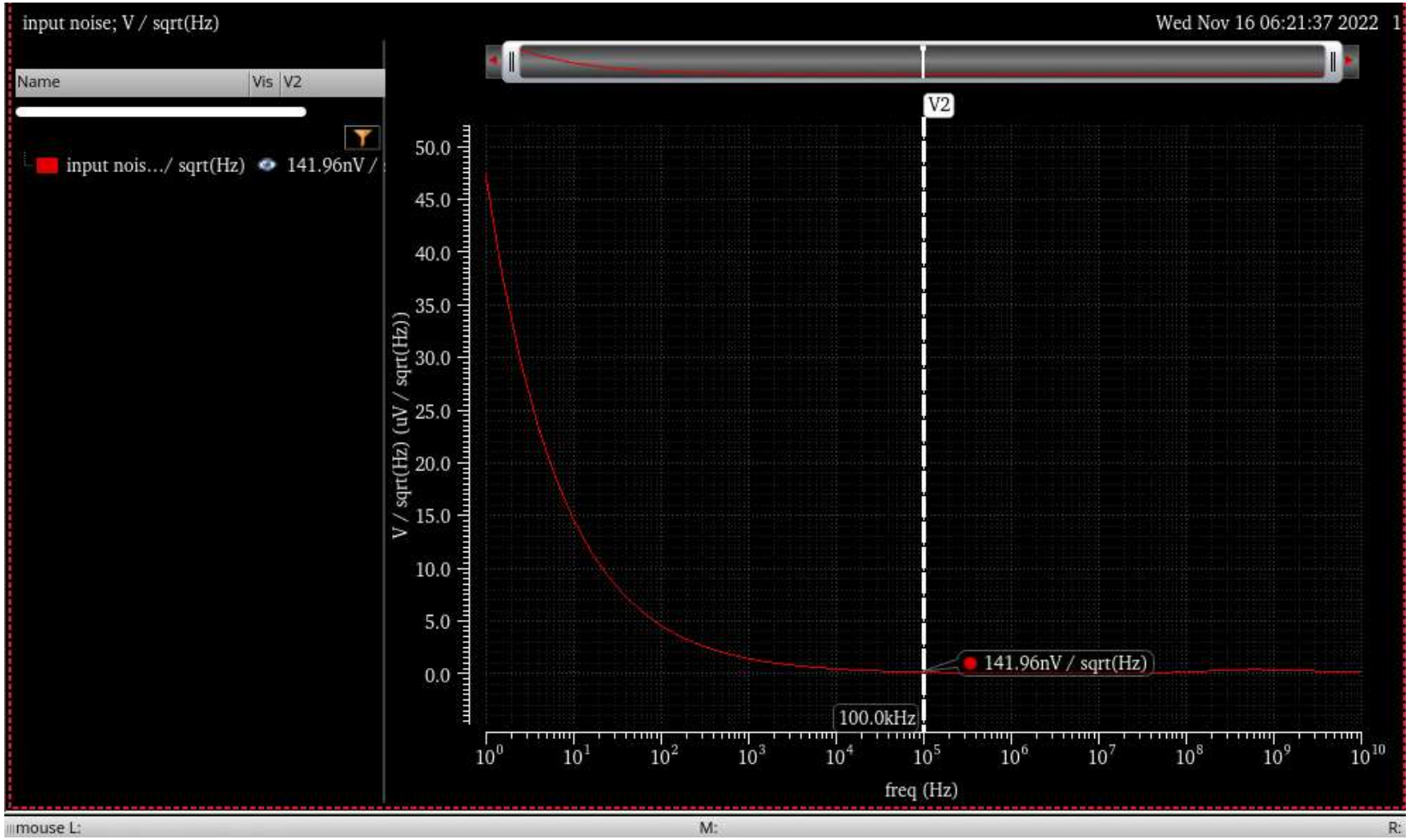
Parameter	Value
IRN	63.33nV/sqrt(Hz)

Cascode Amplifiers : Full cascode



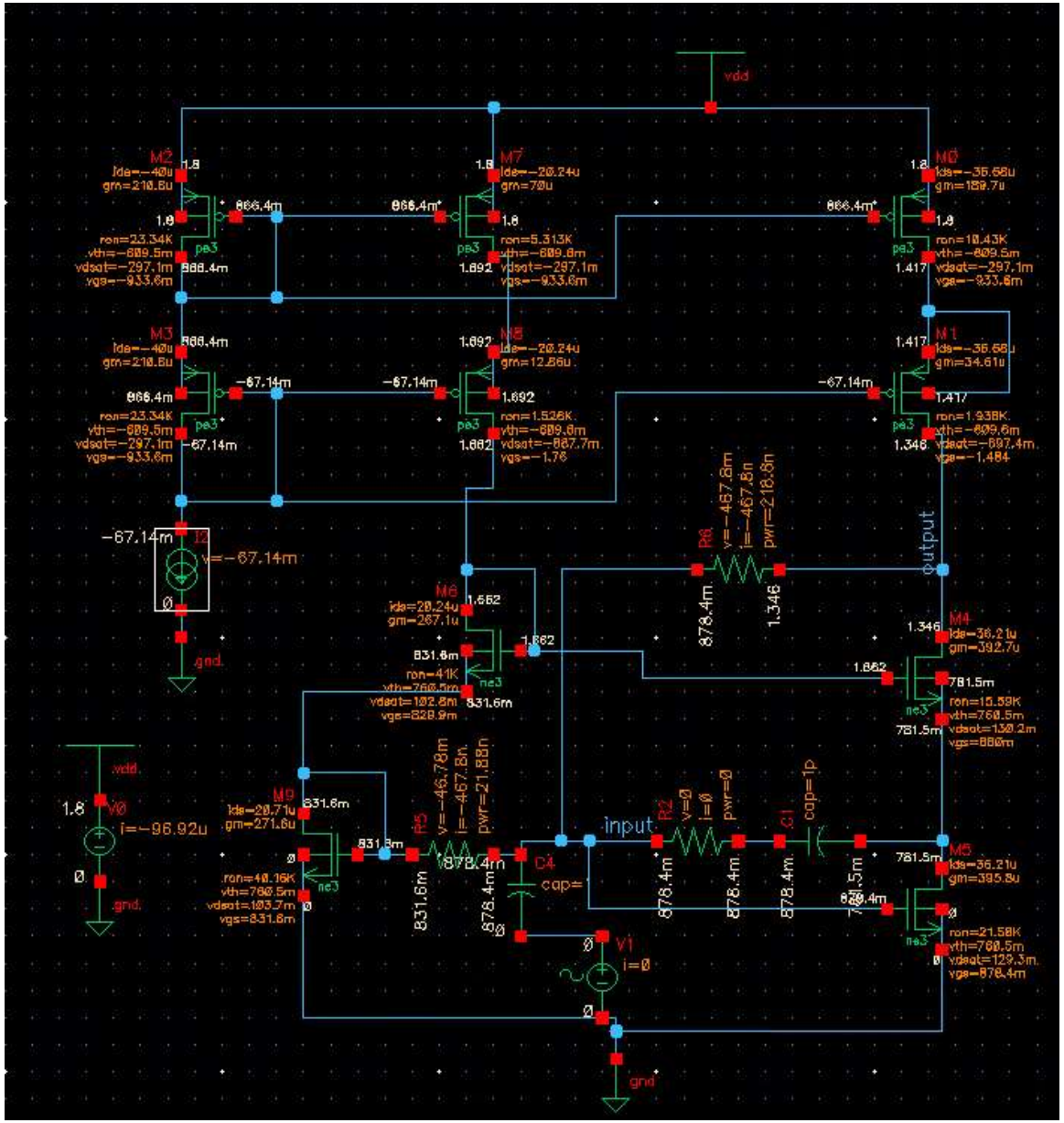
Parameter	Value
ID	10uA
gm	117.1uS

Cascode Amplifiers : Full cascode Input noise curve



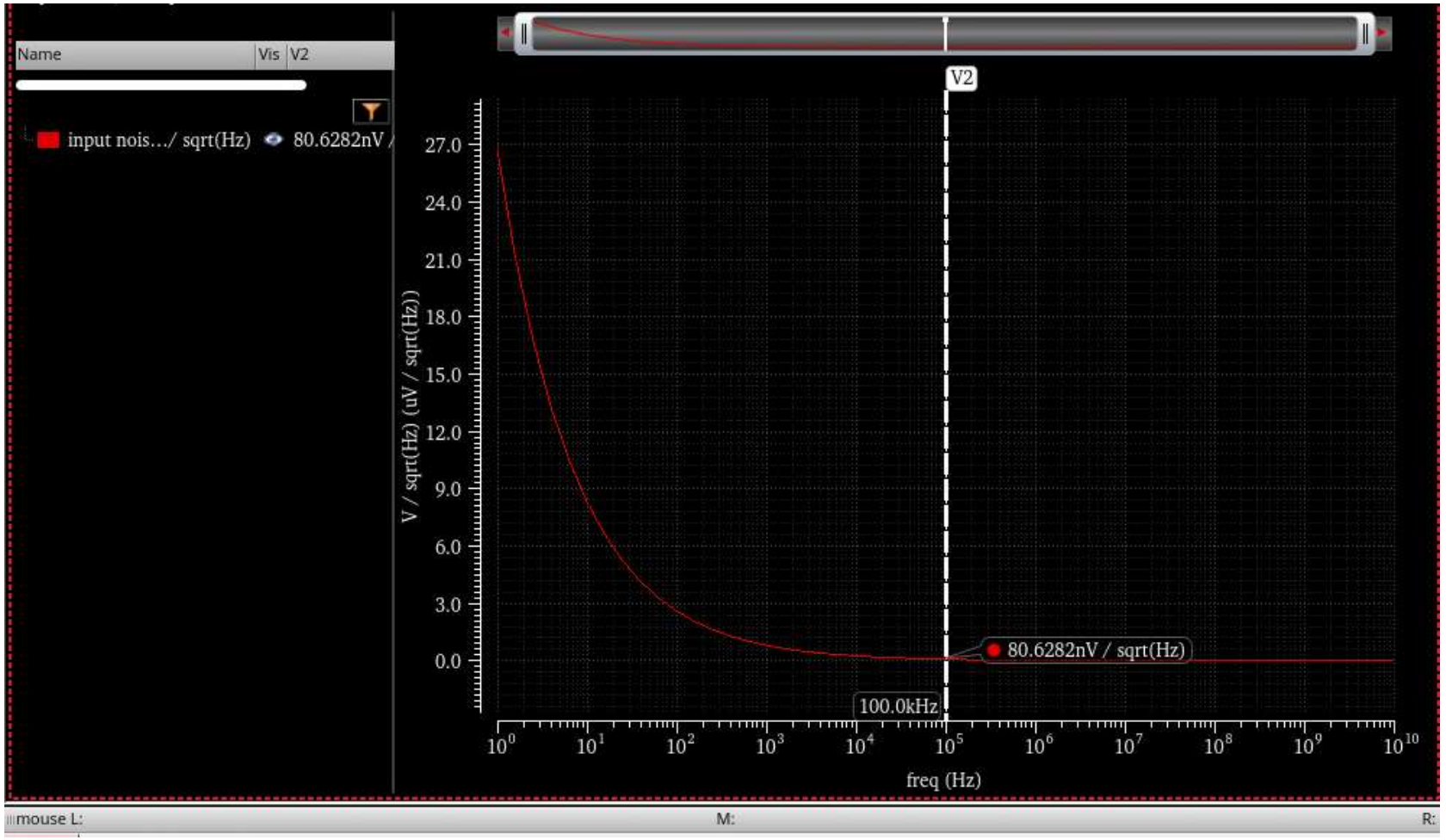
Parameter	Value
IRN	141.96nV/sqrt(Hz)

Cascode Amplifiers : Full cascode increased gm



Parameter	Value
ID	40uA
gm	395.8uS

Cascode Amplifiers : Full cascode input noise curve with increased gm



Parameter	Value
IRN	80.628nV/sqrt(Hz)

Summary of Noise Performance of the amplifiers

Amplifier	ID (uA)	Gm (uS)	IRN (nV/sqrt-Hz)
CS with Ideal current source load	10	93.33	184.43
CS with Ideal current source load	50	381.2	76.01
CS with PMOS load	10	202	48.307
CD with PMOS load	1	14.86	78.82
CD with PMOS load	14.97	19.1	52.269
CG with R load	920k= 3.58	6.766	129.51
CG with R load	165k= 16.81	54.29	250.49
CG with current source load	3.58	56.79	154.024
CG with current source load	10	120	136.0
Cascode-half	10	136.2u	140.994
Cascode-half	40	655.1	63.33
Cascode - Full	10	117.1	141.96
Cascode- Full	40	395.8	80.628

Reference

- CMOS Circuit Design, Layout and Simulation - R. Jacob Baker
- Design of Analog CMOS Integrated Circuits - Behzad Razavi
- CMOS Analog Circuit Design - Douglas R. Holberg and Phillip E. Allen