FAT-Pointer based range addresses

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The increasing disparity between application workloads and the capacity of Translation Lookaside Buffers (TLB) has prompted researchers to explore innovative solutions to mitigate this gap. One such approach involves leveraging physically contiguous memory to optimize TLB utilization. Concurrently, advancements in hardware-level system security, exemplified by the Capability Hardware Enhanced RISC Instructions (CHERI) architecture, offer additional opportunities for improving memory management and security.

CHERI introduces capability-based addressing, a novel approach that enhances system security by associating capabilities with memory pointers. These capabilities restrict access to memory regions, thereby fortifying the system against various security threats. Importantly, the mechanisms implemented in CHERI for enforcing memory protection can also serve as accelerators for standard user-space memory allocators. By leveraging capability-based addressing, memory allocators can efficiently manage memory resources while ensuring robust security measures are in place.

CCS Concepts: • **Do Not Use This Code → Generate the Correct Terms for Your Paper**; *Generate the Correct Terms for Your Paper*; Generate the Correct Terms for Your Paper; Generate the Correct Terms for Your Paper.

Additional Key Words and Phrases: Do, Not, Us, This, Code, Put, the, Correct, Terms, for, Your, Paper

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1 RELATED WORK

Efficient memory management, particularly in the context of Translation Lookaside Buffer (TLB) optimization, has been a focal point of research and development within computer architecture. Various techniques have been proposed to mitigate TLB-related bottlenecks and improve overall system performance.

1.1 Huge Pages

This is used to map a very large region of memory to a single entry. This small/large region of memory is physically contiguous. Most implementations of huge pages are size aligned, For example for the x86 architecture the huge pages size are 4KB, 2MB and 1GB pages.

1.2 Segment

A segment can be viewed as mapping between contiguous virtual memory and contiguous physical memory. The property of a segment allows it to be larger than a page. Direct Segment <paper reference> allows the user to set a single segment for an application. Two registers are added to mark the start and end of the segment. Any virtual address within this region can be translated by adding the fixed offset between the virtual and physical address.

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1.3 RMM

RMM introduces the concept of adding an additional range table. For large allocations RMM eagerly allocates contiguous physical pages. The following allocations creates large memory ranges that are both virtually and physically contiguous. RMM builds on the concept of Direct segment <paper reference> by adding offset to translate a virtual address to physical address. RMM compares address with range boundaries to decide which range it belongs to. RMM queries the range table ofter an L1 TLB miss.

1.4 FlexPointer

FlexPointer is based on the RMM<paper reference RMM> paper. FlexPointer does eagerly allocate pages which are physically contiguous and stores the ID to translate a virtual address to physical address on the remaining unused bits on the 64 bit virtual address. The paper contribution mentions shifting the TLB lookup to an earlier stage to improve latency of accessing the TLB entries. FlexPointer immediate queries the range TLB for translations rather than the RMM paper which waits for the L1 TLB miss.

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