Akila Karunanayake

Department of Computer Engineering, University of Peradeniya, Sri Lanka 20400

🤳 +94 77-45216548 👿 e17154@eng.pdn.ac.lk 🛗 linkedin.com/in/Akila 👩 https://github.com/Akilax0

Interests

• Embedded Systems

• Computer Architecture

• Machine Automation

• Computer Vision

Education

University of Peradeniya

Undergraduate in B.Sc. Engineering(Hons.) Computer Engineering

Nov. 2018 - Present GPA 3.71/4.00

Trinity College Kandy

Jan. 2004 – August 2017

District Rank - 59, National Rank - 831

Relevant Coursework

G.C.E. Advanced Level Examination

• Embedded Systems

• Computer Architecture

- Compilers
- Data Structures
- Software Methodology
- Operating Systems

- Algorithms
- Image Processing

Experience

STERNX | https://www.sternxengineering.com/

Junior Software Engineer

- Developed front end for the company depicting the services and blog posts of the employees.
- Utilized Javascript frameworks, HTML, CSS to allow updates on external sites to be displayed on the relevent site .

Department of Computer Engineering

Spring 2020 - Present

May 2020 - Present

Volunteer Developer and Maintainer

- Development and maintainance of the following department sites.
 - * https://projects.ce.pdn.ac.lk/ongoing-projects/
- Project Cordinator for 40+ undergraduates working on different development projects.

Projects

Autonomous Landmine Detector | C++, Python, AWS, Selenium

Jun 2021 - Present

- Developed an autonomous bot controlled by an ESP32 to scan a given area for landmines using electro-magnetic methods and display results on a webapp.
- Created a back-end using AWS services to store parameters used in each turn and its results.
- Technologies: ESPIDF, MQTT, I2C, SPI.
- Github: https://github.com/cepdnaclk/e17-3yp-Landmine-Detector
- Autonomous Path Planning
 - * Implementation of path finding algorithms for autonomous navigation.
 - * Github: https://github.com/Akilax0/Autonomous-Path-Planning

Multi-Processor System-on-Chip(MPSoC) | FPGA, C

Feb 2022

- Used FPGA design tools to create MPSoc with shared memory to share data between the processors.
- Extended communication to dedicated hardware FIFO queue for better performance.
- Github: https://github.com/Akilax0/FPGA_CO503/tree/main/Lab3

CRC using customized NiosII processor | FPGA, C

Feb 2022

- Improved performance of Cyclic-Redundancy-Check algorithm by adding a custom instruction to the MIPS ISA of NiosII processor.
- Implementation of hardware functionality using XOR and shift operations.
- Github: https://github.com/Akilax0/FPGA_CO503/tree/main/Lab2

Analysis Tool for Industrial Images | Open CV , Automation

Feb 2022 - Present

- Created a tool to analyze performance of an image processing algorithm used to detect deformities in an industrial molding machine.
- Dashboard and API was created to visualize the results.
- Technologies: OpenCV, React, ExpressJS, WebSocket.
- $\bullet \ \ Github: https://github.com/cepdnaclk/e17-co328-Analysis-Tool-for-Industrial-Images$

Compiler for Cool Language | COOL, C++

Feb 2022

- The combination of a lexer, parser, semantic analyser, and code generator that can be used to compile programs written in Cool programming language.
- Github: https://github.com/Akilax0/assignments

Vehicle Number Plate Analyzer | Image Processing, OCR

Feb 2022

- Created Tool to analyze CCTV captured images and recognize number plates of vehicles.
- Classical image processing techniques were used to remove noise and scale the raw images such as super resolution, histogram analysis, Fourier domain analysis.
- Optical character recognition used to extract information from the resulting images.
- Report: https://drive.google.com/file/d/14ejy8Z_6T3mxUF3Oj9dBymhuGgTtWvGL/view?usp=sharing

8-bit processor | Verilog, ARM assembly

October 2020

- Designed 8-bit ALU with a register file for memory using Verilog.
- Simulated processor behaviour using Icarus Verilog and input and output signals were observed using GTKWave.
- Tested behaviour using ARM assembly code.
- Github: https://github.com/Akilax0/FPGA_CO503/tree/main/CO224

Fractal generator $\mid Java$

October 2020

- A tool to display Mandelbrot and Julia sets, for given parameters.
- Use of multi-threading concepts in generating the images.
- Github: https://github.com/Akilax0/Fractal-Generator

Image Processing techniques to detect damaged fruit | Python, OpenCV

November 2019

- Image Filtering with OpenCV was used to create an algorithm to detect the deformities of fruit .
- Created application using python to continuously monitor given set of images .

Competitions

1st Runner up of MoraXtreme 6.0 (of 180+ teams)

Oct.2021

 $12\ hour\ competitive\ programming\ competition\ for\ university\ undergraduates\ in\ Sri\ Lanka.$

208th world rank of IEEEXtreme 15.0 (of 5500+ global teams)

Oct.2021

24 hour competitive programming competition for university undergraduates worldwide.

5th place at IESL UIY

2021

Undergraduate innnovator of the Year competition organized by IESL for undergraduates of Sri Lanka

Jaffna Coders Competitive Programming Competition

2019

Entered the Final 20 teams out of 100+ teams

Top 20 country rank of Google Code Jam, Hash Code, Kick Start, ACES Coders

2019-2020

Certificates and Courses

Classical Cryptosystems and Core Concepts — University of Colarado System

May.2020

Introduction to CyberSecurity Tools & Cyber Attacks— IBM

May.2020

Technical Skills

Languages
Developer Tools
Technologies/Frameworks

C++,C,Verilog HDL,Python,Java, HTML/CSS, JavaScript ESP-IDF, Quartus, AWS, Android Studio Linux, GitHub, Jekyll

Extracurricular

Teaching Git & Github Fundamentals with Hackers' Club for all undergraduates

2021

Workshop to introduce basic developer skills

• Slides: https://drive.google.com/drive/folders/18zGvksfkHTUNqcctLs4e_blR5jXdUOgL?usp=sharing

Member of the Web Consultation team of University of Peradeniya

2021- Present

Group focused on improving university's digital presence

Swarm Robotics group

2021- Present

Documentation of the existing project

References

Prof. Roshan G. Ragel | roshanr@eng.pdn.ac.lk

Head of Department, Department of Computer Engineering, Faculty of Engineering, University of Peradeniya, Sri Lanka

Dr. Isuru Nawinne | isurunawinne@eng.pdn.ac.lk

Senior Lecturer, Department of Computer Engineering, Faculty of Engineering, University of Peradeniya, Sri Lanka