Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO221: Digital Design | Lab 08

Deadline - 17/08/2020

In this lab, you are supposed to implement a 4 bit up counter that increments at the **falling edge (negative edge)** of the clock pulse using Verilog. The counter should have an asynchronous clear. Do the implementation by following the given steps below.

The file named ***counter.v*** has the **testbed** required to test your module. Implement the module called *rippleCounter4,* which is the 4-bit counter in the same file. Use the provided ***exp_output.txt*** to test your module (check if your module produces the output given in this file).

1. Implement an SR latch using basic logic gates.
2. Implement a gated D latch using the SR latch.
3. Implement a master slave D flip flop using the gated D latch (negative edge triggered).
4. Implement a T flip-flop using the D flip-flop.
5. Implement the counter using T flip flops.

Hint: To implement the asynchronous reset implement an SR latch with asynchronous reset.

Thoroughly test the output of your implementation with the given reference output. Then rename *counter.v* to ***E17XXX_counter.v*** where XXX is your **3 digit** E-number. Finally upload **ONLY** that .v file to the link in FEeLS.

Since we do auto marking not following these instructions will result in a penalty of 10%. Also plagiarism will result in 0 marks for the lab.

Make sure you put appropriate comments in your code.