CO503 : Practical 2 - Processor Customizations

In this practical, you will use FPGA design tools to create a System-on-Chip with a customized NiosII Processor. The customization will be done in order to improve the performance of modulo-2 division operation in Cyclic-Redudancy-Check (CRC) algorithm, which is commonly used in network devices.

Tasks:

1. Add a custom instruction to the existing MIPS ISA of the NiosII processor, for performing the modulo-2 division.
2. Implement the required hardware functionality to support the custom instruction, using XOR and shift operations.
3. Use the newly added custom instruction in the CRC algorithm, and compare its performance against pure software implementations.