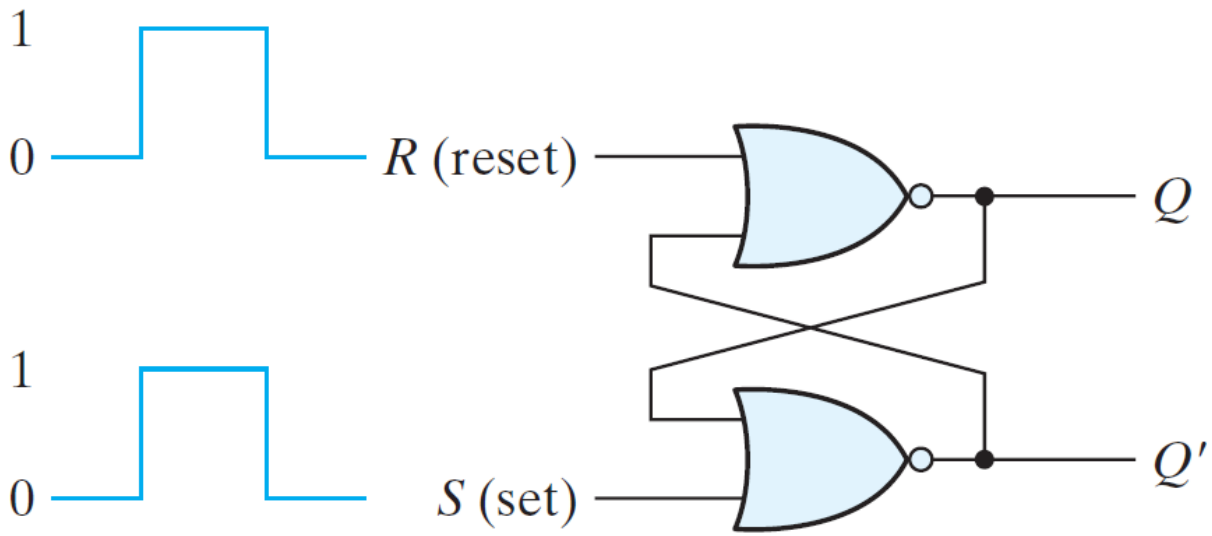
CO221 – Digital Design

LAB 8

SR latch with NOR gates

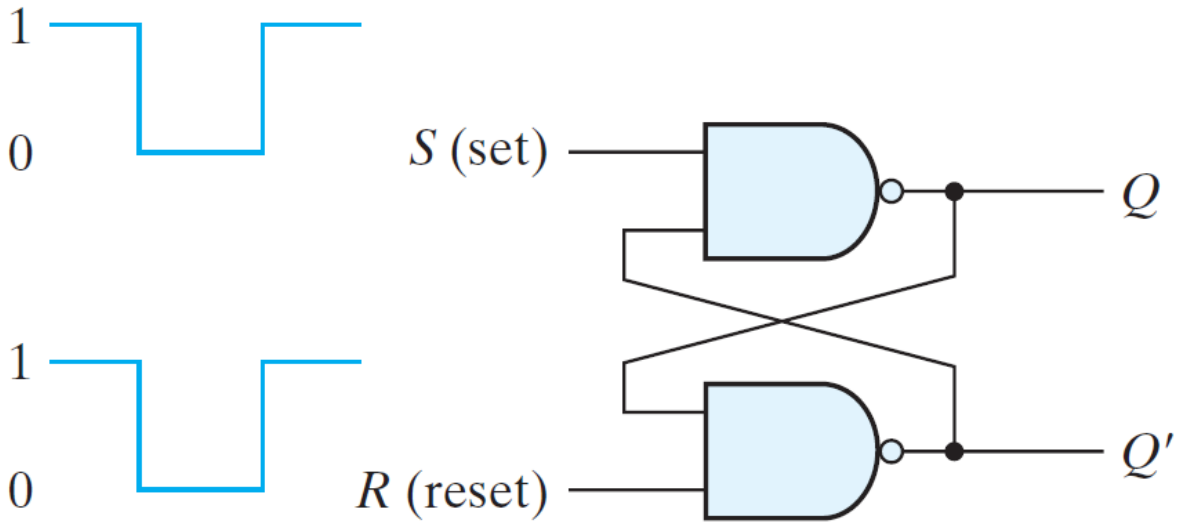


(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

(b) Function table

SR latch with NAND gates

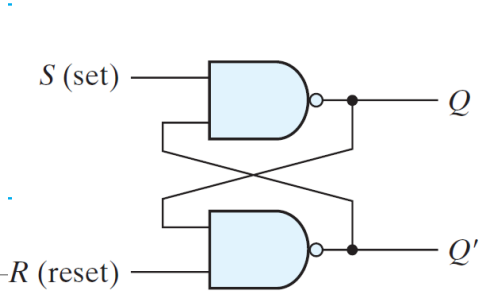


(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

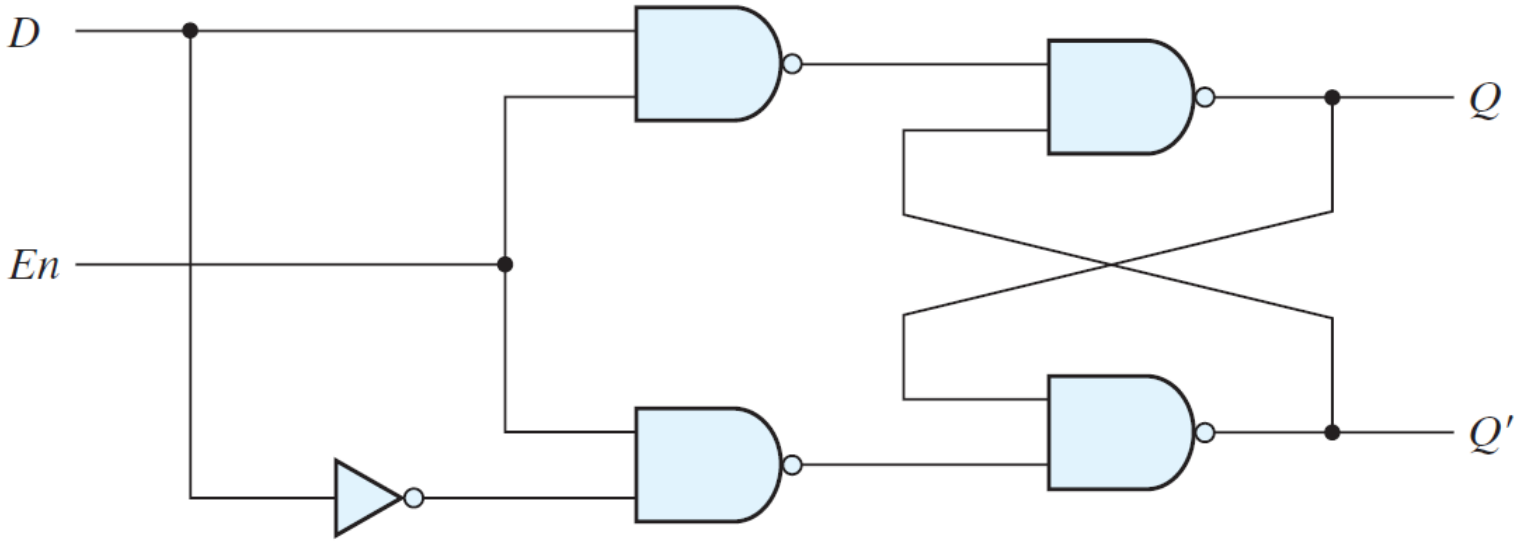
D latch (gated)



(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

(b) Function table

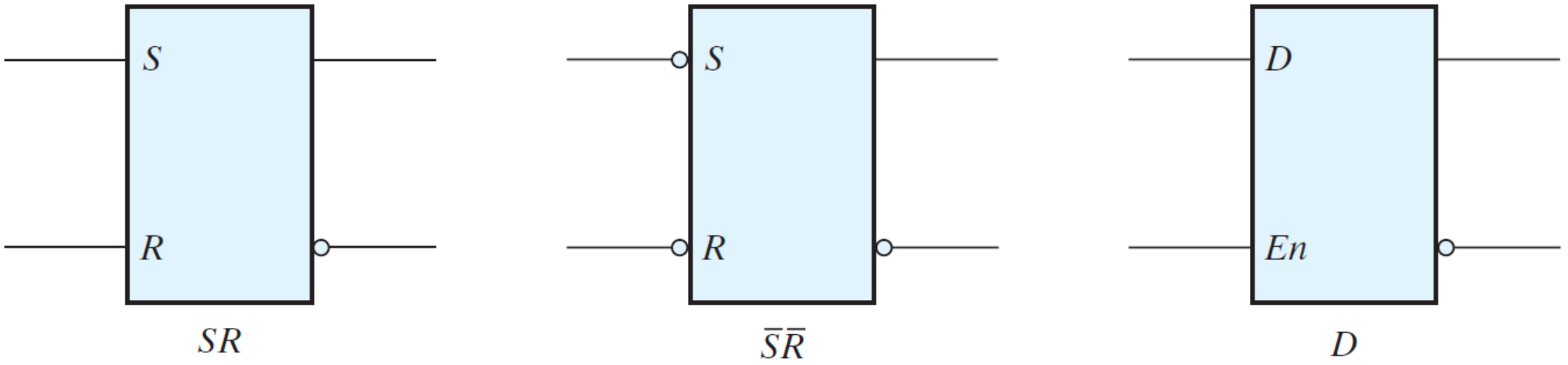


(a) Logic diagram

En	D	Next state of Q
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

Graphic symbols for latches



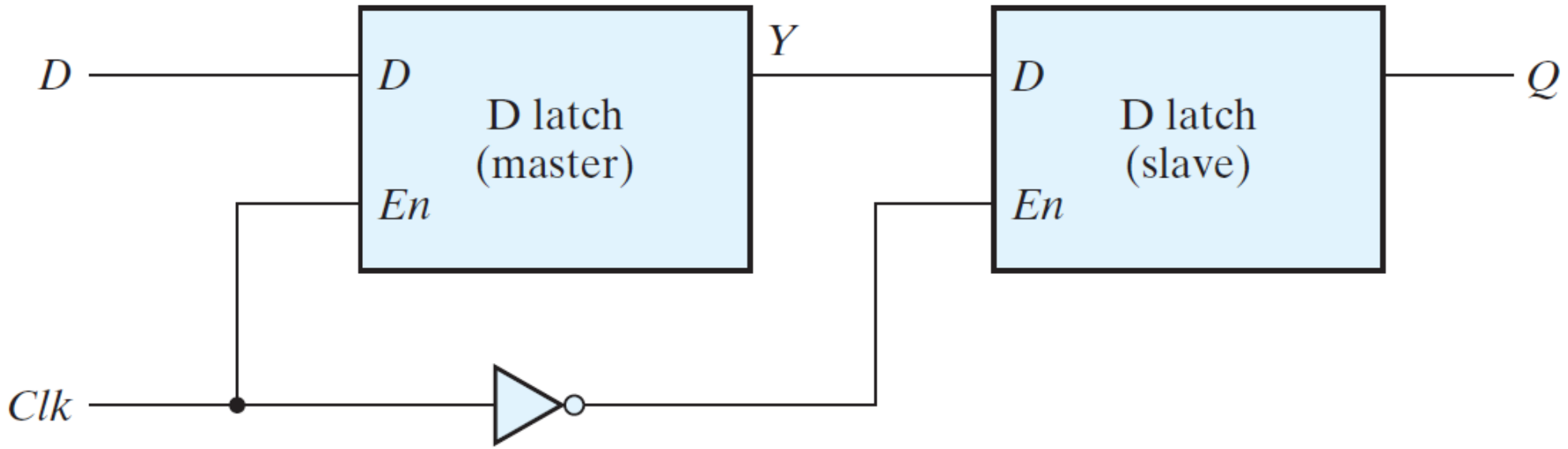
Clock response in latch and flip-flop

(a) Response to positive level

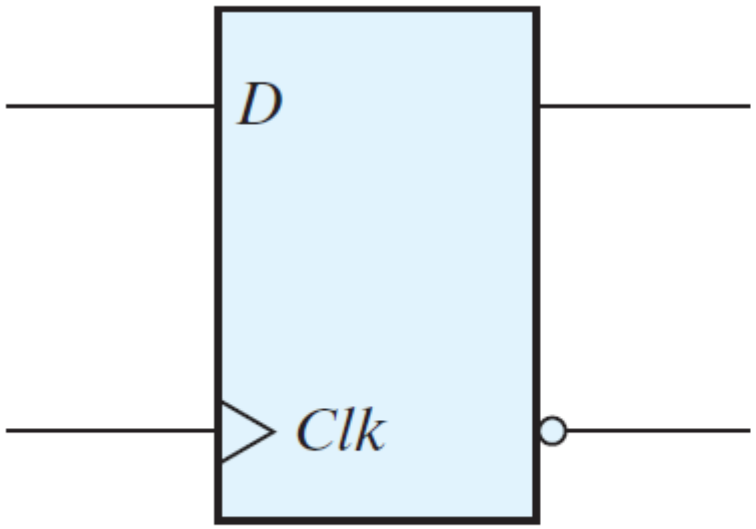
(b) Positive-edge response

(c) Negative-edge response

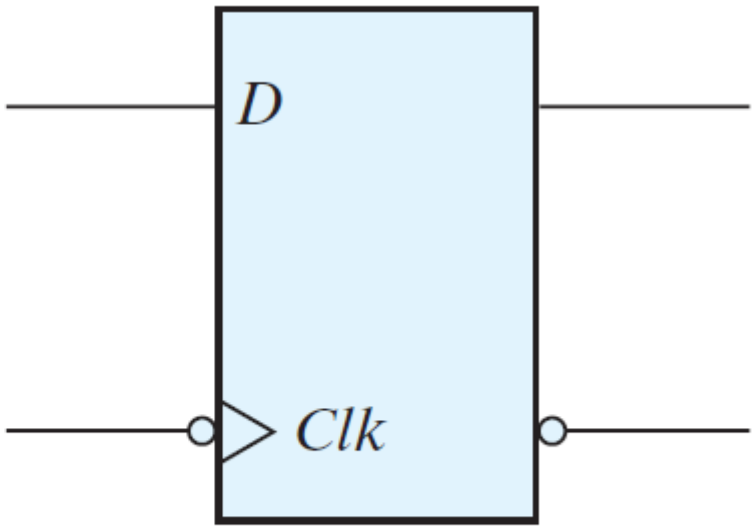
Master–slave D flip-flop



Graphic symbol for edge-triggered D flip-flop



(a) Positive-edge

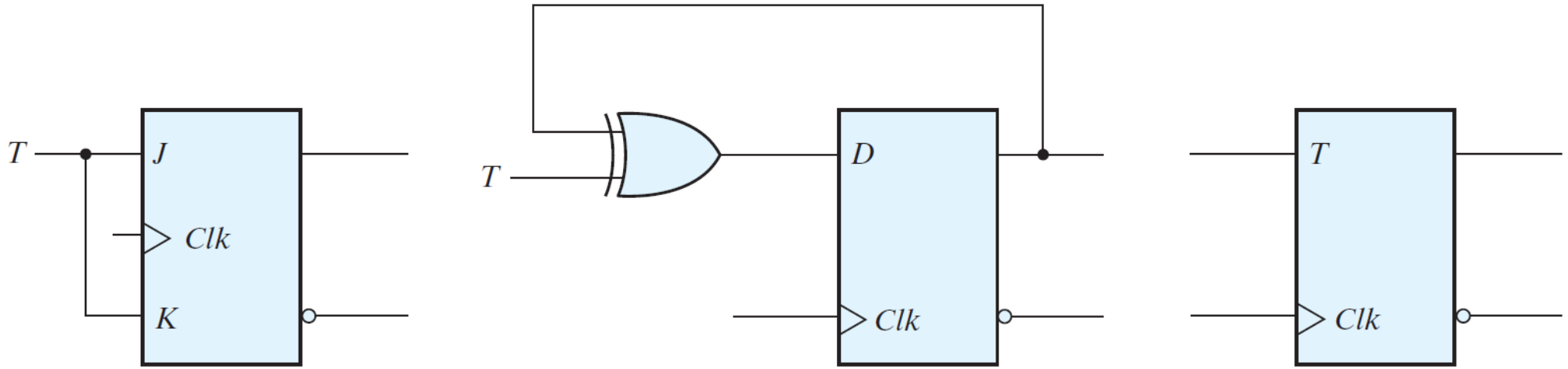


(a) Negative-edge

T Flip-Flop

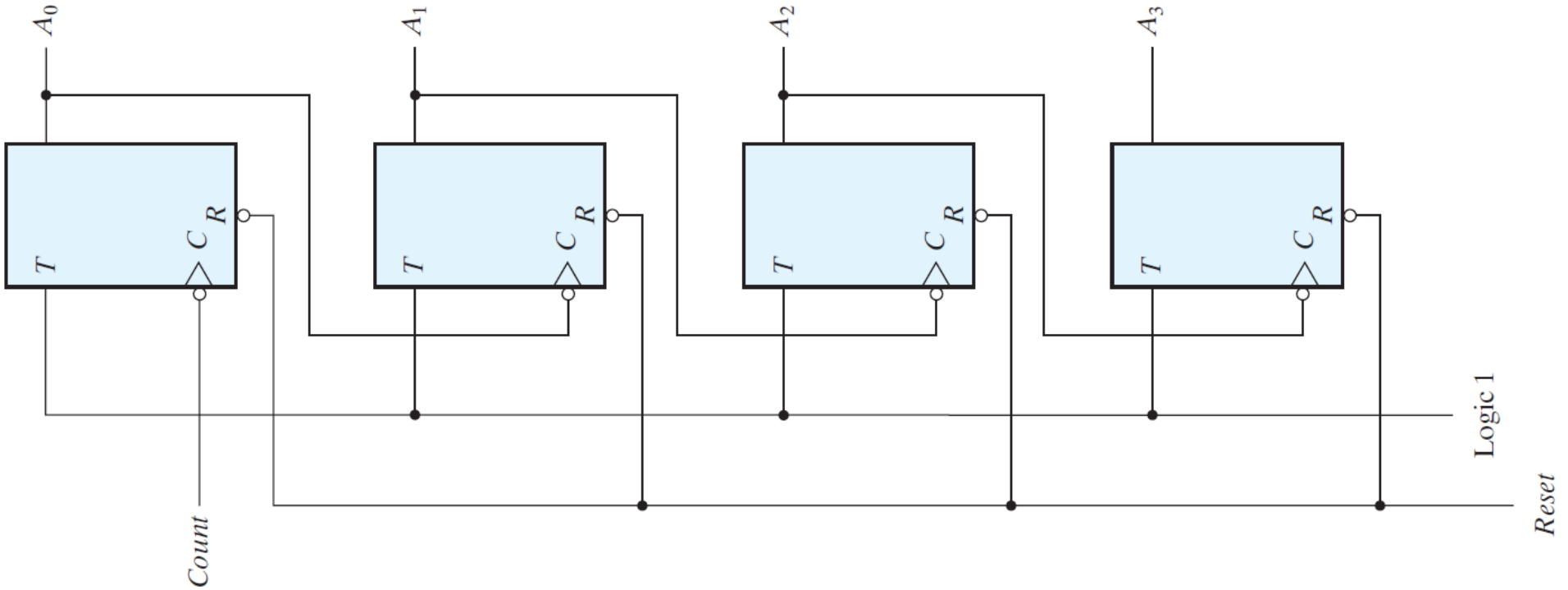
T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

4-bit binary ripple counter



Asynchronous set and reset