CO503: Practical 1 – System-on-Chip (SoC) Design

E/17/154

1/02/2022

Part 1: First SoC - LED Counter

Description:

Simple SoC to display increasing count on a set of LEDs.

Components:

1. Clock
   Provides clock and reset inputs from the board
2. Onchip_mem
   Used to store code using the onboard memory.
3. Nios 2 processor (CPU)
   32 bit embedded processor designed for altera FPGA s.
4. JTAG UART
   Used to communicate with CPU through USB blaster cable
5. Timer
   For precise time calculations when preparing software calculations.
6. SysID
   Adds a unique ID for the SoC. Usually, to prevent accidental software downloading compiled for a different SoC.
7. PIO
   Parallel I/O interface used to drive 8 LED pin s from theCPU.

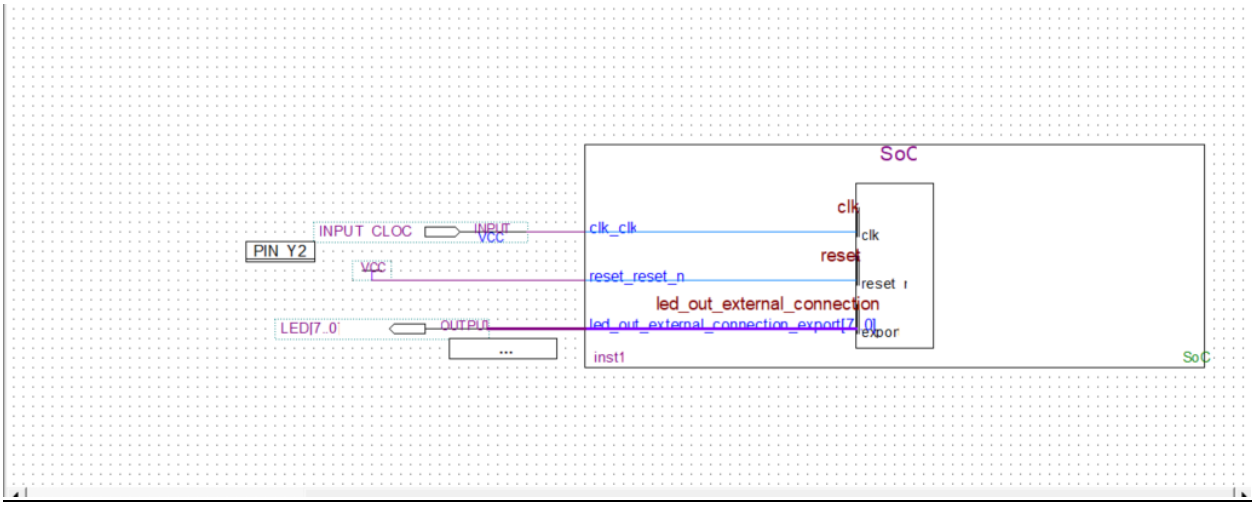

Figure 1: Pin connection of fabrication to display counting LEDs

Software

Provided code edited so the program uses the base address of the PIO to access the LED s. Iterating the loop counts from 0x00 to 0xFF while lighting up relevant LED lights.

Results

The code runs on the FPGA lighting up LED light s from 0x00 to 0xFF with 0.1 second delay in between each change and 1s delay after full light up(0xFF) and reset.

Part 2: JPEG Encoder

Description:

SoC created for JPEG image encoding using the onboard SDRAM as main memory.

Components:

1. SDRAM Controller

   Used to connect to the onboard DRAM chip.

   SDRAM_ADDR[12:0] – 13 bits long address bus
   SDRAM_BA[1:0] – Bank Address
   SDRAM_CAS_N – Column address strobe
   SDRAM_CKE – Clock Enable
   SDRAM_CLK - Clock
   SDRAM_CS_N – Chip Select
   SDRAM_DQ[31:0] – 32bit data
   SDRAM_DQM[3:0] – byte Data Mask
   SDRAM_RAS_N – Row address Strobe
   SDRAM_WE_N – Write Enable

2. Altera PLL (Altera Phase-Locked Loop

   Generates output signal with phase related to phase of input signal.
   For the lab task the input frequency of 50MHz to generate 3 clock signals of
   100MHz with 0 phase shift -> for components (cpu,PIO,JTAG)
   10MHz with 0 phase shift -> for components (Timer,SysID)
   100MHz with -65 phase shift -> for onboard DRAM
   Usually the phase shift doesn't interfere synchronization between components within a system. We use this frequency with negative phase shift to align with DRAM chip. The delay usually gets calculated once a chip is designed for a given data path.

3. Clock Crossing Bridge

   Component used to synchronize data exchange between components running with different clock frequency. In this parts design data from CPU gets delivered to TIMER and SYSID running on 10MHz.

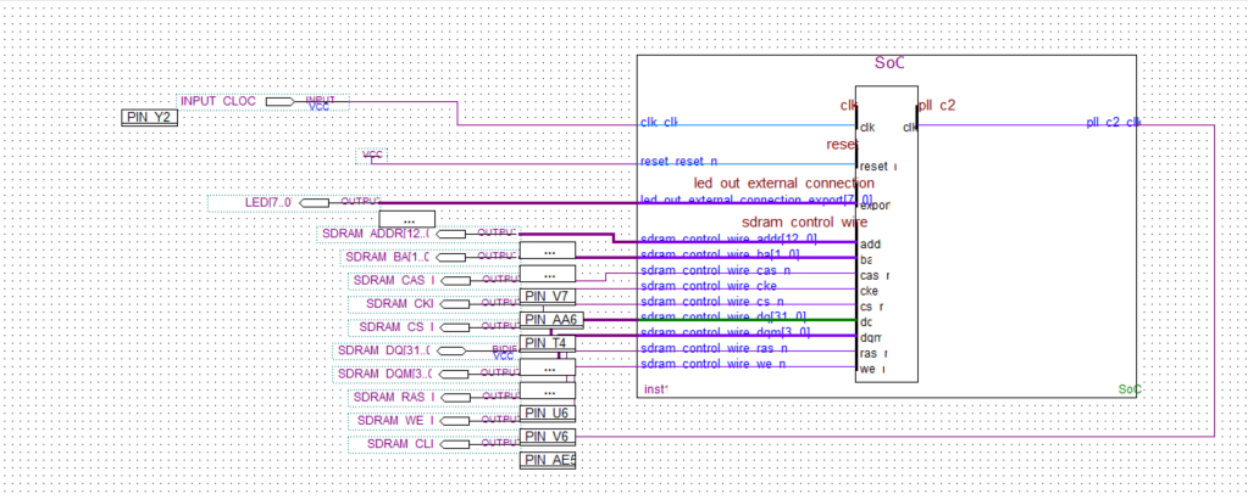

Figure 2: Pin connection of fabrication to encode images from .bmp to .jpg

Software

The code written to encode bmp images to jpeg modified to show LED outputs during process.

Implemented LED indications

- After Checking file format(.bmp) -> 11000000
- After calling convert_picture function (creating destination path) -> 11110000
- After file extract -> 11111100
- At finish and wait -> 11111111

Results

Applying the design and code to the board the encoding of the given set of images is done with the timings given below.

Image	Time after encoding	Time after writing image
Image0.bmp	00.39.18	00.49.35
Image1.bmp	03.30.60	03.55.70
Image2.bmp	00.57.10	01.03.41
Image3.bmp	00.54.44	01.01.14
Image4.bmp	00.13.24	00.18.21
Image5.bmp	00.12.92	00.16.92
Image6.bmp	03.21.07	03.46.96

Table 1: Timings of image encoding

Final Remarks

The Lab acted as an entry way to getting started for FPGA board designs and implementations.

Things gained through the Lab,

a. Introduction to basic components on a SoC
b. SoC designing by using Qsys tool and identifying connections between components
c. Pin mapping to connect fabricated design to onboard ports.

Issues Encountered

Problems occurred when uploading designs and code to board.

➔ Had to figure out that the mode of FPGA board should be set to run

Errors given when running the code as file path not found

➔ The file path /mnt/host/ stands for the project folder and any path assigning should be done relative to it.