ECE 5022 FINAL DESIGN PROJECT

AKINLAWON SOLOMON

Section I: 16-QAM Modulator

[Question 1.1] To create the 16-QAM modulator, a random bit-stream is first passed through a process block which maps the bits into the appropriate symbol mapping, splits the bit stream into I and Q channels, then converts the stream into a corresponding square wave. The resulting square wave is then shaped using a raised cosine filter, modulated using an LO signal, added and then passed on to the transmission channel. A simple diagram illustrating the process is shown below.

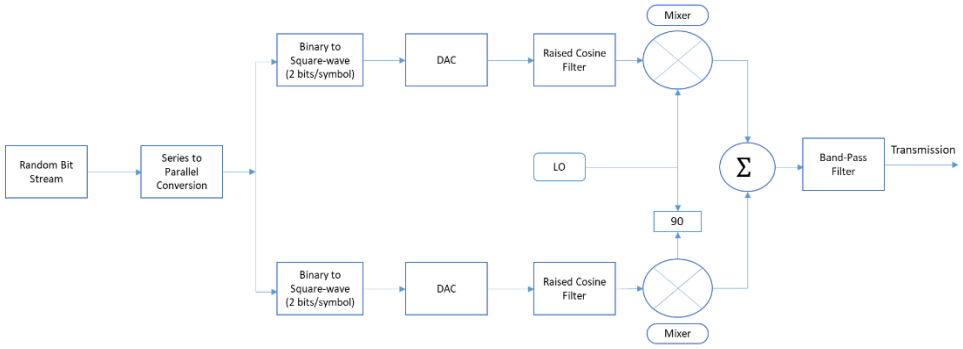


Figure 1. A flowchart depicting 16-QAM Modulation

[Question 1.2] As shown in the figure below, the E_b/N_0 required to obtain a BER of 10^{-5} is about $13.5dB$. Since the number of bits per symbol is 4, using the SNR conversion formula we obtain:

$$SNR_{required} = 10\log_{10}(4) + 13.5dB = 19.7dB$$

[Question 1.3] The bit period, T_b, is equal to the inverse of the bit rate which is 1Mbps. Therefore, $T_b = 1\mu s$. The random data stream is shown below:

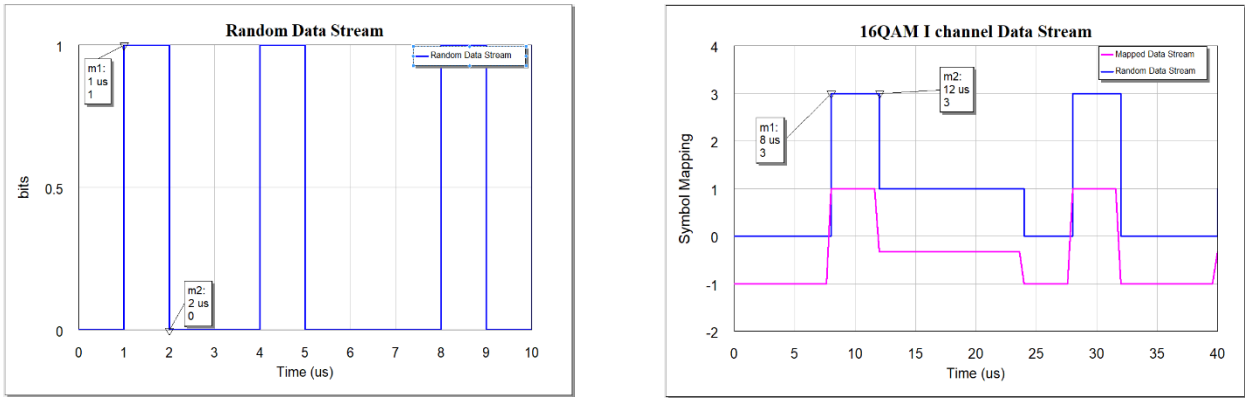


Figure 2. Random Bit Stream of 1's and 0's and the 16-QAM symbol mapping

[Question 1.4] The symbol period, T_s, is defined by the relation:

$$T_S = \frac{bits}{symbol} \times T_b = 4\mu s$$

The plot below depicts the input and output spectrum of the pulse shaping filter. As can be observed in the figure, the main lobe bandwidth is reduced from $0.25MHz$ to $0.1831\ MHz$. This indicates the side-lobes have been suppressed as expected, and the pulse has been shaped accordingly.

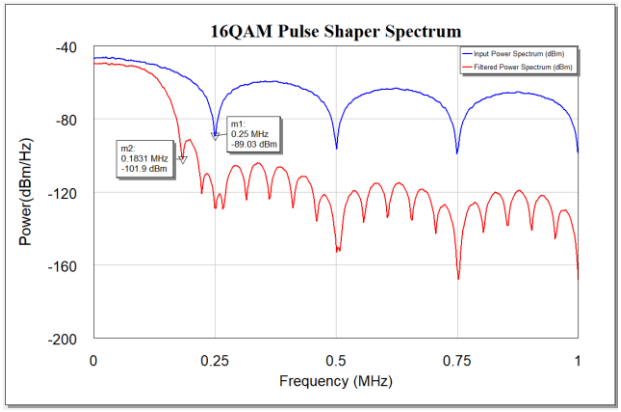


Figure 3. Filtered Power Spectrum using Raised Cosine Filter

[Question 1.5] The roll-off factor used was about 0.35, and this was to ensure that a trade-off between side-lobe reduction and the bandwidth of the pulse-shaped signal. This relation is defined by the equation:

$$B = R_S(1 + R) = 0.25 * 10^6 * (1 + 0.35) = 0.3357MHz$$

As can be observed in the plot above, the resulting main-lobe bandwidth is about $B = (2 \times 0.1831) = 0.3662\ MHz$, which is close to the theoretical result. The bandwidth of the filter was chosen to be approximately $2 * B \approx 0.8MHz$, this was chosen to ensure that the power is more evenly distributed about the center frequency, and to stop lower frequencies in the passband from being attenuated.

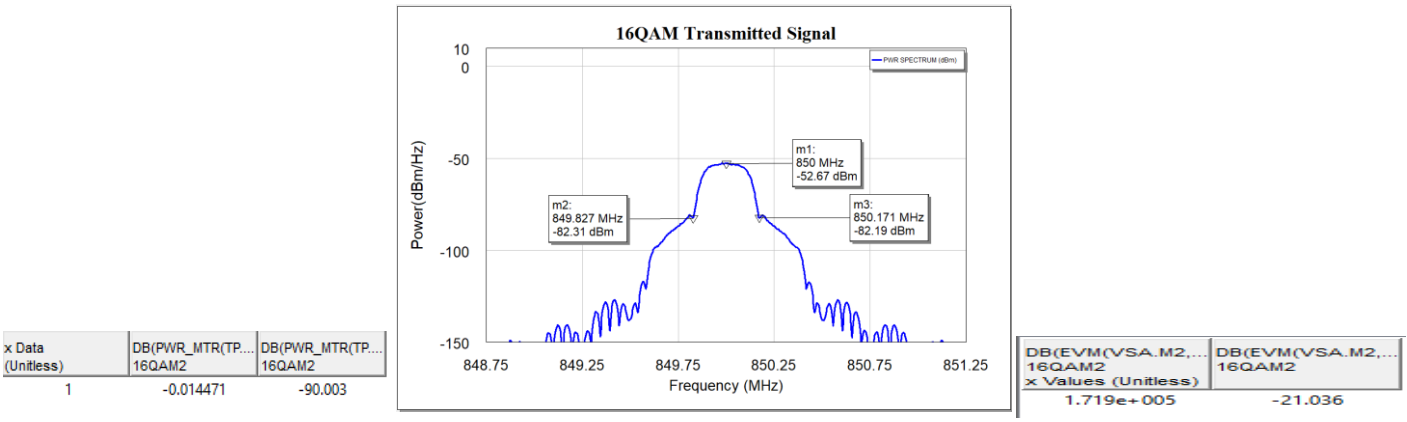


Figure 5. The Transmitted Signal after 16-QAM Modulation before AWGN Channel Loss

[Question 1.6] The spectrum of the transmitted signal is shown above. The loss and bandwidth of the filter were adjusted to ensure that the output power is approximately 0dBm. The $21dB$ SNR was also verified using the VSA analyzer. The power of the signal was also verified using the power meter block.

[Question 1.7] The LNA chosen was the SKY67150-396LF model from Skyworks Inc. This device is an ultra-low noise amplifier with a high-OIP3 of about $39dBm$ which is designed especially for telecommunication recievers, with a bandwidth of $300 - 2200\ MHz$. It has a low noise factor of only 0.23dB, which means that it barely affects the total noise factor of the receiver. The mixer used was the ADL5802 model by Analog Devices. This mixer was chosen because of its high linearity and high LO-RF isolation, with an OIP3 of $30dBm$ and an isolation of 20dB. The PGA amplifier used was the HMC625BPL5E model. This amplifier was used because of the balanced tradoff between a decent gain range of $13 - 18dB$ and a moderately low noise figure of $6dB$. The final datasheets are included at the end of the document.

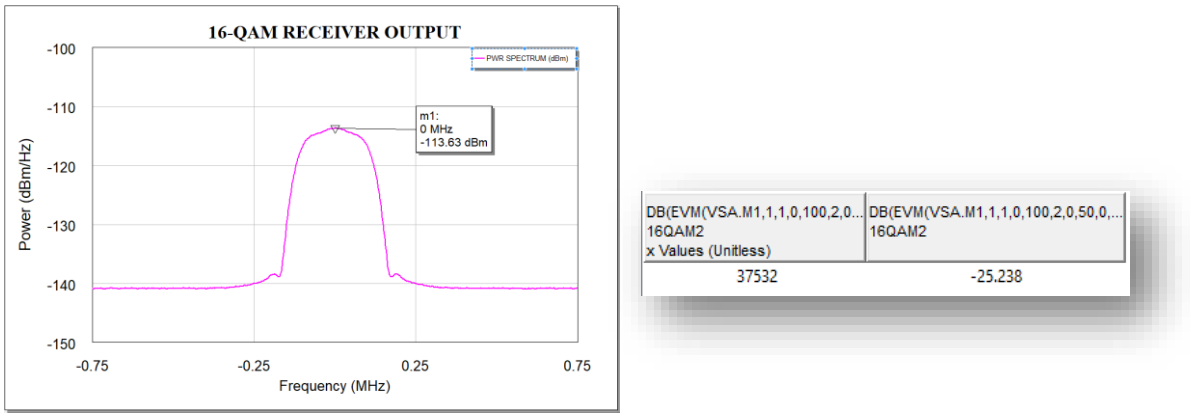


Figure 6. The Power Spectrum of the Received Signal and the corresponding EVM

As specified, AWGN channel noise was included which resulted in a $-90dBm$ signal at the input of the receiver with an SNR of $21dB$. This was done by adjusting the channel loss and at

gain of an attenuator attached to the AWGN block. The confirmed result is shown above using the VSA analyzer. The signal was then passed on to the receiver block. The receiver output spectrum is also shown above. Using the VSA analyzer, the final SNR was obtained to be about 24dB which matches the required BER quite well. The constellation diagram indicating the received and transmitted symbols is shown in Figure. Clearly, we can see that the symbols align fairly well, which indicates that the BER is being met.

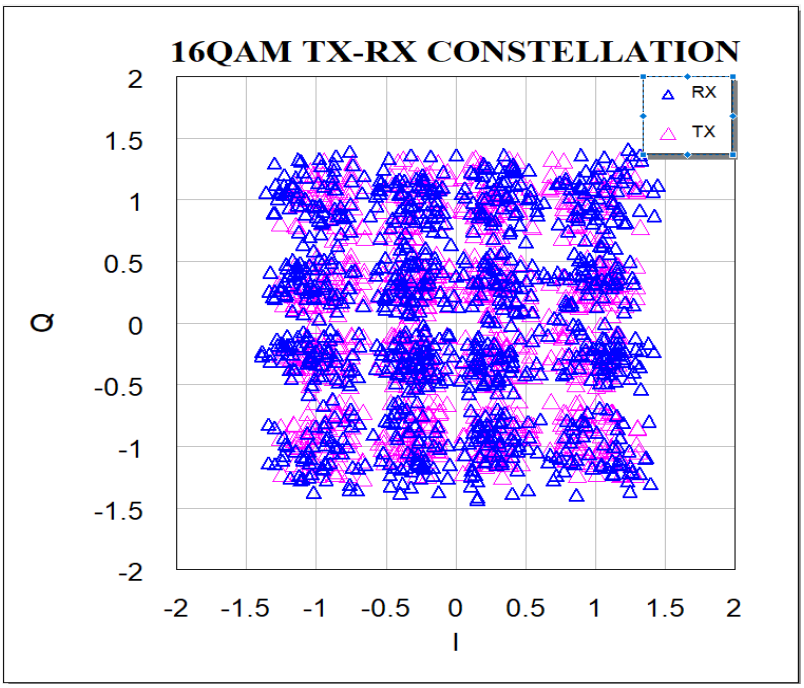


Figure 7. The IQ constellation showing the received and transmitted symbols overlaid

[Question 1.8] The final system diagram is included at the end of the document.

Section II: Designing With Imperfections

B1. Effects of IQ mismatch

[Question 2.1] A $0.5dB$ I/Q amplitude mismatch was included in the I-channel. The SNR changes only slightly to about $24.9dB$, which is a $0.3dB$ drop from the matched case. The constellation diagram is shown below, and we can observe that the BER specification is still met. We would expect that introducing amplitude mismatch may reduce the spacing between the symbols, but there is no significant change in the constellation diagram due to the low value of $0.5dB$.

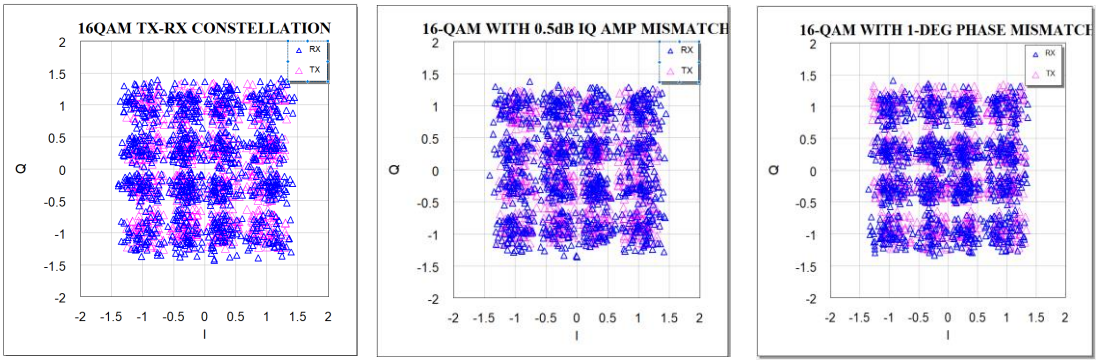


Figure 8. The IQ constellation showing the received and transmitted symbols overlaid; with amplitude mismatch; with phase mismatch

[Question 2.2] A $1.0°$ I/Q phase mismatch was introduced into the system. This caused only a minor drop in the SNR by about $0.18dB$, resulting in a final SNR of about $25.05dB$. The constellation diagram is shown above, and we can observe that the BER specification is still met. There is no significant change in the constellation diagram. We would expect that introducing phase mismatch may cause the entire diagram to rotate (a shear transformation proportional to the mismatch), but there is no significant change in the constellation diagram due to the low value of $1.0°$.

B2. Effects of Phase Noise

[Question 3.1] Phase Noise was added to the LO in the receiver front-end. The filter order was chosen to be a 100 and the resulting constellation diagram is shown below. There is only a slight drop in the SNR, and the BER specification is still being met. However, when the filter order is increased, we can observe significant distortion in the IQ plot. The diagram contracts into a circular shape as expected, and we can observe that the received and transmitted symbols are mis-aligned. A plot showing higher-order filter distortion and corresponding SNR is also shown below.

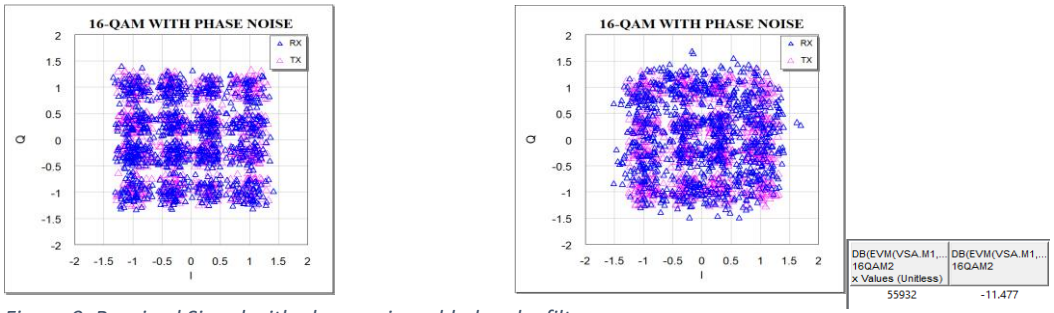


Figure 9. Received Signal with phase noise added and a filter order of 100; filter order increased to a 1000, phase noise more pronounced and the SNR is lowered

B3. System Tolerance

[Question 4.1] The system was tested to observe the maximum amplitude mismatch it could handle. The system was shown to tolerate a 24dB amplitude mismatch with no phase noise and 18dB with phase noise while still meeting the BER/SNR specification.

[Question 4.2] The system was tested to observe the maximum phase mismatch it could handle. The system was shown to tolerate a $93°$ phase mismatch with no phase noise and $90°$ with phase noise while still meeting the BER/SNR specification.

[Question 4.3] A jammer signal, in the form of an $850MHz$ tone, was added to the system. The system was then tested to observe how high the jamming signal could be without violating the SNR specification. The system was shown to tolerate a $-113dBm$ power signal with and without phase noise while still meeting the BER/SNR specification.

B4. System Diagram

[Question 5.1] The final system diagram is shown on the last page.

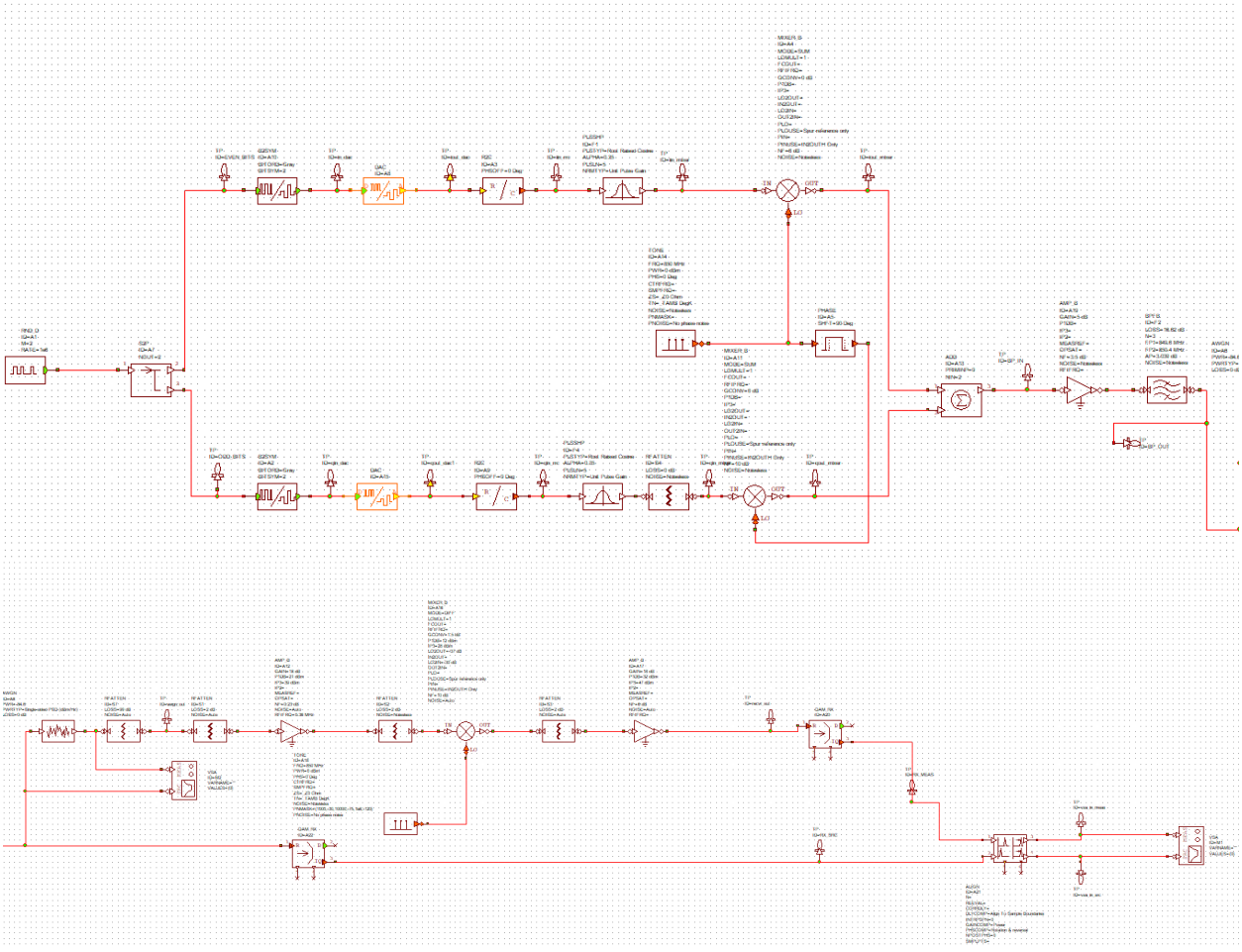


Figure 10. The System Diagram for Part I

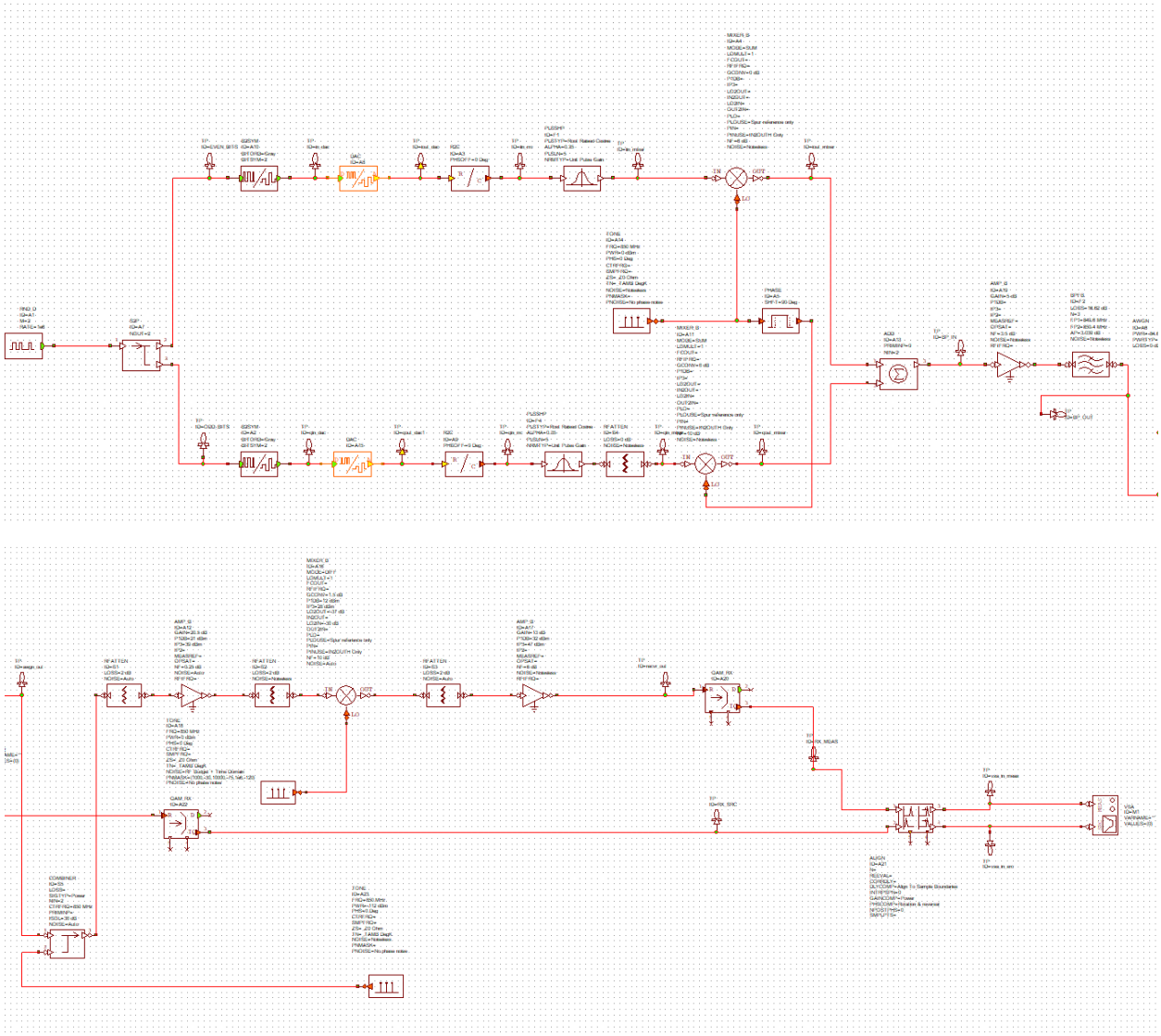


Figure 11. The Final System Diagram

HMC625BLP5E

v02.0616

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 5 GHz

Typical Applications

The HMC625BLP5E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

-13.5 to +18 Gain Control in 0.5 dB Steps

Power-up State Selection

High Output IP3: +32 dBm

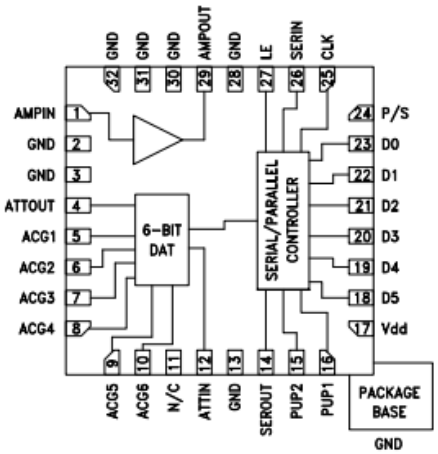
TTL/CMOS Compatible
Serial, Parallel, or latched Parallel Control

±0.25 dB Typical Gain Step Error

Single +5V Supply

32 Lead 5x5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC625BLP5E is a digitally controlled variable gain amplifier which operates from DC to 5 GHz, and can be programmed to provide anywhere from 13.5 dB attenuation, to 18 dB of gain, in 0.5 dB steps. The HMC625BLP5E delivers noise figure of 6 dB in its maximum gain state, with output IP3 of up to +32 dBm in any state. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 6 bit parallel word. The HMC625BLP5E also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC625BLP5E is housed in a RoHS compliant 5x5 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, 50 Ohm System, Vdd= +5V, Vs= +5V

Parameter	Frequency	Min.	Typ.	Max.	Units
Gain (Maximum Gain State)	DC - 3.0 GHz 3.0 - 5.0 GHz	13 5	18 13		dB dB
Gain Control Range			31.5		dB
Input Return Loss	DC - 5.0 GHz		15		dB
Output Return Loss	DC - 5.0 GHz		10		dB
Gain Accuracy: (Referenced to Maximum Gain State) All Gain States	DC - 0.8 GHz 0.8 - 5.0 GHz	± (0.10 + 5% of Gain Setting) Max. ± (0.30 + 3% of Gain Setting) Max.			dB dB
Output Power for 1dB Compression	DC - 3.0 GHz 3.0 - 5.0 GHz	16 13	19 16		dBm dBm
Output Third Order Intercept Point (Two-Tone Output Power= 0 dBm Each Tone, 1 MHz Spacing)	DC - 5.0 GHz		32		dBm
Noise Figure	900 MHz		6		dB
Total Supply Current (Idd + Is)	DC - 5.0 GHz	60	87.5	100	mA

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Dual Channel, High IP3, 100 MHz to 6 GHz Active Mixer

Data Sheet **ADL5802**

FEATURES

- Power conversion gain of 1.6 dB
- Wideband RF, LO, and IF ports
- SSB noise figure of 11 dB
- Input IP3 of 28 dBm
- Input P1dB of 12 dBm
- Typical LO drive of 0 dBm
- Low LO leakage
- Single supply operation: 5 V @ 240 mA
- Exposed paddle, 4 mm × 4 mm, 24-lead LFCSP package

APPLICATIONS

- Cellular base station receivers
- Main and diversity receiver designs
- Radio link downconverters

FUNCTIONAL BLOCK DIAGRAM

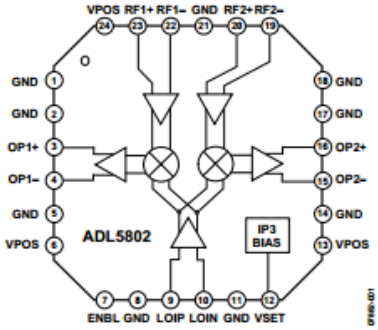


Figure 1.

GENERAL DESCRIPTION

The ADL5802 uses high linearity, double-balanced, active mixer cores with integrated LO buffer amplifiers to provide high dynamic range frequency conversion from 100 MHz to 6 GHz. The mixers benefit from a proprietary linearization architecture that provides enhanced input IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB noise figure, and dc current to be optimized using a single control pin. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. The balanced active mixer arrangement provides superb LO to RF and LO to IF leakage, typically better than −30 dBm.

The IF outputs are designed for a 200 Ω source impedance and provide a typical voltage conversion gain of 7.6 dB when loaded into a 200 Ω load.

The ADL5802 is fabricated using a SiGe high performance IC process. The device is available in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

DATA SHEET

SKY67150-396LF: 300 to 2200 MHz Ultra Low-Noise Amplifier

Applications

- LTE, GSM, WCDMA, HSDPA macro and micro base stations
- UHF and L-band ultra low-noise receivers
- Cellular repeaters, DAS and RRH/RRUs
- High temperature transceiver applications to +105 °C

Features

- Ultra-low Evaluation Board NF of 0.23 dB @ 849 MHz
- High OIP3 performance: +39 dBm
- Adjustable supply current from 20 to 100 mA
- Flexible bias voltage: 3 to 5 V
- Temperature and process-stable active bias
- Miniature DFN (8-pin, 2 x 2 mm) package (MSL1 @ 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

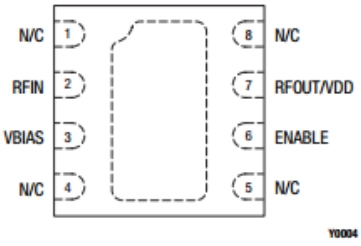


Figure 2. SKY67150-396LF Pinout (Top View)

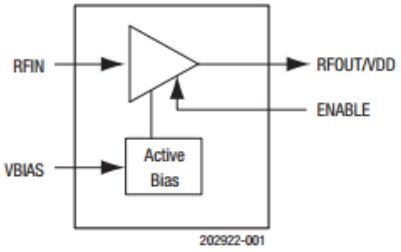


Figure 1. SKY67150-396LF Block Diagram

Description

The SKY67150-396LF is GaAs, pHEMT low-noise amplifier (LNA) with an active bias, high linearity, superior gain, and industry-leading noise figure (NF) performance. The device features Skyworks advanced, pHEMT enhancement mode process in a compact 2 x 2 mm, 8-pin Dual Flat No-Lead (DFN) package.

The internal active bias circuitry provides stable performance over temperature and process variation. The device offers the ability to externally adjust supply current. Supply voltage is applied to the RFOUT/VDD pin through an RF choke inductor. The RFIN and RFOUT/VDD pins should be DC blocked to ensure proper operation.

The SKY67150-396LF operates in the frequency range of 300 to 2200 MHz using a common layout and band-specific tunes. Operation with high gain and a low NF at frequencies as low as 100 MHz is possible with degraded input return loss.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.