CS1050 Computer Organization and Digital Design
Lab 5 — Counter with External Input
210113L
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Introduction

- In this lab, we have to design a 3-bit counter
- the direction of counting is controlled based on an external input.
- When input button is switched off, counter runs clockwise. When it is switched on, we will count runs anticlockwise

Truth Table

T				T+1					
Q2	Q1	Q0	B	Q2	Q1	Q0+	D2	D1	D0
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	1	0	0	1
1	1	1	0	1	1	0	1	1	0
1	1	1	1	0	1	1	0	1	1
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1	0

K-Maps

	Q2 Q1				D0 = Q2'.B' +Q1.B
Q0 B	00	01	11	10	
00	1	X	0	0	
01	0	X	1	0	
11	0	X	1	X	
10	1	1	0	X	

	Q2 Q1				D1 = Q0.B' +B.Q2
Q0 B	00	01	11	10	
00	0	X	0	0	
01	0	X	1	1	
11	0	0	1	X	
10	1	1	1	X	

	Q2 Q1				D1 = Q0.B' +B.Q'
Q0 B	00	01	11	10	
00	0	X	1	0	
01	1	X	1	1	
11	0	0	0	X	
10	0	1	1	X	

D_FF - VHDL

Project Summary | D_FF.vhd

E:/Xilinx/Projects/lab5/lab5.srcs/sources_1/new/D_FF.vhd

```
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity D_FF is
35      Port ( D : in STD_LOGIC;
36             Res : in STD_LOGIC;
37             Clk : in STD_LOGIC;
38             Q : out STD_LOGIC;
39             QBar : out STD_LOGIC);
40  end D_FF;
41
42  architecture Behavioral of D_FF is
43  begin
44      process (Clk) begin
45          if (rising_edge (Clk)) then --Check for rising-edge of clock pulse
46              if Res = '1' then       --Clear output if reset zs high
47                  Q<='0';
48                  QBar<='1';
49              else                    --Else output same as input
50                  Q<=D;
51                  QBar<=not D;
52              end if;
53          end if;
54      end process;
55  end Behavioral;
56
```

D_FF_Sim - VHDL

Project Summary | D_FF.vhd

E:/Xilinx/Projects/lab5/lab5.srcs/sources_1/new/D_FF.vhd

```
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35      Port ( D : in STD_LOGIC;
36             Res : in STD_LOGIC;
37             Clk : in STD_LOGIC;
38             Q : out STD_LOGIC;
39             QBar : out STD_LOGIC);
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42  architecture Behavioral of D_FF is
43  begin
44      process (Clk) begin
45          if (rising_edge (Clk)) then --Check for rising-edge of clock pulse
46              if Res = '1' then       --Clear output if reset is high
47                  Q<='0';
48                  QBar<='1';
49              else                    --Else output same as input
50                  Q<=D;
51                  QBar<=not D;
52              end if;
53          end if;
54      end process;
55  end Behavioral;
56
```
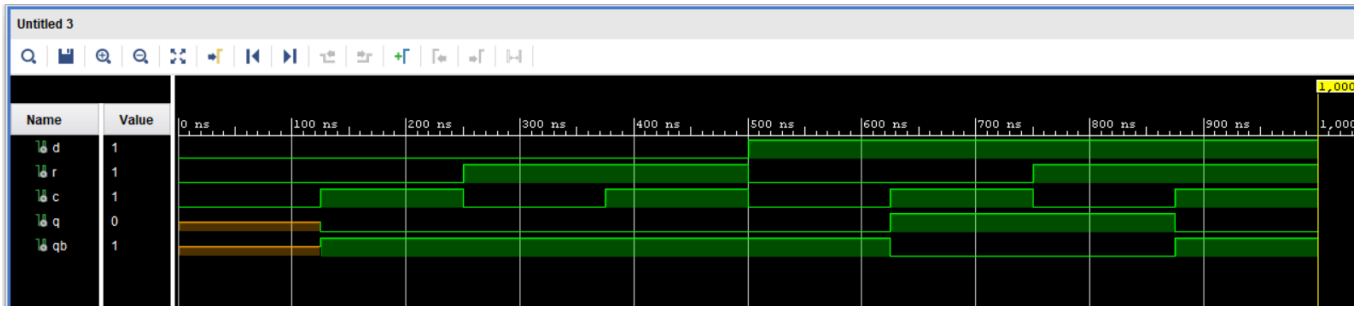

D_FF_Sim - Time


Untitled 3
Name
Value
d
1
r
1
c
1
q
0
qb
1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns

Clk_Slow - VHDL

D_FF.vhd | Counter.vhd | Slow_Clk.vhd | D_FF_Sim.vhd | Slow_Clk_Sim.vhd *

E:/Xilinx/Projects/lab5/lab5.srcs/sources_1/new/Slow_Clk.vhd

```
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Slow_Clk is
35      Port ( Clk_in : in STD_LOGIC;
36             Clk_out : out STD_LOGIC);
37  end Slow_Clk;
38
39  architecture Behavioral of Slow_Clk is
40
41  signal count :  integer:=1;
42  signal clk_status : std_logic :='0';
43
44  begin
45      process (Clk_in) begin
46          if(rising_edge(clk_in)) then
47              count<=count+1;
48              if (count=10) then
49                  clk_status<=not clk_status;
50                  Clk_out<=clk_status;
51                  count<=1;
52              end if;
53          end if;
54      end process;
55
56  end Behavioral;
57
```

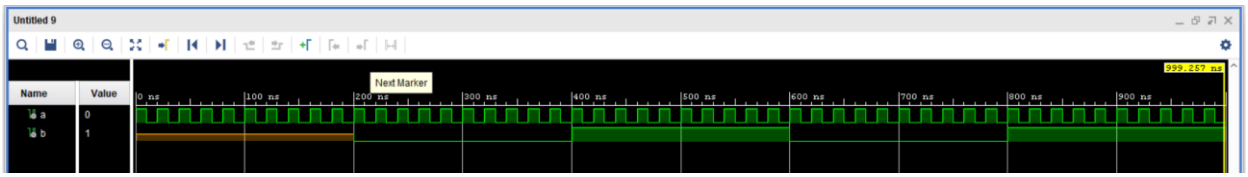
Clk_Slow_Sim - VHDL

D_FF.vhd | Counter.vhd | Slow_Clk.vhd | D_FF_Sim.vhd | **Slow_Clk_Sim.vhd *** | Counter_Sim.vhd

E:/Xilinx/Projects/lab5/lab5.srcs/sim_1/new/Slow_Clk_Sim.vhd

```
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Slow_Clk_Sim is
35  --  Port ( );
36  end Slow_Clk_Sim;
37
38  architecture Behavioral of Slow_Clk_Sim is
39
40  COMPONENT Slow_Clk PORT
41  (Clk_in : in STD_LOGIC;
42  Clk_out : out STD_LOGIC);
43  END COMPONENT;
44   SIGNAL a,b:std_logic;
45
46  begin
47
48  UUT:Slow_Clk PORT MAP(
49  Clk_in =>a,
50  Clk_out=>b
51  );
52
53  process
54  begin
55
56  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
57  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
58  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
59  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
60  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
61
62  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
63  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
64  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
65  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
66  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
67
68  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
69  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
70  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
71  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
72  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
73
74  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
75  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
76  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns;
77  a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns;
78  a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT FOR 10 ns; a<='1';WAIT FOR 10 ns; a<='0';WAIT;
79  end process;
80
81  end Behavioral;
```

Clk_Slow - Time



Counter - VHDL

Counter.vhd

E:/Xilinx/Projects/lab5/lab5.srcs/sources_1/new/Counter.vhd

```
20
21
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Counter is
35      Port ( Dir : in STD_LOGIC;
36             Res : in STD_LOGIC;
37             Clk : in STD_LOGIC;
38             Q : out STD_LOGIC_VECTOR (2 downto 0));
39  end Counter;
40
41  architecture Behavioral of Counter is
42  component D_FF
43   port (
44   D : in STD_LOGIC;
45   Res: in STD_LOGIC;
46   Clk : in STD_LOGIC;
47   Q : out STD_LOGIC;
48   Qbar : out STD_LOGIC);
49  end component;
50
51  component Slow_Clk
52   port (
53   Clk_in : in STD_LOGIC;
54   Clk_out: out STD_LOGIC);
55  end component;
56
57  signal D0, D1, D2 : std_logic;
58  signal Q0, Q1, Q2 : std_logic; -- Internal signals
59  signal Clk_slow : std_logic;
60
61  begin
62   Slow_Clk0 : Slow_Clk
63   port map (
64   Clk_in => Clk,
65   Clk_out => Clk_slow);
66
67   D0 <= ((not Q2) and (not Dir)) or (Q1 and Dir);
68   D1 <= (Q0 and not Dir)or(Q2 and Dir);
69   D2 <= (not Q0 and Dir)or(Q1 and not dir);
70
71   D_FF0 : D_FF
72   port map (
73   D => D0,
74   Res => Res,
75   Clk => Clk_slow,
76   Q => Q0);
77
78   D_FF1 : D_FF port map (
79   D => D1,
80   Res => Res,
81   Clk => Clk_slow,
82   Q => Q1);
83
84   D_FF2 : D_FF port map (
85   D => D2,
86   Res => Res,
87   Clk => Clk_slow,
88   Q => Q2 );
89
90   Q(0) <= Q0;
91   Q(1) <= Q1;
92   Q(2) <= Q2;
93
94  end Behavioral;
```

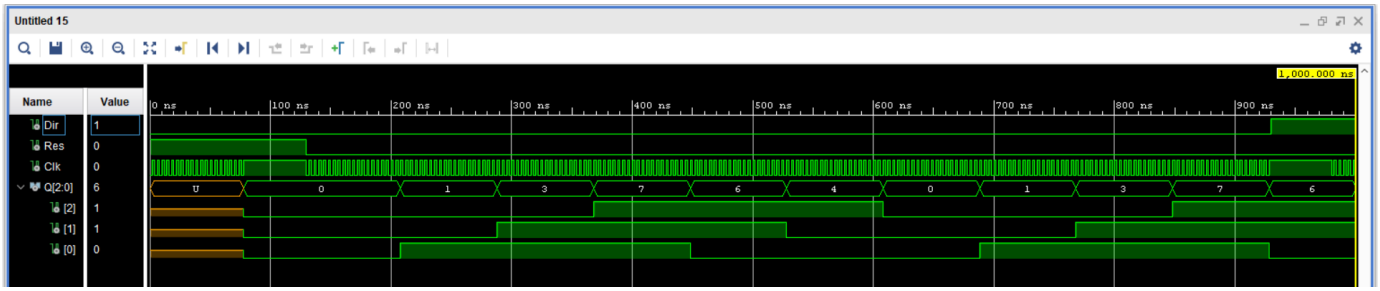
Counter_Sim - VHDL

D_FF.vhd | Slow_Clk.vhd | D_FF_Sim.vhd | Slow_Clk_Sim.vhd | **Counter_Sim.vhd**

E:/Xilinx/Projects/lab5/lab5.srcs/sim_1/new/Counter_Sim.vhd

```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Counter_Sim is
35  --  Port ( );
36  end Counter_Sim;
37
38  architecture Behavioral of Counter_Sim is
39
40  COMPONENT Counter PORT
41  ( Dir,Res,Clk : in STD_LOGIC;
42  Q : out STD_LOGIC_VECTOR (2 downto 0));
43  END COMPONENT;
44
45  SIGNAL Dir,Res,Clk : std_logic;
46  SIGNAL Q : std_logic_vector(2 downto 0);
47  begin
48  UUT: Counter PORT MAP(
49  Dir => Dir,
50  Res => Res,
51  Clk => Clk,
52  Q=>Q
53  );
54  process
55   begin
56   Dir <= '0';
57   Res <= '1';
58   for i in 1 to 20 loop
59   Clk <= '0';
60   WAIT FOR 2 ns;
61   Clk <= '1';
62   WAIT FOR 2 ns;
63   end loop;
64   WAIT FOR 50 ns;
65   Res <= '0';
66   for i in 1 to 200 loop
67   Clk <= '0';
68   WAIT FOR 2 ns;
69   Clk <= '1';
70   WAIT FOR 2 ns;
71   end loop;
72   Dir <= '1';
73   WAIT FOR 50 ns;
74   for i in 1 to 200 loop
75   Clk <= '0';
76   WAIT FOR 2 ns;
77   Clk <= '1';
78   WAIT FOR 2 ns;
79   end loop;
80   WAIT;
81
82  end process;
83  end Behavioral;
```

Counter - Time



Conclusion

- The 3-bit counter is built using relatively simple component such as D flip flops and combinational logic circuits. This shows hierarchical design.
- The inbuilt clock of basys board is used is to give the clock signal for the logic unit.
- In VHDL we can define how a circuit should behave more abstractly. This is known as VHDL Behavioral Modelling. It allows us to use high-level programming constructs such as variables, conditions, procedures and loops in our code.