参考資料

TI Designs: TIDA-00915
200V ACサーボ・ドライブ用、高PWM周波数動作、三相GaNインバータのリファレンス・デザイン

概要

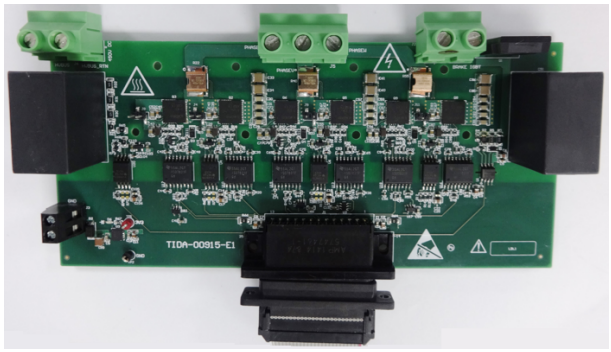
TIDA-00915デザインは、200V ACサーボ・モータを2kW$_{PEAK}$で駆動するための三相インバータです。600V、12AのLMG3410窒化ガリウム(GaN)パワー・モジュールが搭載され、FETおよびゲート・ドライバが内蔵されています。GaN FETはシリコンFETよりもはるかに高速にスイッチング可能で、さらにドライバが同じパッケージに統合されているため、寄生インダクタンスが減少し、スイッチング性能が最適化されて電力損失が減少することにより、設計者はヒートシンクのサイズを小さくできます。この容積削減は、小型のサーボ・ドライブやモータ内蔵ドライブに利益があります。インバータは100kHzの高いスイッチング周波数で動作するため、電流リップルが減少し、低インダクタンスのモータとともに使用するときトルク・リップルが改善されます。これによって、位置制御アプリケーションの性能が向上します。

リソース

TIDA-00915	デザイン・フォルダ
LMG3410	プロダクト・フォルダ
ISO7831	プロダクト・フォルダ
LM3840	プロダクト・フォルダ
TLV1117-33	プロダクト・フォルダ
SN74AHC1G08	プロダクト・フォルダ
SN74LVC1G11	プロダクト・フォルダ
AMC1306	プロダクト・フォルダ
TMDSCNCD28379D	ツール・フォルダ

TI E2E™ Community

E2Eエキスパートに質問

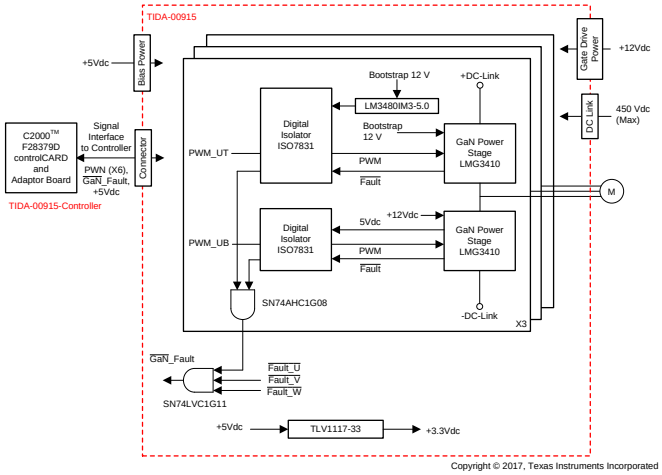


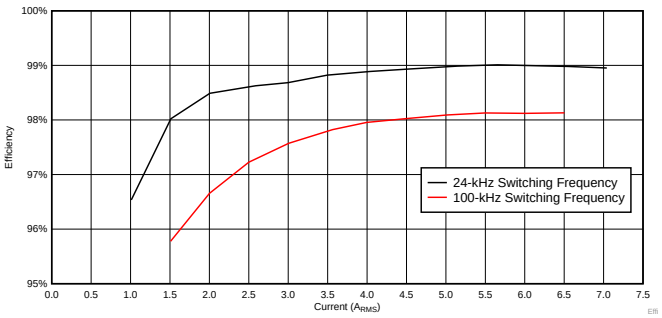
特長

- 高いPWMスイッチング周波数(最高100kHz)により、低インダクタンスのモータを最小の電流リップルで駆動
- 600V、12AのLMG3410 GaNモジュールと内蔵のFETおよびゲート・ドライバにより、PCBの外形が小さくなり、レイアウトの複雑性が低減
- 非常に高速なスイッチング遷移(25ns未満)で、スイッチ・ノード電圧リンギングがないため、EMIが低減
- 高効率の電力段(100kHz PWMで98%超、24kHz PWMで99%)によりヒート・シンクが小型化
- ゲート低電圧、過電流、過熱に対する保護

アプリケーション

- モータ内蔵ドライブ
- サーボ・ドライブ
- ロボティクス





1 System Description

High-voltage brushless motors with low inductance and high speed are used in precision applications like servo drives, CNC machines, and industrial robotics. There is a need for driving low-inductance motors using a three-phase inverter at a high switching frequency to reduce the torque ripple in the motor and minimize the losses in the motor.

The phase current ripple is inversely proportional to the switching frequency of the pulse width modulation (PWM). The phase current ripple contributes to motor losses, which reduce the efficiency of the motor and increase the temperature of the motor. These losses are especially present in motor-integrated power electronics and multi-axis drives used in service robots, where any additional motor losses limit the maximum power of the device over the rated operating temperature range.

For precision servo drives, which require high position accuracy, a torque ripple can have a negative impact on static position accuracy. The motor phase-current ripple must be reduced to reduce the torque ripple for a given motor, which can be achieved by increasing the inverter PWM switching frequency.

However, inverters based on IGBTs cannot increase the switching frequency above 40 kHz due to large switching losses. The switching losses necessitates to use a larger heat sink with an IGBT. A larger heat sink increases the system cost, weight, and space. The solution to this problem is to use gallium nitride GaN FETs, which can operate with much lower power dissipation. 表 1 shows the advantage GaN-FETs have over Si-FETs.

表 1. Comparison of Silicon MOSFET and TI's GaN FET (HEMT)

PARAMETER	Si-FET	TI's GaN (HEMT)	COMMENTS
Device structure	Vertical	Lateral	The TI GaN FET and driver are in the same package, which reduces parasitic inductances and optimizes switching performance
R_{DS_ON}, area metric	> 10 mΩ-cm^2	Lateral 5 to 8 mΩ-cm^2	Lower conduction losses
Gate charge Q_G	≈ 4 nC-Ω	≈ 1 to 1.5 nC-Ω	Reduces gate driver losses and enables faster switching, lower switching losses, and lower dead band distortions
Reverse recovery Q_{RR}	≈ 2 to 15 µC-Ω	—	Zero reverse-recovery enables efficient half-bridge inverters and reduces or eliminates ringing in hard switching

GaN transistors can switch much faster than silicon MOSFETs, which allows the potential to achieve lower switching losses. However, at high slew rates, certain package types can limit GaN FET switching performance. Integrating the GaN FET and driver in the same package reduces parasitic inductances and optimizes switching performance. The faster switching is achieved with little or no turnon or turnoff ringing, which reduces the electromagnetic interferences. For more details, see the GaN white paper page (SLYY071).

The low-power dissipation benefits servo and embedded drives. In servo drives, the low-power dissipation results in a small form factor. In embedded drives, the drive electronics is enclosed inside the motor hub, and the inverter uses the motor frame as the heat sink. Here the inverter has to operate at high ambient temperatures with little cooling. The low-power dissipation allows the embedded drive inverter to deliver more power for the same operating temperature.

The TIDA-00915 is a three-phase inverter for driving 200-V AC servo motors with 2 kW_{PEAK}. It features a 600-V and 12-A LMG3410 GaN power module with an integrated FET and gate driver. The inverter is able to operate at a high switching frequency of 100 kHz, which reduces the current ripple and improves torque ripple when used with low-inductance motors. The TIDA-00915 has the three-phase inverter with the required isolation, DC-link voltage sensing, and inline current sensing. The TIDA-00915 board supports interface to a C2000™ F28379D control card through an adaptor card. The adaptor card is designated as TIDA-00915-Controller.

1.1 Key System Specifications

表 2. Key System Specifications

PARAMETER	SPECIFICATION
DC link voltage	300 V (200 to 450 V)
Output voltage	Three-phase 220-V AC
Current	4.5 A_{RMS} continuous
Nominal output power	1.5 kW
Peak output power	2 kW
Slew rate	20 kV/µs
PWM switching frequency	100 kHz
PWM dead-band	50 ns
Efficiency	99% at 24 kHz, 2-kW output power 98% at 100 kHz, 2-kW output power
Protection	UVLO protection on gate drive power supply (9.3 V) Overcurrent protection (24 A) Overtemperature protection (160°C)
Feedback	Three inline isolated current sensing DC-Link Voltage sensing
Host controller interface	3.3-V I/Os with: • 6× PWM signals for three phase inverter • 4× delta-sigma modulated feedback signals
PCB form factor	180 mm × 82 mm 4 layers 1.6-mm thickness

2 System Overview

2.1 Block Diagram

図 1 shows the system block diagram of the three-phase GaN inverter with the TIDA-00915 reference design indicated in the red dotted box. The three-phase inverter employs six GaN power modules LMG3410, which have a 600-V and 12-A rating. There are three isolated line current sensing using shunt-based isolated delta-sigma modulators (AMC1306), one on each motor terminal. The TIDA-00915 three-phase inverter accepts voltages from 200- to 450-V DC at the DC-link input. The nominal DC input voltage is 300-V DC. The GaN module has built-in undervoltage lockout (UVLO) on the gate drive input, overcurrent protection, and overtemperature protection.

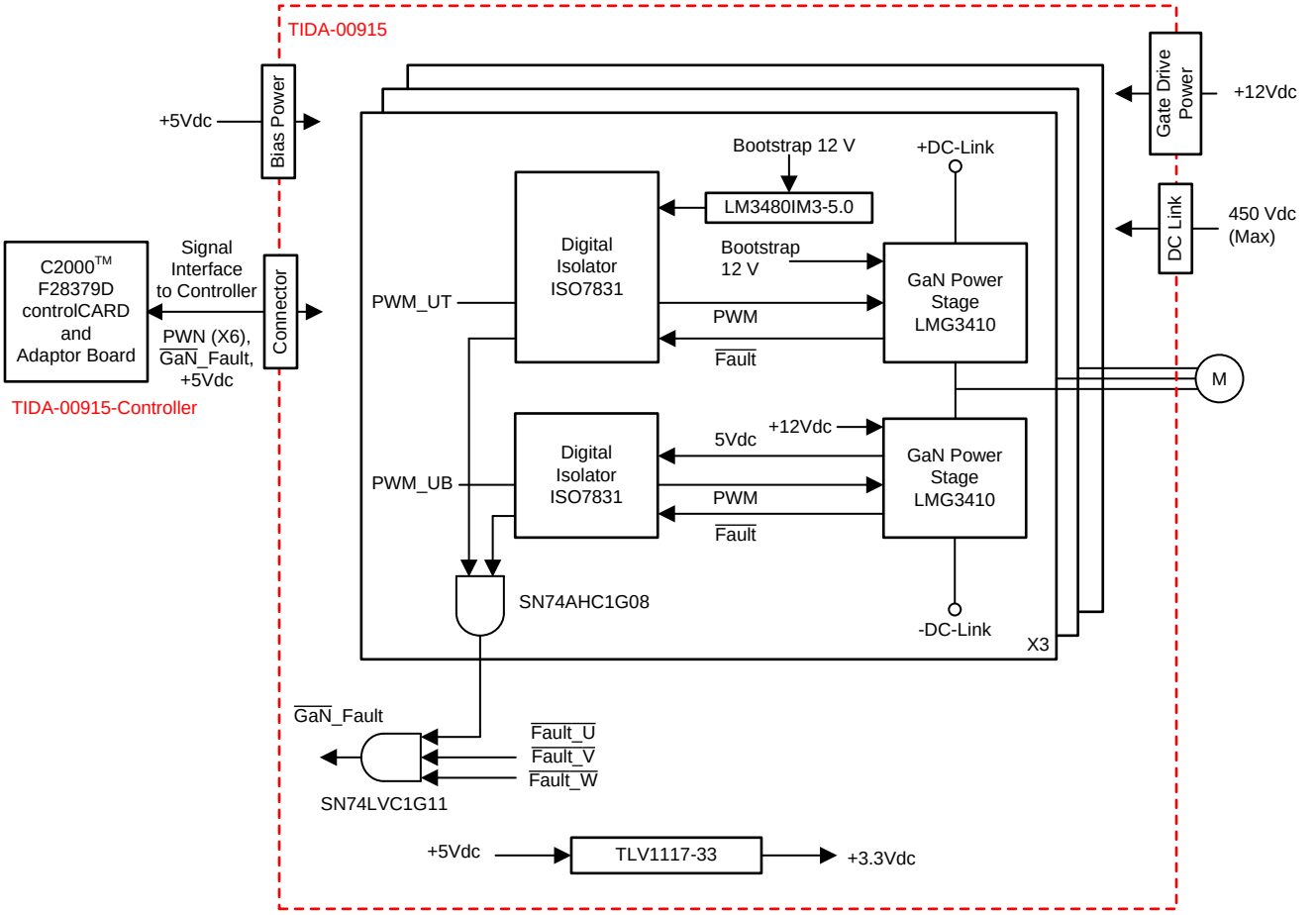


図 1. TIDA-00915 Block Diagram

Reinforced isolation is provided between the low-voltage MCU side and the high-voltage GaN inverter using ISO7831 digital isolators. The digital isolators are needed for the six PWMs of the inverter and connect the $\overline{\text{FAULT}}$ signals to the low-voltage side. The $\overline{\text{FAULT}}$ signal from each power module is grouped using AND gates (SN74AHC1G08, SN74LVC1G11)

The low-voltage side is powered from an external 5-V input. A TLV1117-33 LDO is used to generate a 3.3-V rail from this 5-V input for powering the MCU side of the digital isolator. An external 12-V gate drive power supply is used, which has to be isolated from the 5-V input given on the low-voltage side. The 12-V gate drive power supply biases the three low-voltage GaN modules. A three-bootstrap 12-V rail is derived from the gate drive power supply for the three high-side GaN modules. The GaN module generates 5-V and –12-V rails, which are used internally. This 5-V rail is also used to bias the three bottom digital isolators. The high-voltage side of the top digital isolator is powered from the LM3480 5-V LDO.

The inverter power stage interfaces to the C2000 control card. There is an adaptor board (TIDA-00915-Controller) on which the control card is inserted. The adaptor board interfaces the TIDA-00915 through a ribbon cable. The C2000 control card and implements a simple space vector modulated PWM to generate a rotating voltage vector where the voltage vectors frequency and magnitude can be controlled. The firmware is based on the controlSUITE™ library.

2.2 Highlighted Products

2.2.1 LMG3410

The LMG3410 Single-Channel GaN Power Stage contains a 70-mΩ, 600-V GaN power transistor and specialized driver in an 8-mm by 8-mm QFN package. The Direct Drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3410 is unpowered, integrated low-voltage silicon MOSFET turns the GaN device off at its source. In normal operation, the low-voltage silicon MOSFET is held on continuously while the GaN device is gated directly from an internally generated negative voltage supply.

The integrated driver provides additional protection and convenience features. Fast overcurrent, overtemperature, and UVLO protections help create a fail-safe system; the device's status is indicated by the FAULT output. An internal 5-V low-dropout regulator (LDO) can provide up to 5 mA to supply external signal isolators. Finally, externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

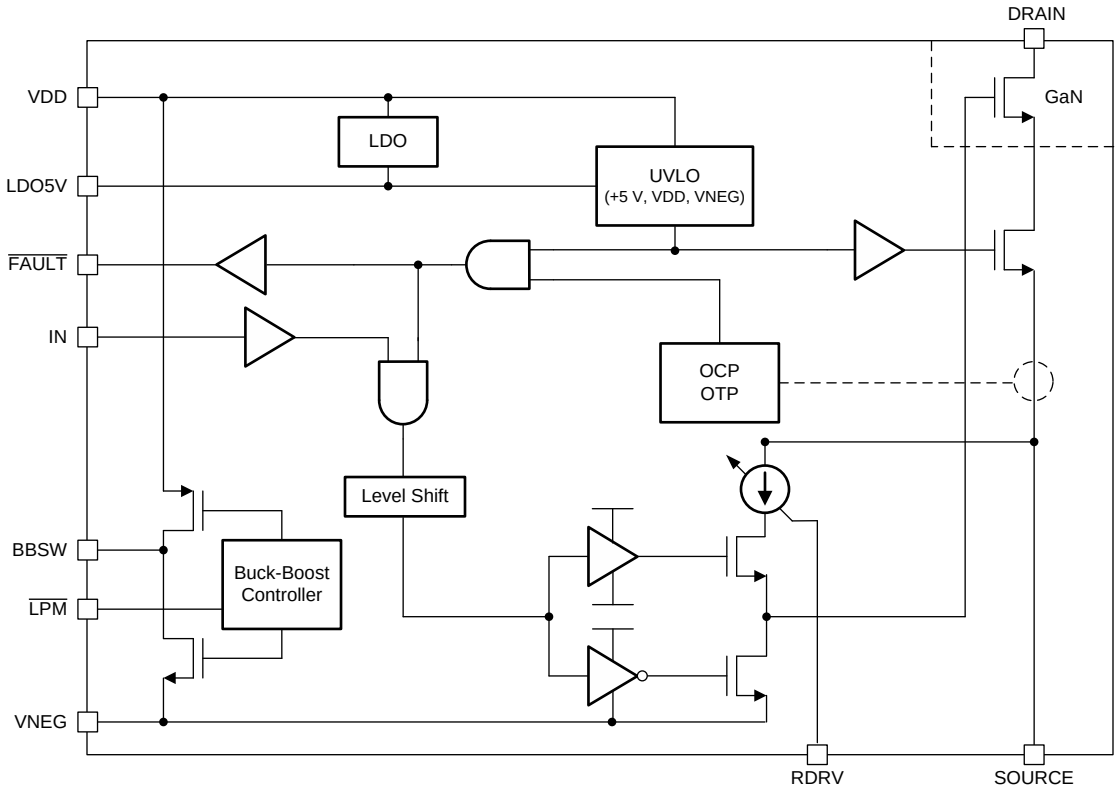


図 2. Functional Block Diagram of LMG3410

2.2.2 ISO7831

The ISO7831x device is a high-performance, three-channel digital isolator. This device has isolation certifications according to VDE, CSA, TUV, and CQC. The ISO7831x device also incorporates advanced circuit techniques to maximize the CMTI performance with an industry leading CMTI of ±100-kV/μs minimum. The isolator provides high EMI and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os.

Each isolation channel has a logic input and output buffer separated by silicon dioxide (SiO2) insulation barrier. The ISO7831x device has two forward and one reverse-direction channels. If the input power or signal is lost, the default output is high for the ISO7831 device and low for the ISO7831F device.

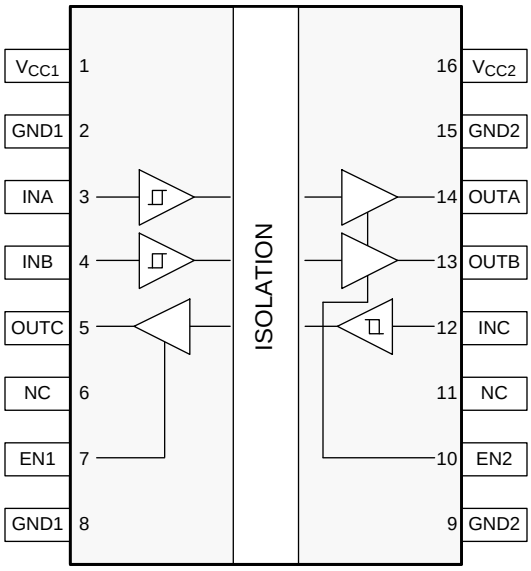


図 3. Functional Block Diagram of ISO7831

2.2.3 LM3480

The LM3480 is an integrated linear voltage regulator. It features operation from an input as high as 30 V and an ensured maximum dropout of 1.2 V at the full 100-mA load. Standard packaging for the LM3480 is the three-lead SOT-23 package.

The 5-V, 12-V, and 15-V members of the LM3480 series are intended as tiny alternatives to industry standard LM78Lxx series and similar devices. The 1.2-V quasi-low dropout of LM3480 series devices makes them a nice fit in many applications where the 2- to 2.5-V dropout of LM78Lxx series devices precludes their (LM78Lxx series devices) use. The LM3480 series also features a 3.3-V member. The SOT-23 packaging and quasi-low dropout features of the LM3480 series converge in this device to provide a very nice, very tiny bias supply.

2.2.4 TLV1117

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents. The TLV1117 device is designed to be stable with tantalum and aluminum electrolytic output capacitors having an ESR between 0.2 and 10 Ω. Unlike pnp-type regulators, in which up to 10% of the output current is wasted as quiescent current, the quiescent current of the TLV1117 device flows into the load, increasing efficiency.

2.2.5 AMC1306

The AMC1306 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to the DIN V VDE V 0884-10 and cUL1577 standards. Used in conjunction with isolated power supplies, the device prevents noise currents on a high common-mode voltage line from entering the local system ground and interfering with or damaging low-voltage circuitry.

The input of the AMC1306 is optimized for direct connection to shunt resistors or other low-voltage level signal sources. The unique low input voltage range of the ±50-mV device allows significant reduction of the power dissipation through the shunt while supporting excellent AC and DC performance. The output bit stream of the AMC1306 is Manchester coded (AMC1306Ex) or un-coded (AMC1306Mx), depending on the derivate. By using an appropriate digital filter (that is, as integrated on the TMS320F2807x or TMS320F2837x families) to decimate the bit stream, the device can achieve 16 bits of resolution with a dynamic range of 81 dB (13.2 ENOB) at a data rate of 78 kSPS. On the high-side, the modulator is supplied by a 3.3- or 5-V power supply (AVDD). The isolated digital interface operates from a 3.0-V, 3.3-V, or 5-V power supply (DVDD). The AMC1306 provides a very high CMTI performance of 100 kV/µs, required in high-switching environments like GaN inverter to suppress data corruption.

2.3 System Design Theory

2.3.1 Three Phase GaN Inverter Power Stage

The three-phase GaN inverter is realized with six LMG3410 GaN modules. 図 4 shows the DC-link input and the three-phase output of the inverter section. The power stage consist of three identical half bridges; one of the half-bridge is shown in 図 5.

2.3.1.1 Bypass and Bulk Capacitors

Two film capacitor (C50 and C51 in 図 4) of 3 µF each is used on the DC-link input to suppress any transient voltage spikes due to switching. Each half bridge also has additional local capacitors (C81 to C86 in 図 5) of 0.14 µF. The bulk capacitors, which are usually kept after the AC-to-DC rectification in the end application, are not placed on the board. The end system using the GaN inverter should have this to reduce voltage variation when operating from AC mains. However, for lab testing, this is inconsequential as the DC-link is powered from a well-regulated high voltage power supply. A bleeder resistors consisting of three series resistors of 100 kΩ are placed between the DC-link capacitors. This is done to discharge the capacitor when the turned DC-link power is switched off.

2.3.1.2 Inverter Power Capability

The LMG3410 can support maximum peak current of ±12 A_{PEAK}, which corresponds to an RMS current of 8.4 A_{RMS}. The 8.4-A_{RMS} value should not be exceeded during operation. The 8.4 A_{RMS} is a momentary maximum current rating for the TIDA-00915. The continuous current is determined by the thermal design. The board should be able to deliver 4.5 A_{RMS} (I_{RMS}) continuously at full speed, which is at 200 V_{AC} (V_{RMS}) and at the unity power factor. The corresponding power is given by 式 1, which is the output power for a balanced three phase output.

$$P_{OUT} = \sqrt{3} \times V_{RMS} \times I_{RMS} \times PF \quad (1)$$

The rated output power is calculated as $P_{OUT} = \sqrt{3} \times 200\ V \times 4.5\ A \times 1 = 1558\ W$.

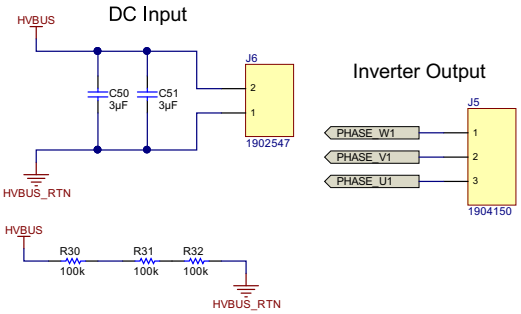


図 4. DC-Link Input and Three-Phase Output Schematic

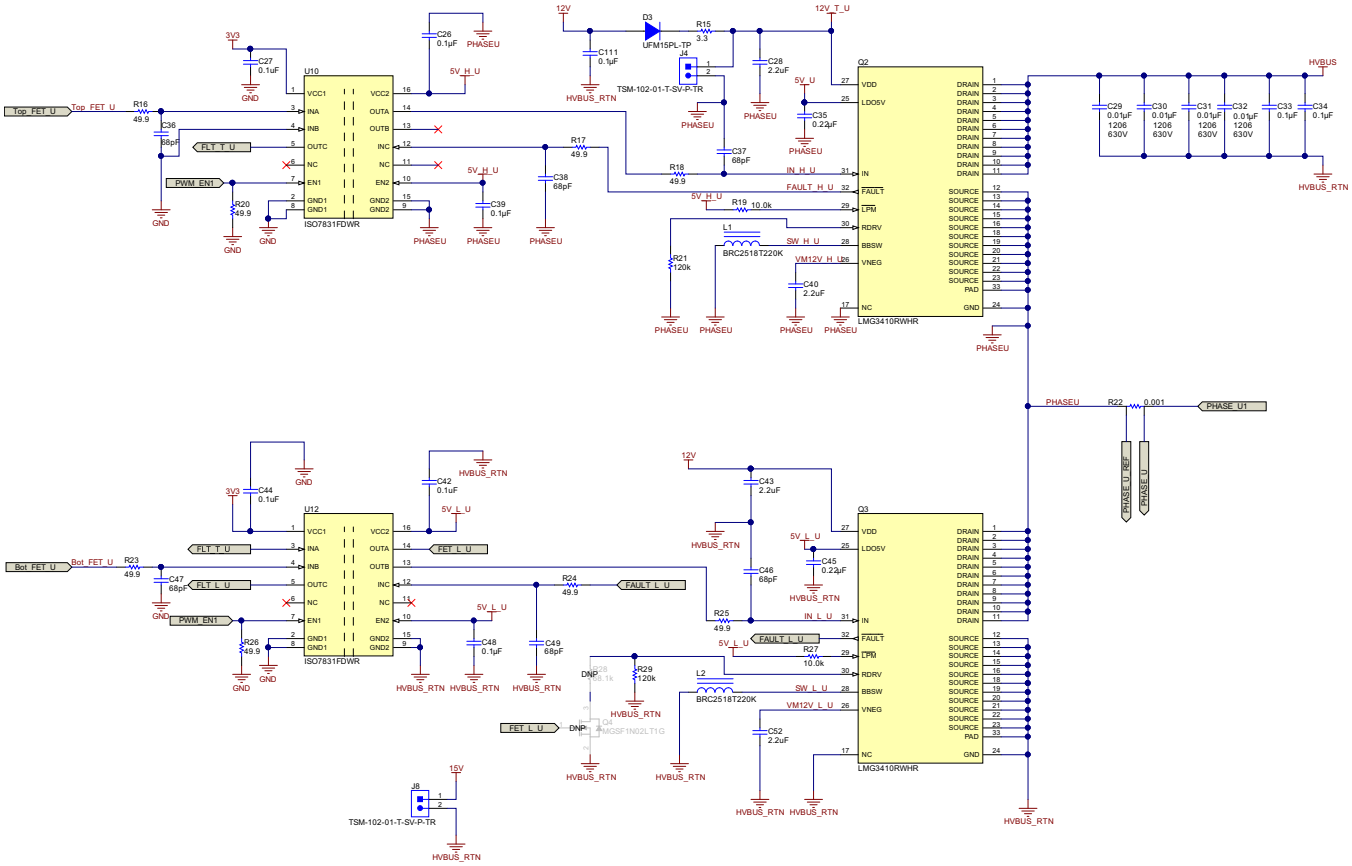


図 5. Half Bridge of GaN Inverter Schematic

2.3.1.3 Power Stage Half Bridge

The power stage consist of three identical half bridges; one of the half-bridge is shown in 図 5. Each GaN module generates 5 V from an internal LDO, which is used internally and also to power the high-voltage side of digital isolator for the bottom GaN module. C87 and C97 in 図 6 are the bulk capacitors for this 5-V LDO. The high-voltage side of the top digital isolator is biased by the 5-V LDO connected to the 15-V bootstrap power supplies. The GaN module also generates a negative 12-V power supply rail for the gate drive using an internal switching regulator, L5 and C92, and L6 and C102 are the passive components for this regulator. The RDRV pin of the GaN module is used to set the switching transient, a 120-kΩ value set the dV/dt to 20 V/ns.

Isolation is required between the GaN module, which is on the high-voltage side, and the controller generating the PWM, which is on the low-voltage side. The PCB employs two separated ground planes to achieve this galvanic isolation. The digital isolator is chosen to support a very high CMTI of 100 kV/µs. Each digital isolator is used to give a PWM input to the GaN module and also to take $\overline{\text{FAULT}}$ feedback from the GaN module to the low-voltage side.

2.3.1.4 Gate Drive Power Supply

The low-side gate drivers for all three channels are powered using 15 V, which is supplied externally from connector J8 as shown in 図 6. Each of the bottom LMG3410 has a 2.2-µF decoupling capacitor (C95 in 図 5). 図 3 calculates the current requirement for the gate drive power supply. The current consumption is considered maximum worst case from their respective datasheets. The 6.5 mA for the ISO7831 is the current consumed on the high-voltage side bias at 5 V and for a square waveform with a 1-Mb bandwidth.

表 3. Current Consumption of Gate Drive Power Supply

CIRCUIT POWERED FROM GATE DRIVE POWER SUPPLY	CURRENT
6 × LMG3410 (100 kHz)	6 x 6mA
6 x ISO7831 high side	6 × 6.5mA
3 × AMC1306 high side	4 × 3.6mA
Total	89.4 mA

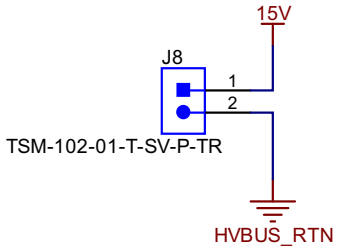


図 6. Power Supply Input of Gate Drive Schematic

2.3.1.5 Bootstrap Power Supply

The top three LMG3410 is powered by a bootstrap power supply configuration consisting of a bootstrap capacitor (C_{BOOT} is C80 in 図 5), bootstrap diode (D5 in 図 5) and bootstrap resistor (R_{BOOT} is R48 in 図 5). This method has the advantage of being simple. The maximum voltage that the bootstrap capacitor (V_{BS}) can reach is dependent on the elements of the bootstrap circuit. Consider the voltage drop across R_{BOOT}, V_F of the bootstrap diode, and the drop across the low-side switch (V_{DS_ON}, depending on the direction of current flow through the switch). Also, before the inverter is started, the bottom GaN module should be turned on for a sufficient duration to allow the bootstrap capacitor to charge.

2.3.1.6 Selection of Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor is charged when the bottom GaN module is on and is discharged when the top GaN module is on. C_{BOOT} must be sized to maintain enough voltage throughout the PWM period. The current required to supplied is 6 mA (LMG3410 at a 100-kHz PWM) + 3.6 mA (ISO7831) + 6.5 mA (AMC1306) = 16.1 mA. For 100 kHz, the PWM period is 10 µs. This corresponding charge that has to be stored on C_{BOOT} is 10 µs × 16.1 mA = 0.161 µC. Good guideline is to size C_{BOOT} to store ten times the charge over the PWM period (that is, C_{BOOT} should store Q_{BOOT} = 10 × 0.161 µC). The bootstrap capacitor has to supply this charge. C_{BOOT} is calculate as Q_{BOOT} / ΔV_{BOOT}, which is 1.7 µC/1V = 1.7 µF. C_{BOOT} is chosen to be 2.2 µF.

2.3.1.7 Selection of Bootstrap Diode

The voltage that the bootstrap diode encounters is the same as the full DC bus voltage (in this case, a maximum of 600-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. The bootstrap diode must be a fast recovery diode to minimize the recovery charge and thereby the charge that feeds from the bootstrap capacitor from the 15-V supply. The diode must be able to carry a pulsed peak current of 4.43 A (discussed in 2.3.1.8). However, the average current is much smaller and depends on the switching frequency and the bootstrap charge. The selected diode is UFM15PL which is a 600-V, 1-A diode with a fast reverse recovery.

The bootstrap diode power dissipation (P_{DBOOT}) can be estimated based on the switching frequency, diode forward voltage drop, and the switching frequency of the PWM signal (f_{SW}). In this TI Design, the switching frequency has been set to 100 kHz. The estimated power loss for the bootstrap diode is P_{DBOOT} = ½ × Q_{BOOT} × V_{DBOOT} × f_{SW} = 0.5 × 1.7 µC × 1.7 V × 100 kHz = 144.5 mW.

2.3.1.8 Selection of Current Limiting Resistor for Bootstrap Diode (R_{BOOT})

The bootstrap charge Q_{BOOT} flows through R_{BOOT} for a charging time of 0.3 µs; the average resistor current should be I_{CH} = Q_{BOOT} / t = 0.161 µC / 0.3 µs = 0.53 A.

With the voltage drop across the diode being 1.7 V, R_{BOOT} = V_{DBOOT} / I_{CH} = 1.7 V / 0.53 A = 3.2 Ω.

This TI Design uses an R_{BOOT} value of 3 Ω.

The peak resistor current is (15 V – V_{DBOOT}) / R_{BOOT} = (15 V – 1.7 V) / 3 Ω = 4.43 A. The R_{BOOT} resistor should be able to supply this peak current and the average current of 0.53 A.

2.3.1.9 Thermal Design

The aim of the thermal design is to ensure the TIDA-00915 board can deliver the rated power without exceeding the maximum junction temperature of the GaN modules. The temperature depends on power loss occurring inside the GaN module, the power loss is also the heat generated on the board. Considering an efficiency of 98% at the rated power of 1.5 kW, the corresponding power loss on the board is 30.6 W. This power loss is distributed across each GaN module, hence the power loss per GaN module is (30.6 W) / 6 = 5.1 W.

The LMG3410 datasheet gives the thermal specification of θ_{JA} while operating in still air of 26.5°C/W. When operating at 5.1 W, the temperature rise of the LMG3410 junction is 5.1 W × 26.5°C/W = 135°C. This value is more than the 125°C rating of the LMG3410.

A heat sink with fan cooling is chosen. The fan is assumed to give 800 LFM of air flow to operate the heat sink at max thermal efficiency. Approximate thermal calculations with heat sink shown in 表 4 with assumption of equal distribution of the power loss between the six GaN modules.

表 4. Thermal Impedance Estimation of Three-Phase GaN Inverter

COMPONENT	THERMAL IMPEDANCE (θ)	THERMAL IMPEDANCE (θ) FOR 6 GaN MODULES
LMG3410 GaN module θ_{JC}	0.5°C/W	= 0.5 / 6 = 0.084°C/W
24 thermal via (10-mil diameter and 17.5-µm via copper thickness)	11.375°C/W	= 11.375 / 6 = 1.895°C/W
Thermal interface material (Part number: Tgard™ K52-1)	0.9°C-cm^2 / Watt / (Copper plane area under LMG3410) = 0.9°C-cm^2 / Watt / (0.45 cm × 0.8 cm) = 0.324°C/W	= 0.324 / 6 = 0.054°C/W
Extrusion heat sink with 800 LFM (Part number: ATS-EXL65-300-R0)	= (2.4 C/W per inch) / Extrusion length = 2.4 / 5.9 = 0.407°C/W	= 0.407°C/W

At 32 W, the temperature rise is 2.44°C/W × 30.1 = 73.44°C. The estimated room temperature of a 23°C junction temperature would be 73.44°C + 23°C = 96.44°C. There is a head room of 28°C, which limits the maximum ambient to 50°C.

2.3.1.10 Inverter Protection and $\overline{FAULT}$ Feedback

The LMG3410 has UVLO, overcurrent detection, and overtemperature with latched turnoff of the GaN FET. The UVLO is used to prevent improper operation due to a failing gate drive power supply. The overtemperature and overcurrent protection ensure the GaN FETs are protected against short circuit faults of the inverter. There are six GaN modules each with a $\overline{FAULT}$ signal, which are brought to the low-voltage side using digital isolators. The fault signals are combined using the logic circuit shown in 図 7.

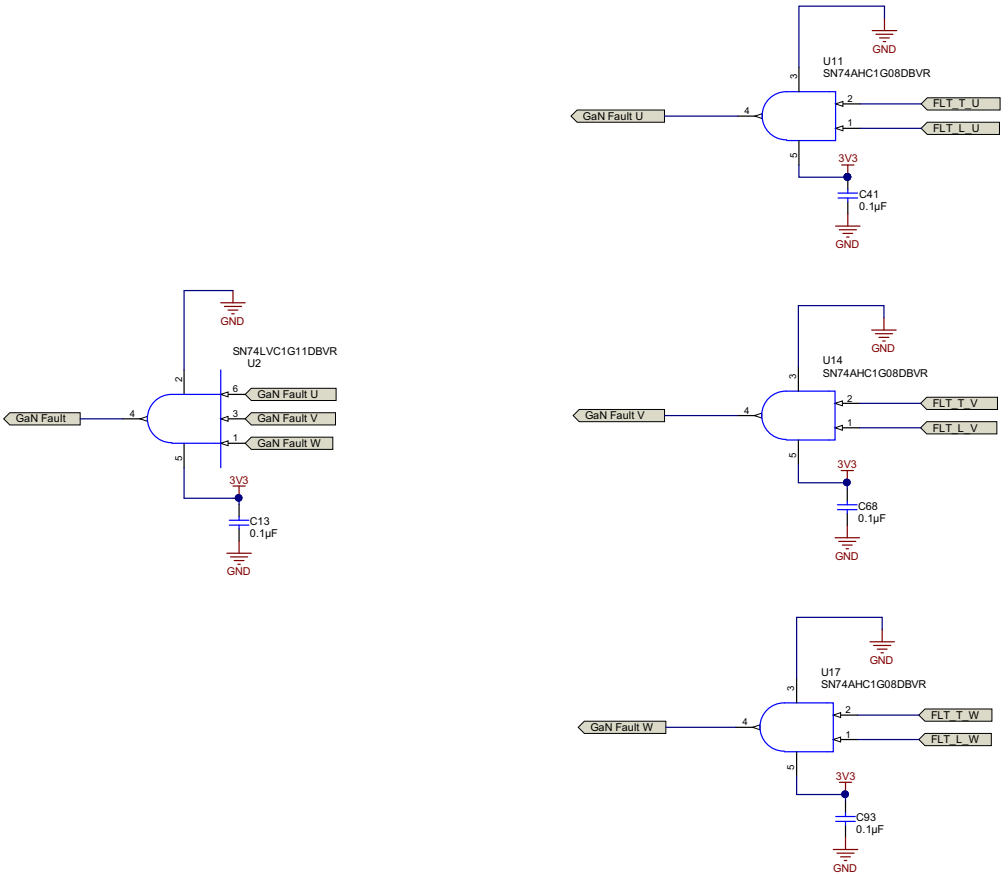


図 7. Logic Circuit to Group $\overline{\text{FAULT}}$ Signals Schematic

2.3.2 5- and 3.3-V Low-Voltage Power Rail

An external 5-V power supply is required to bias all the circuits on the low-voltage side of the board. 図 8 shows the 5-V rail input. The diode D2 protects against accidental reverse biasing the 5-V rail. The TLV1117-3 is the LDO used for generating the 3.3-V rail.

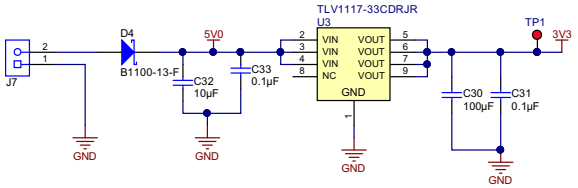


図 8. 3.3-V Power Supply LDO Schematic

表 5 shows the power consumption by the different circuit biased by the 3.3-V rail. There are three AMC1306 devices, six digital isolators, an indication LED, and FAULT grouping using AND gates powered from this 3.3-V rail. The current consumption is considered maximum worst case from their respective datasheets. The 4 mA for ISO7831 is the current consumed on the low-voltage side bias at 3.3 V and for a square waveform with a 1-Mb bandwidth.

表 5. Current Consumption of 5-V Rail Power Supply

CIRCUITS POWERED FROM 3.3-V LDO	CURRENT
ISO7831 × 6	6 × 4 mA
AMC1306 × 4	4 × 3.6 mA
Clock termination resistors ×1	1.65 mA
SN74AHC1G08 × 3	3 × 4 mA
SN74LVC1G11 × 1	16 mA
Indication LED × 1	10 mA

The total worst case power consumption is about 78 mA. The power dissipation in the LDO is $P = (V_{IN} – V_{OUT}) \times I_{OUT} = (5 – 3.3) \times 0.078 = 0.1326$ W.

2.3.3 Signal Interface to Controller

A DB-25 connector is used for the signal interface connector. 図 9 shows the different signal between interfaced to the inverter on the signal interface connector. The 5 V is given from power stage to the TIDA-00915-Controller to power the C2000 control card through the signal interface connector. This routing of the 5-V power rail is done to have the 5-V rail in a star network with the center on the TIDA-00915 board. The 5 V is required to be supplied to the TIDA-00915-Controller, where the 5-V rail is stepped down to 3.3 V by an LDO to power the C2000 MCU on the control card. The interface signals are all 3.3-V logic signals. The multiple ground lines are used on the connector to ensures a solid ground connection to prevent ground bounce issues.

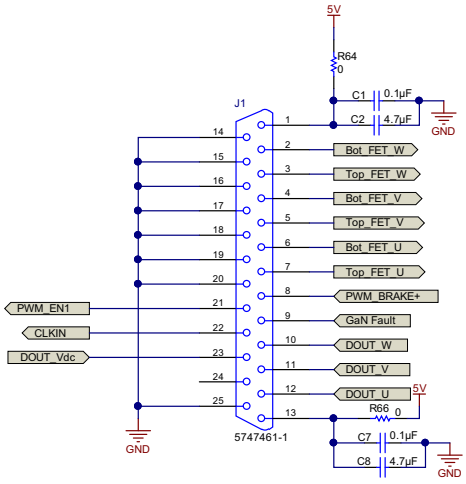


図 9. Signal Interface Connector to Controller Schematic

2.3.4 TIDA-00915 Controller

The TIDA-00915-Controller is adapter board between the 180-pin C2000 F28379D control card and the TIDA-00915 GaN inverter. The TIDA-00915-Controller has the same DB-15 signal interface connector as the TIDA-00915 GaN inverter. The inverter and the controller are connected using a DB-15 ribbon cable. 図 10 shows the important parts of the board used for testing. There are additional features on the TIDA-00915-Controller that are not used in this TI Design.

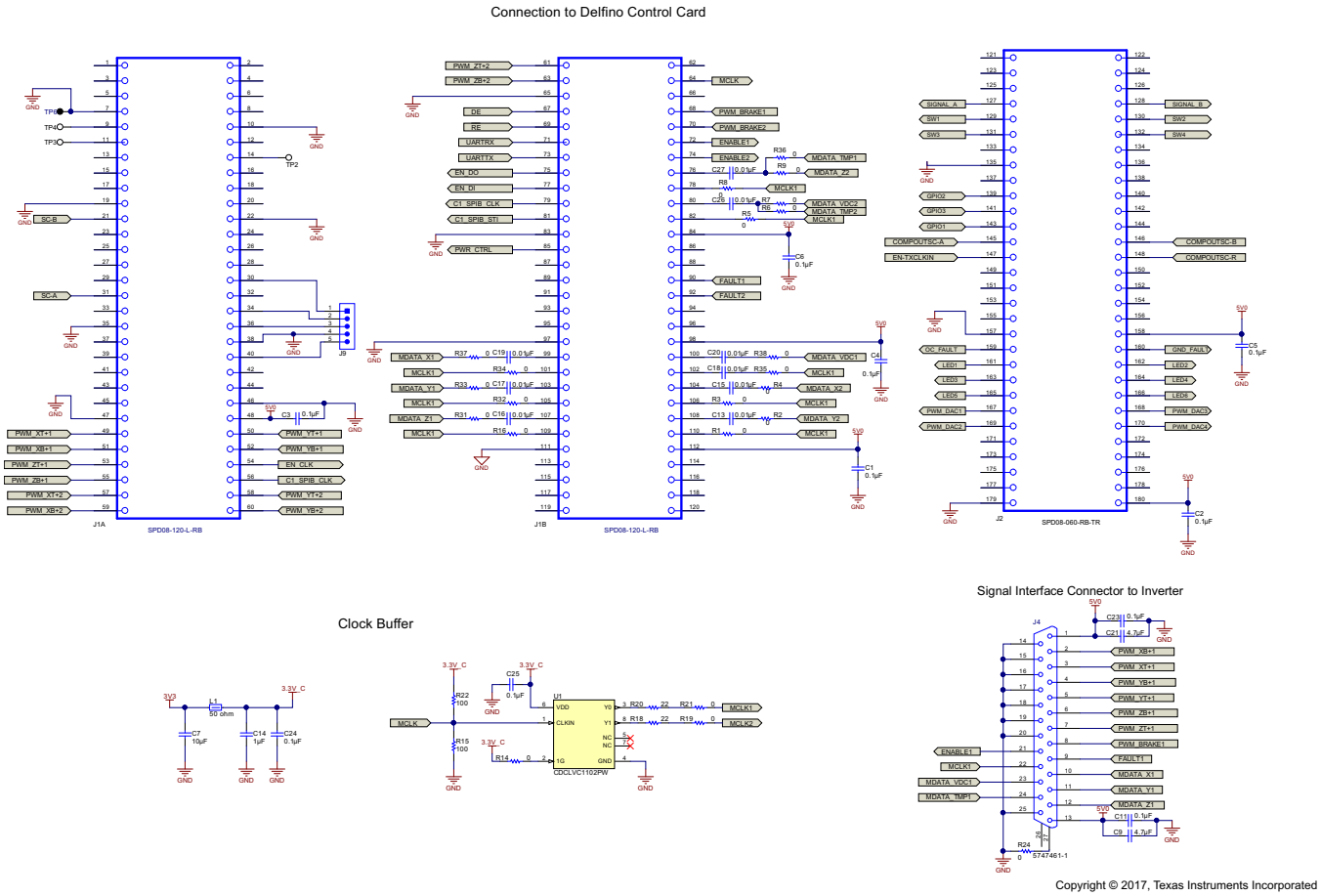


図 10. TIDA-00915 Controller Schematic

3 Getting Started Hardware and Software

3.1 Hardware

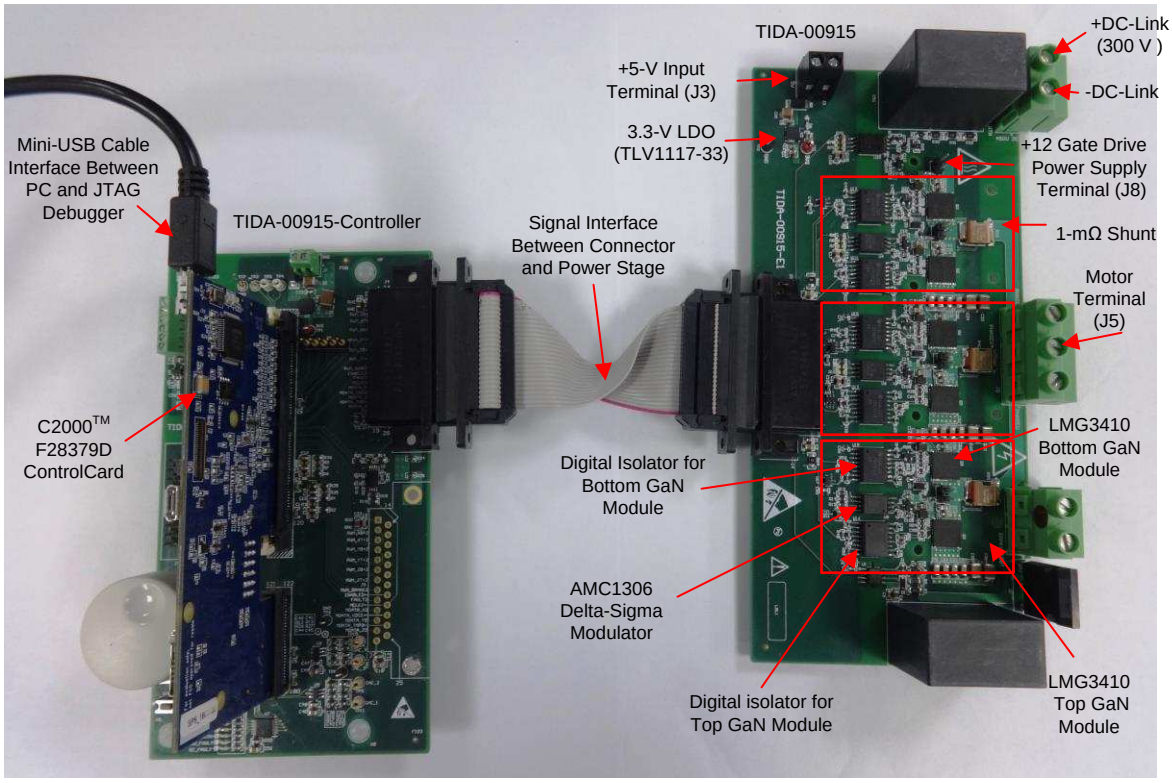


図 11. TIDA-00915 PCB and TIDA-00915-Controller Top Side

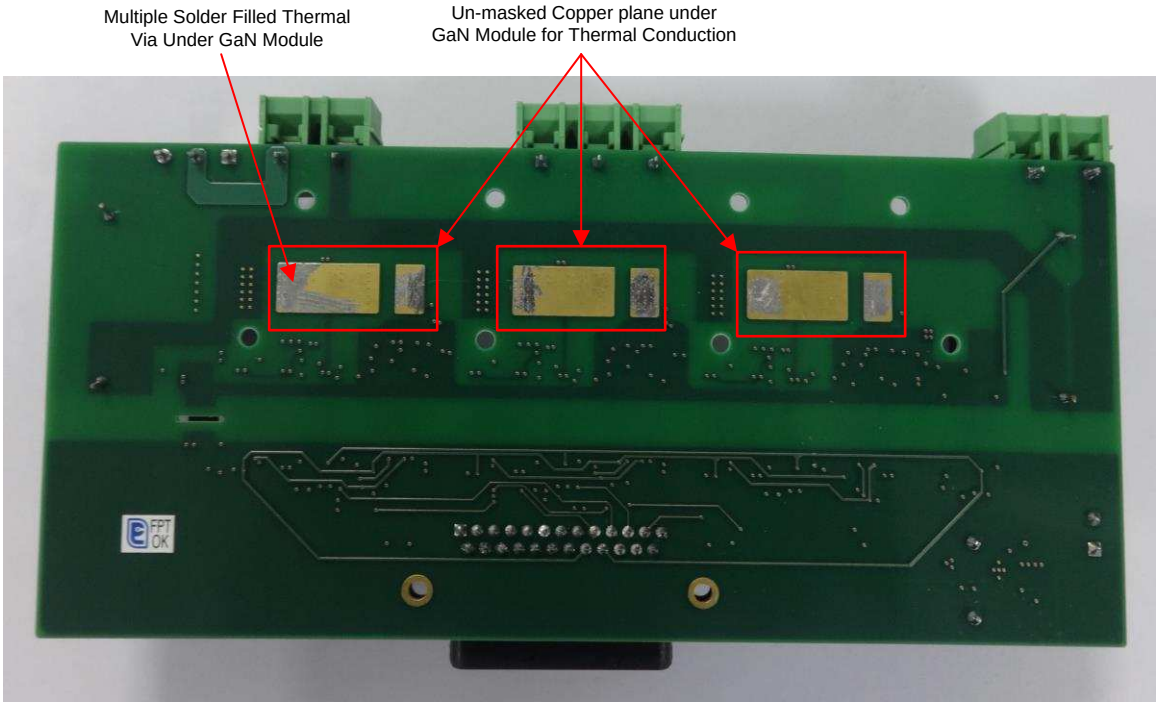


図 12. TIDA-00915 PCB Bottom Side

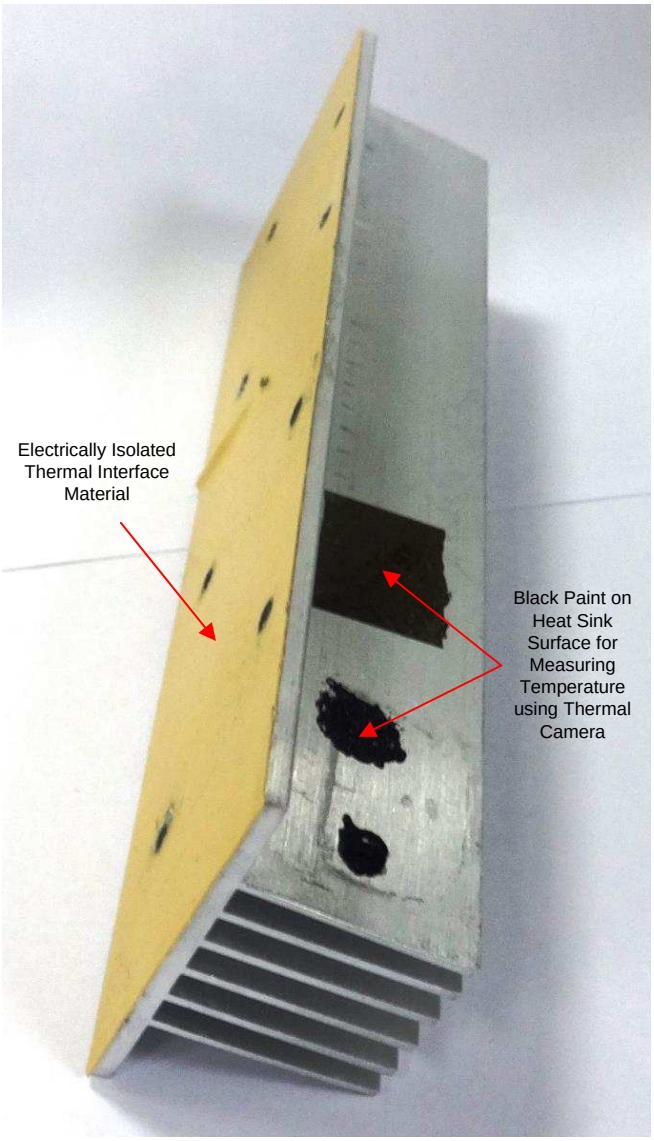


図 13. Heat Sink With Electrically Insulated Thermal Interface Material

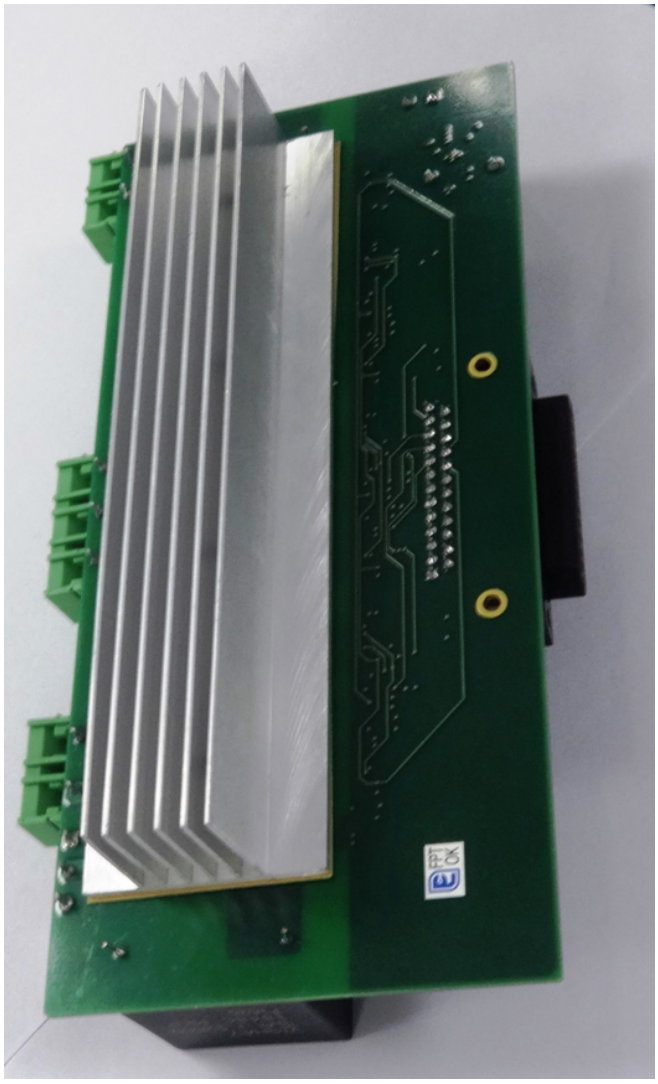


図 14. Heat Sink Mounted on Bottom Side of TIDA-00915 PCB

図 15 shows the fan used for cooling. There is an encasing around the fan to duct the airflow from top to under the PCB where the heat sink is located. 図 16 shows the position of the fan with respect to the heat sink.

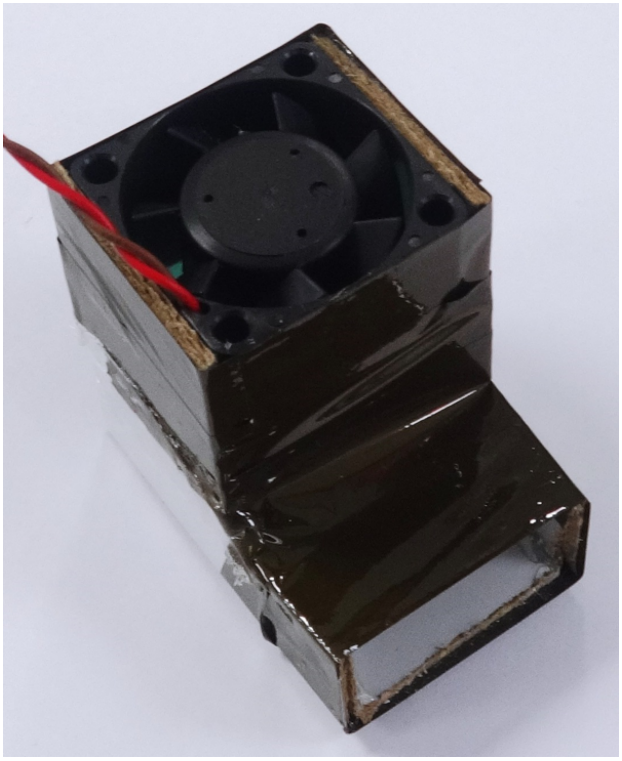


図 15. Fan With Duct

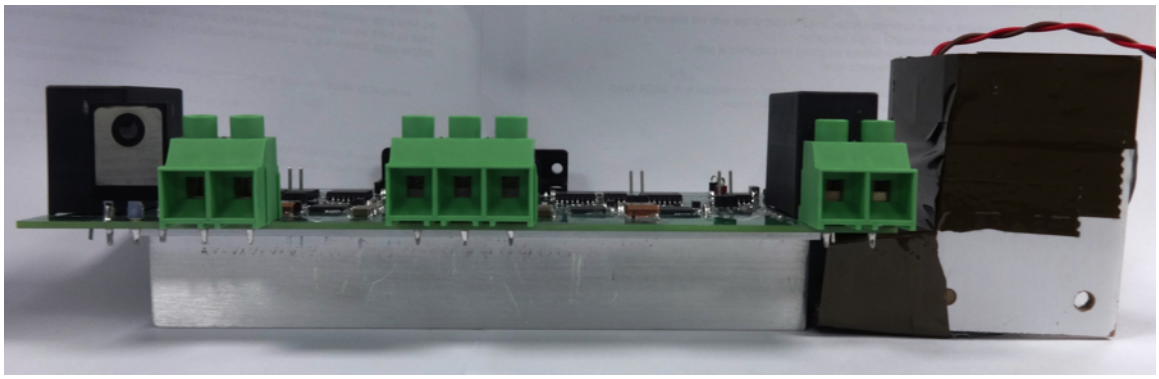


図 16. Position of Air Flow and Heat Sink

表 6. Signal Interface Connector Pin Description on TIDA-00915

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	5V	Power	5-V power to TIDA-00915-Controller
2	Bot_FET_W	3.3-V input	Phase W lo-side gate driver PWM input
3	Top_FET_W	3.3-V input	Phase W hi-side gate driver PWM input
4	Bot_Fet_V	3.3-V input	Phase V lo-side gate driver PWM input
5	Top_FET_V	3.3-V input	Phase V hi-side gate driver PWM input
6	Bot_FET_U	3.3-V input	Phase U lo-side gate driver PWM input
7	Top_FET_U	3.3-V input	Phase U hi-side gate driver PWM input
8	PWM_BRAKE+	3.3-V input	PWM input to brake IGBT gate driver
9	GaN Fault	3.3-V output	FAULT signal combined from all LMG3410 modules
10	DOUT_W	3.3-V output	Phase W current measurement data from delta-sigma modulator
11	DOUT_V	3.3-V output	Phase V current measurement data from delta-sigma modulator
12	DOUT_U	3.3-V output	Phase U current measurement data from delta-sigma modulator
13	5V	Power	5-V power to TIDA-00915-Controller
14	GND	Power	Low-voltage side ground
15	GND	Power	Low-voltage side ground
16	GND	Power	Low-voltage side ground
17	GND	Power	Low-voltage side ground
18	GND	Power	Low-voltage side ground
19	GND	Power	Low-voltage side ground
20	GND	Power	Low-voltage side ground
21	PWM_EN1	3.3-V input	Enable receiving GaN Fault Signal
22	CLKIN	3.3-V output	Clock input to TIDA-00915 from the control card
23	DOUT_Vdc	3.3-V output	DC bus voltage measurement data from delta sigma modulator
24	NC	NA	NA
25	GND	Power	Low-voltage side ground

3.2 Software

The firmware is based on controlSUITE library. The reference code and the documentation can be can be found in the controlSUITE installation location at: controlSUITE\development_kits\HVMotorCtrl+PfcKit_v2.1\HVPM_Sensorless_2833x. This code has been ported to run on the C2000 F28379D control card.

図 17 shows the block diagram of the firmware used for testing the TIDA-00915 power stage. The firmware generates a three-phase sine modulated PWM. The voltage magnitude and the sine frequency at the output of the inverter can be independently controlled with this firmware. The "SpeedRef" variable adjusts the frequency, and the "VqTesting" variable changes the magnitude of the inverter output voltage.

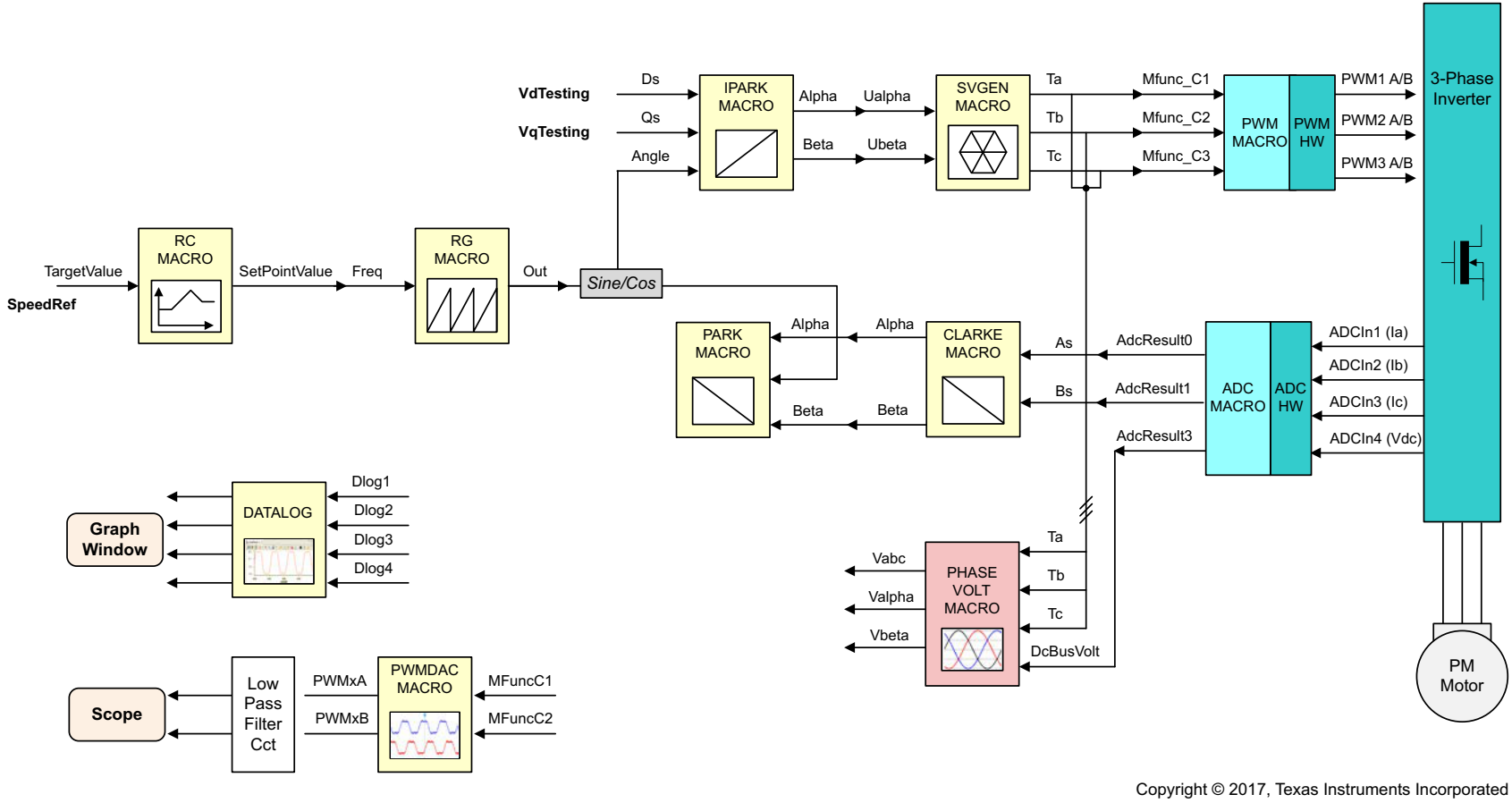


図 17. Block Diagram of Firmware Used for Testing TIDA-00915

4 Testing and Results

表 7 lists the key test equipment. The board is powered from three power supplies: 300 V for the DC-link, 15 V for the gate drive power supply, and 5 V for the low-voltage side bias. All power supplies are isolated from each other.

The following subsections provide descriptions and pictures of the test setup for each specific test.

表 7. Key Test Equipment

DESCRIPTION	PARTNUMBER
High-speed oscilloscope	Tektronix MSO2024B
Isolated oscilloscope	Tektronix TPS2014B
High-voltage probes	Keysight 10076B
Low-voltage probes	Tektronix TPP0200
Isolated current probe	Keysight N2781B
C2000 F28379D control card	Texas Instruments TMDSCNCD28379D
Adjustable power supply	Keithley 2230G-30-1
High-voltage power supply	Sorensen SGI 1000/5
Thermal camera	Fluke Ti400
Power analyzer	Tektronix PA4000
Inverter load	3.7 kW, 1460 rpm (0.5 to 100 Hz), 415 V_{RMS} ± 10%, η =83 %, cosφ = 0.74, 8.4 A_{MAX}

4.1 Bootstrap Power Supply Ripple

The bootstrap voltage across the bootstrap capacitor is monitored to verify that the rail has charged up to the expected gate drive voltage and is able to maintain the voltage throughout the entire switching cycle. This test is done with the inverter DC-link at 300 V and supplying a no-load current to the motor. The switching frequency is set at 48 kHz.

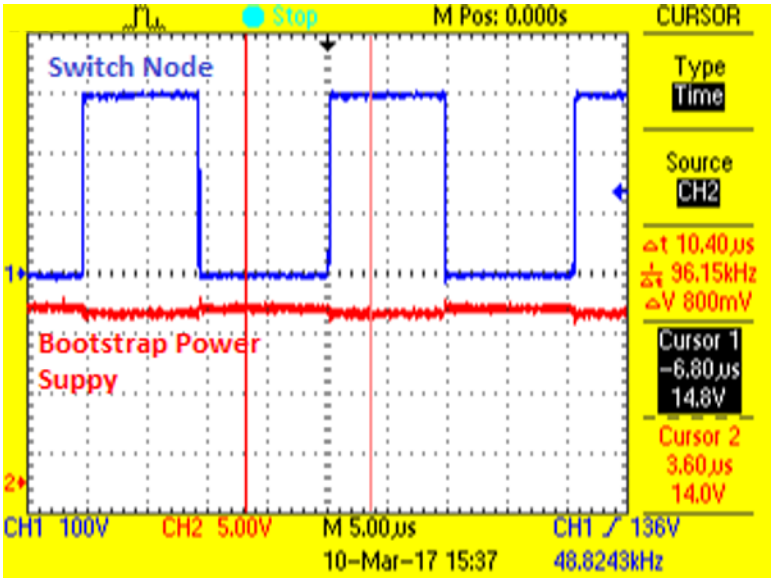


図 18. Switch Node Voltage and Bootstrap Power Supply

図 18 shows the bootstrap power supply charges to 14.8 V when the switch node voltage is low this is when the bottom GaN module is on and the top is off. The voltage drops to 14 V when the switch node voltage is high; this is when the bottom GaN module is off and the top is on. The drop is because the bootstrap cap is floating and the capacitor discharges when the top GaN module turns on. The total power supply ripple is 0.8 V.

4.2 Invert Output dV/dt and Ringing

An inverter is required to operate up to a maximum dV/dt as permitted by the type of load connected and without excessive ringing across the FETs. The ringing can cause the FETs to fail if the ringing is above the absolute maximum voltage rating.

The switch node voltage is captured with a high-voltage probe with a bandwidth of 200 MHz. The inverter was running the motor without load. 図 19 and 図 20 show the rising edge of the u-phase switch node voltage, and 図 21 and 図 22 show the falling edge. This node is the furthest from the DC-link input terminal and more prone to ringing due to a larger power trace inductance. The oscilloscope is set up to trigger when the edge transition time is less than the trigger threshold time. This corresponds to the highest dV/dt, which is also when the half bridge is hard switching.

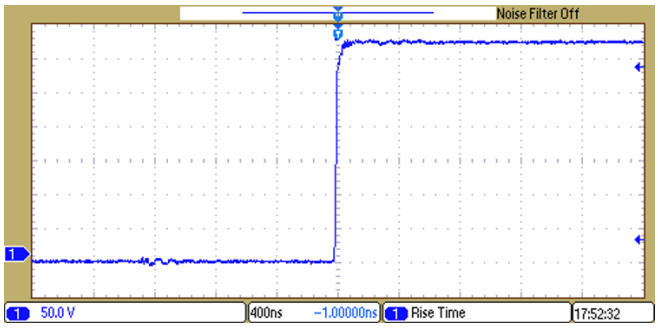


図 19. Rising Edge Switch Node Waveform

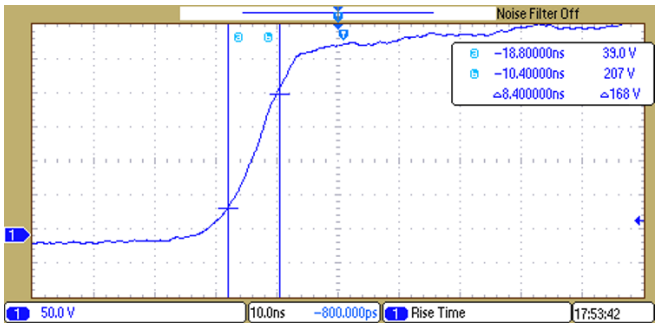


図 20. Rising Edge Switch Node Waveform Zoomed

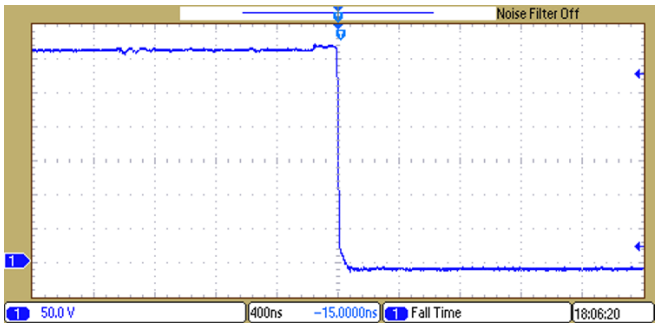


図 21. Falling Edge Switch Node Waveform

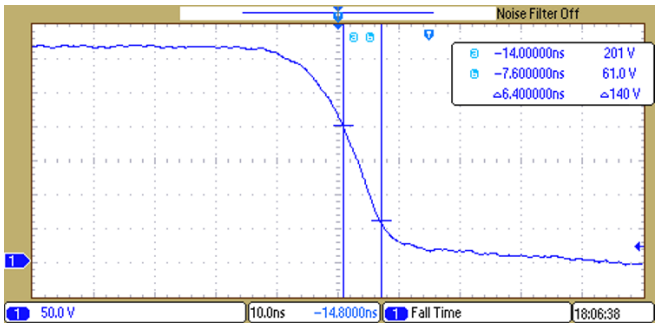


図 22. Falling Edge Switch Node Waveform Zoomed

図 19 and 図 21 show that there is no visible ringing at the end of rising edge or the falling edge of the switch node. The ringing happens in silicon FETs as it is oscillation between FET output capacitance the parasitic trace inductance. The ringing in a GaN-based inverter is absent as the GaN FET has very small output capacitance. The rising and falling dV/dt is measure to be 20 V/ns and 21 V/ns, respectively.

4.3 Inverter Power Loses

The inverter power loss is obtained using a power analyzer, which measures the input power at the DC-link terminal and the output power at the three phase inverter output terminal. The difference between input and output power is the power loss. This test is done at 300 V and the inverter is loaded by the motor. 図 24 is the power loss versus the output line current of the inverter.

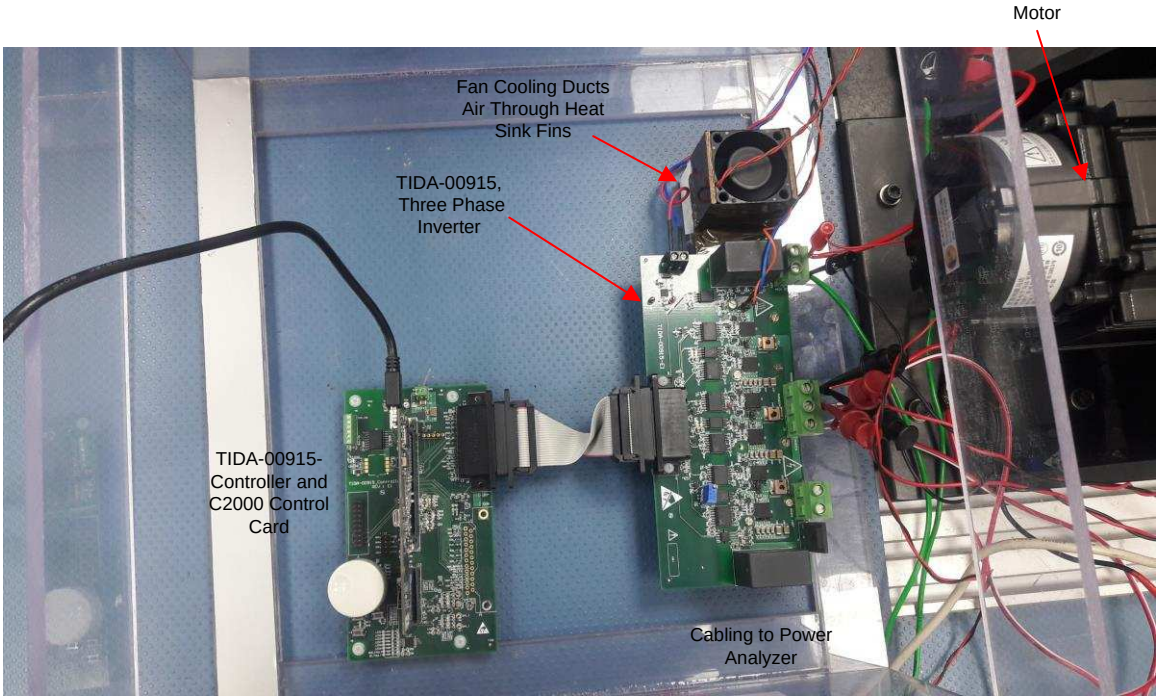


図 23. Test Setup for Inverter Power Loss

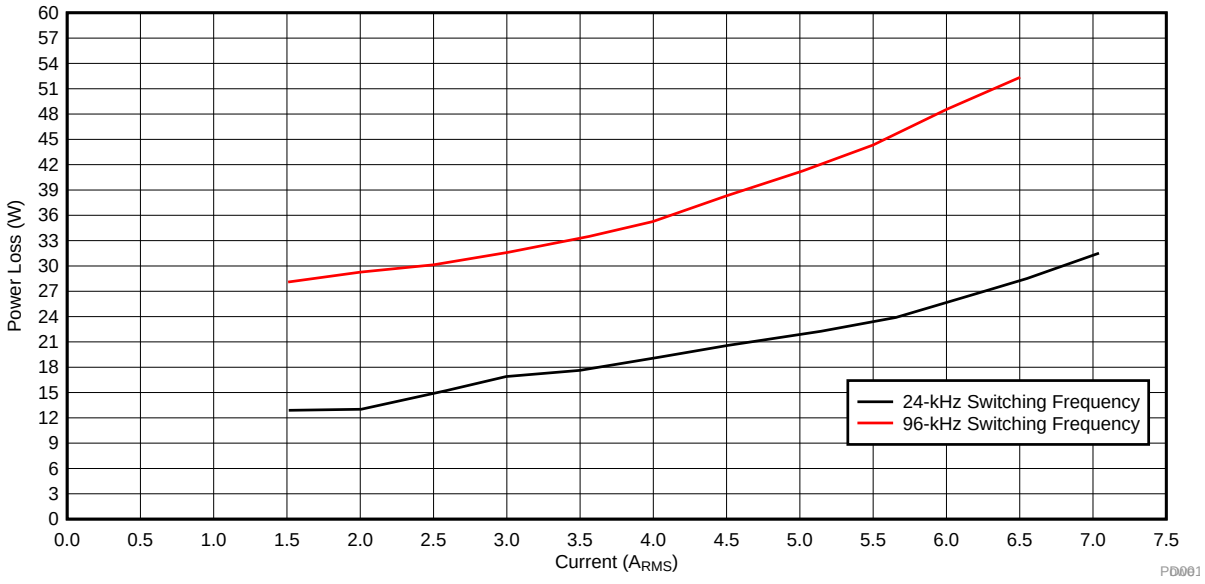


図 24. Inverter Power Loss

Inverter efficiency is derived from the power loss by calculating the output power and input power. The output power is obtained from 式 1 where:

- V is the maximum RMS voltage form the inverter, calculated as DC-Link Voltage × 1.15 / √2.
- I_{RMS} is the line current used in 図 24 for the inverter power loss
- PF is the power factor for a permanent magnet servo motor the power factor is near 1.

The input power is obtained from $P_{IN} = P_{OUT} + P_{LOSS}$.

Efficiency $\eta = P_{OUT} / P_{IN} \times 100$.

図 25 is the inverter efficiency plotted versus the output power and also the inverter current.

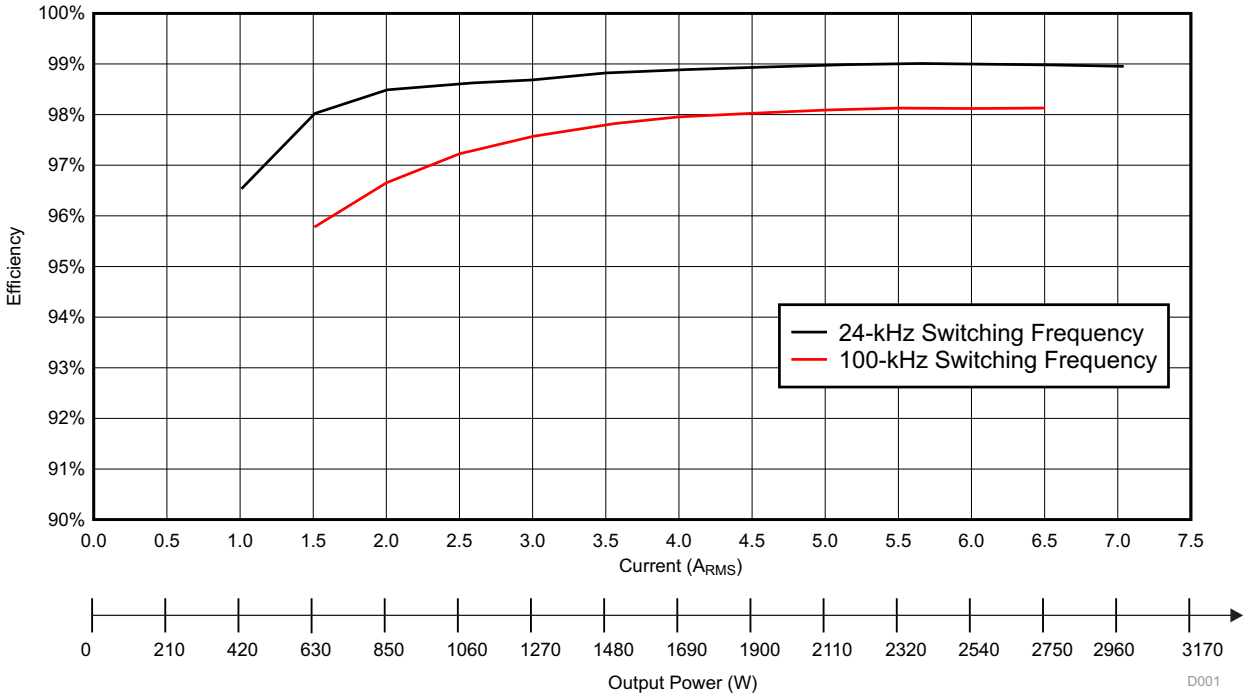


図 25. Inverter Efficiency versus Inverter Current Output Power

4.4 Thermal Characteristics

This test verifies the safe operation of the inverter with the chosen heat sink and fan cooling with the PCB in an open environment. However, characteristics depend on the amount of cooling available, hence results can vary in the end product depending on if more or less cooling available. This test should be only taken for guidance that a small thermal solution is possible for a 2-kW inverter and is made possible by the low-power loss of the GaN module-based inverter.

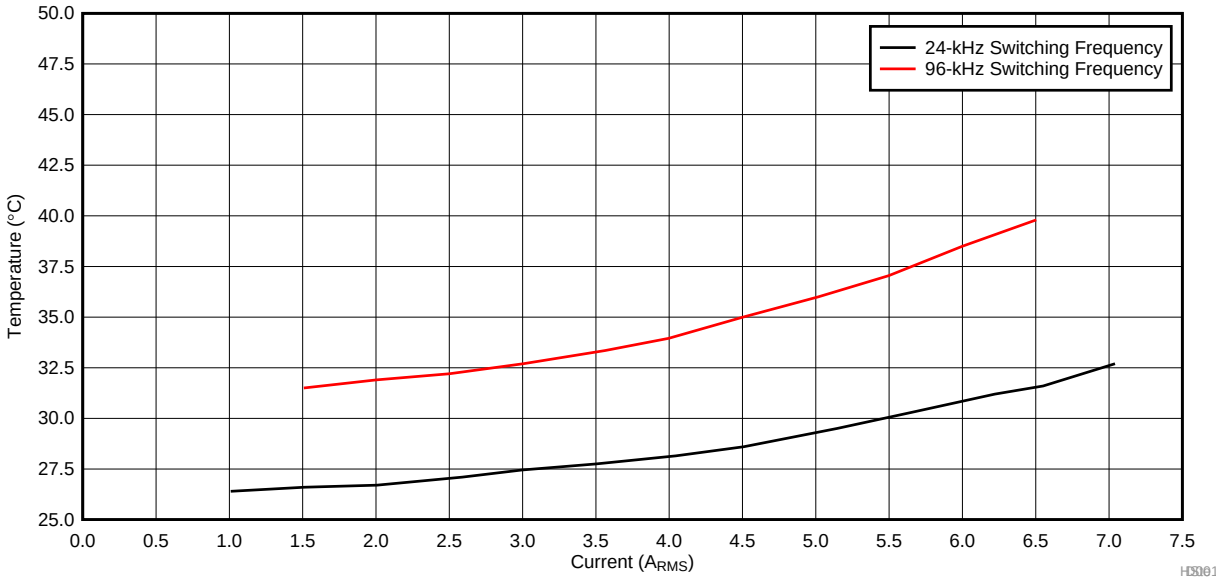


図 26. Heat Sink Temperature versus Inverter Output Current

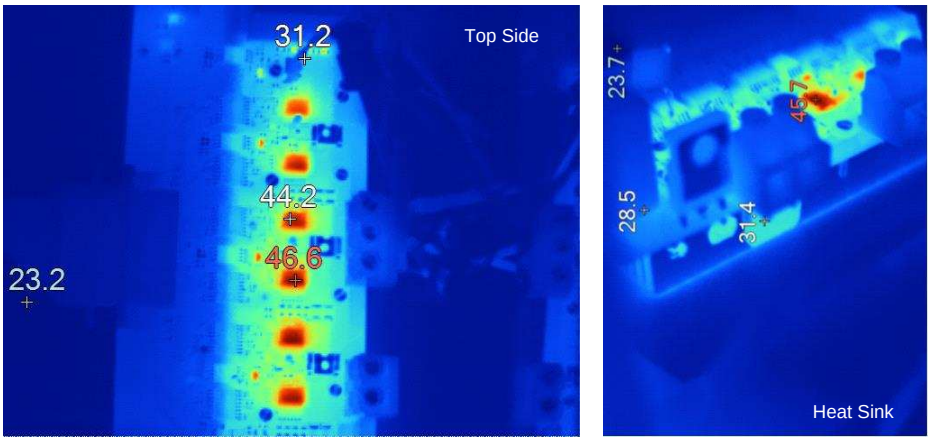


図 27. Inverter Thermal Image at 24-kHz and 4.5-A_{RMS} Inverter Output Current

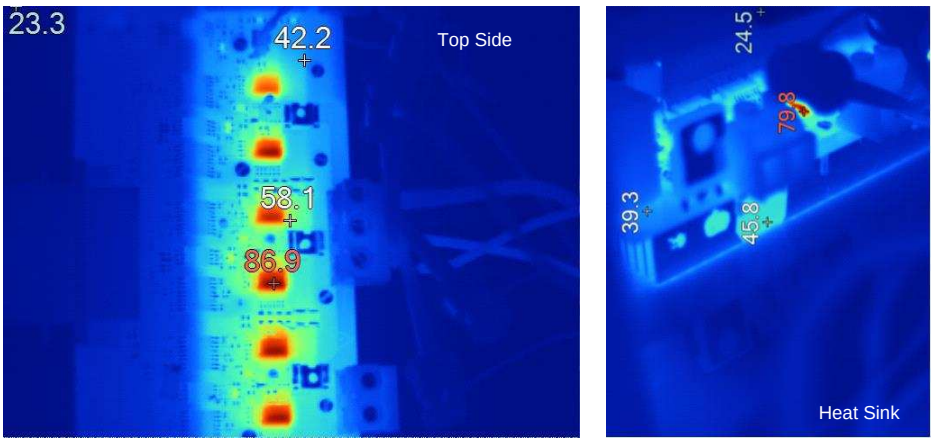


図 28. Inverter Thermal Image at 100-kHz and 4.5-A_{RMS} Inverter Output Current

4.5 Undervoltage Protection for Inverter Gate Drive Power Supply

Under normal operation, the inverter is started after all the power rails have reached their proper voltage level. There may be a condition that the power supply of the gate drive has failed and the voltage is below the recommended value. This situation is prevented by the detection of undervoltage and disabling the turnon of the gate driver inside the LMG3410 GaN module.

The UVLO is verified by powering the DC-link form a 300-V power supply and the inverter is given a PWM of 100 kHz with a constant duty. The bench power supply connected to the gate drive power supply is turned off. The point at which the switch node stops giving a PWM is when the UVLO is activated when the voltage is falling. Similarly, the power supply of the gate drive is turned on and the point at which the switch node start gives a PWM is where the UVLO is deactivated.

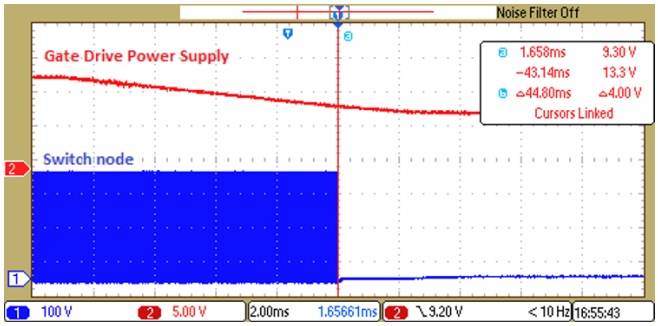


図 29. UVLO Activation due to Falling Gate Drive Power Supply

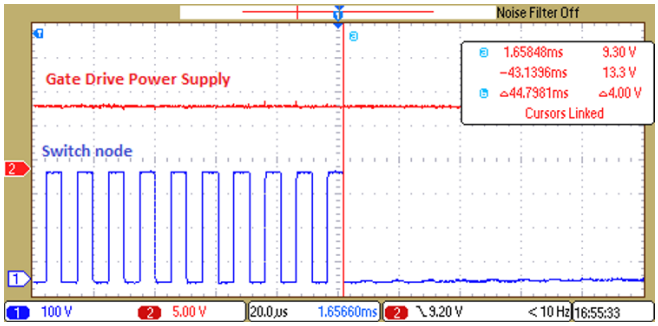


図 30. Zoomed in UVLO Activation due to Falling Gate Drive Power Supply

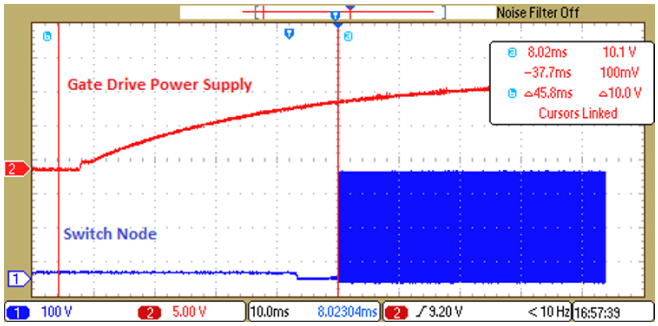


図 31. UVLO Deactivation due to Rising Gate Drive Power Supply

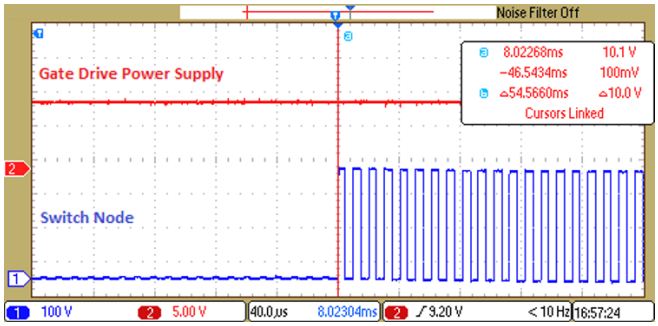


図 32. Zoomed in UVLO Deactivation due to Rising Gate Drive Power Supply

図 30 shows the UVLO is activated at 9.1 V and 図 32 UVLO is deactivated at 10.1 V. There is a hysteresis of 0.5 V between the activation and deactivation of the UVLO.

4.6 Inverter Overcurrent Protection

This test is validates effectiveness of the overcurrent trip provided inside the LMG3410 to protect the three-phase inverter.

For the test an overcurrent situation is created in the inverter when driving an induction motor. The motor is suddenly over magnetized by suddenly reducing the frequency of the space vector PWM while the voltage vector is kept constant.

図 33 shows the result of the test, where the waveforms are triggered when $\overline{\text{FAULT}}$ signal is activated along with one of the inverter line current. The $\overline{\text{FAULT}}$ signal is the grouped fault signal ($\overline{\text{GaN\_FAULT}}$) from all the LMG3410 modules in the inverter. The PWM frequency is 100 kHz.

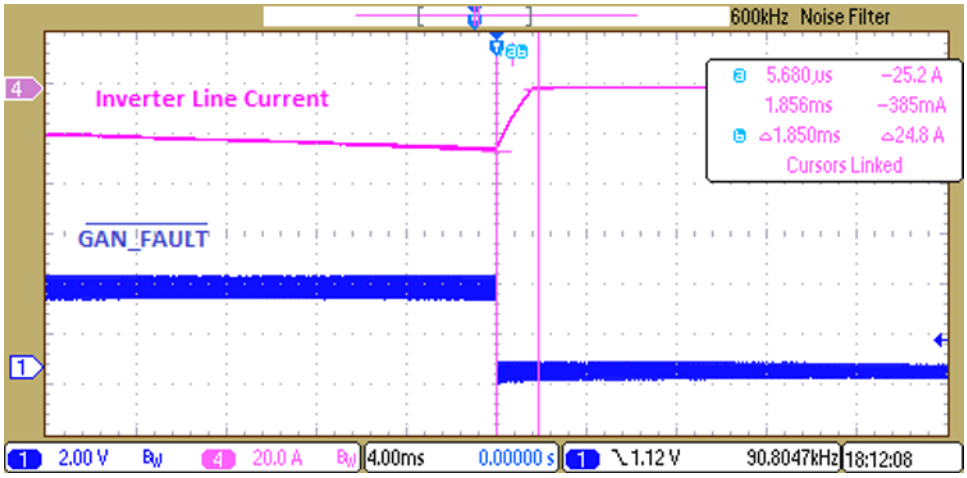


図 33. Overcurrent Fault Detection

The current triggering the $\overline{\text{FAULT}}$ signal low is about 24.8 A. The line current reduces to zero as the GaN FET carrying this current has been turned off internally. The PWM controller may use the $\overline{\text{FAULT}}$ feedback to turn off the remaining PWM.

注: All GaN FETs are protected from overcurrent at any time, and when overcurrent is detected, the turnoff is latched. The latched turnoff can only be removed if PWM signal is held low for 350 µs.

5 Design Files

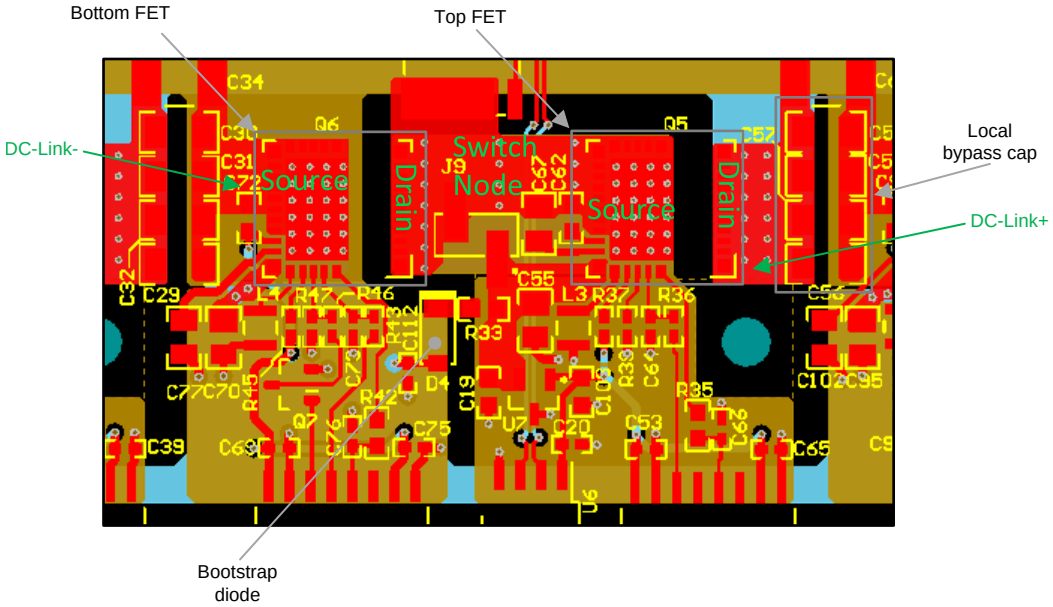
5.1 Schematics

To download the schematics, see the design files at TIDA-00915.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00915.

5.3 PCB Layout Recommendations



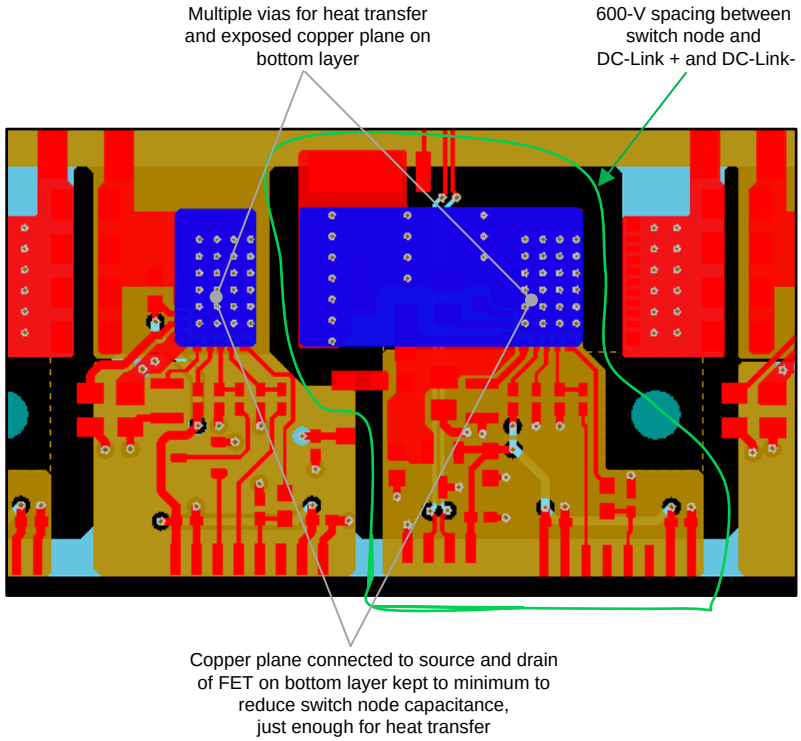


図 34. Layout Recommendation

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00915.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00915.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00915.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00915.

6 Software Files

To download the software files, see the design files at TIDA-00915.

7 Related Documentation

1. Texas Instruments, *High Voltage Half Bridge Design Guide for LMG3410 Smart GaN FET*, Application Report (SNOA946)
2. Texas Instruments, *GaN FET module performance advantage over silicon*, White Paper (SLYY071)

7.1 商標

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8 Terminology

GaN— Gallium nitride

IGBT— Isolated gate bipolar transistor

UVLO— Undervoltage lockout

CMTI— Common-mode transient immunity

HEMT— High electron mobility transistor

9 About the Authors

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