Simulation Report -
Basic ALU Design using Verilog

1. Objective

The objective of this project is to design and verify a basic Arithmetic Logic Unit (ALU) using Verilog HDL that supports arithmetic and logical operations such as Addition, Subtraction, AND, OR, and NOT. Simulation is performed to validate the functionality of the ALU using a testbench.

2. Tools Used

- HDL: Verilog
- Simulator: Xilinx Vivado (xsim)
- Operating System: Windows
- Target Design: Behavioral Simulation

3. ALU Design Description

The ALU is designed to perform arithmetic and logical operations based on a control signal (opcode). It accepts two input operands and produces an output corresponding to the selected operation.

Signal Type	Signals	Description
Input Signals	A	First input operand
	B	Second input operand
	SEL	Operational Select signal
Output Signal	Result	Output of the ALU

4. Supported Operations

Opcode	Operation
000	Addition
001	Subtraction
010	AND
011	OR
100	NOT

5. Testbench Description

A Verilog testbench is written to apply different input combinations and opcodes to the ALU. The testbench verifies each operation by monitoring the output result and observing the waveform behavior**.**

6. Simulation Procedure

1. The ALU design and testbench were compiled in Vivado.
2. Behavioral simulation was executed using xsim.
3. Input values and opcodes were applied through the testbench.
4. Output waveforms were observed and verified.
5. Simulation results were captured for documentation.

7. Simulation Results

The simulation waveforms confirm that the ALU operates correctly for all supported operations.

Waveform Observations

Addition: Correct sum observed for inputs A and B.

Subtraction: Correct difference observed.

AND / OR: Logical operations performed correctly.

NOT: Inversion of input observed correctly.

Figure 1: Addition Operation Waveform

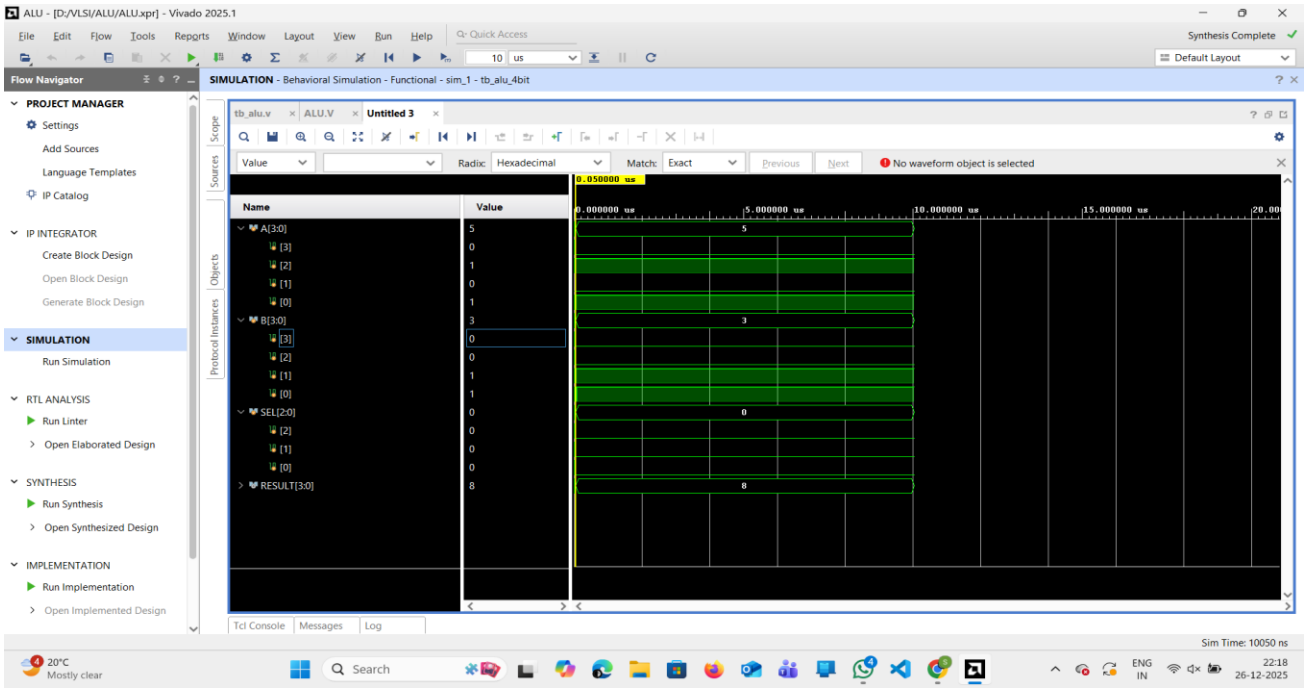


Figure 2: Subtraction Operation Waveform

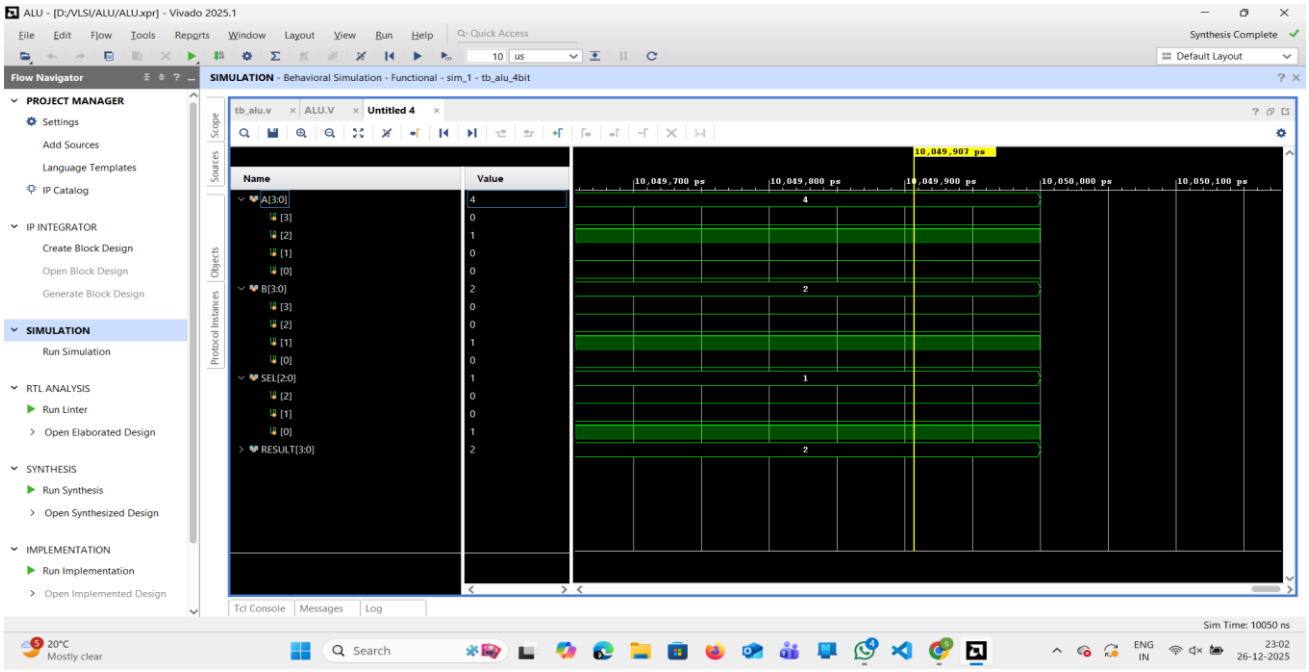
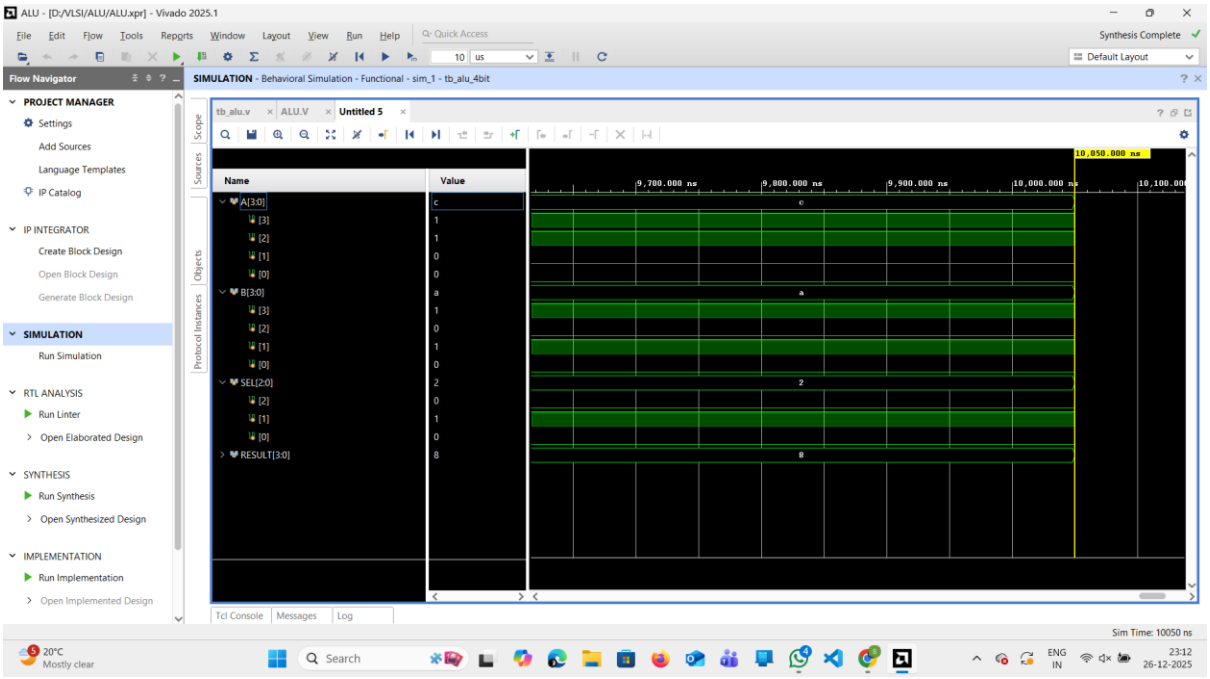
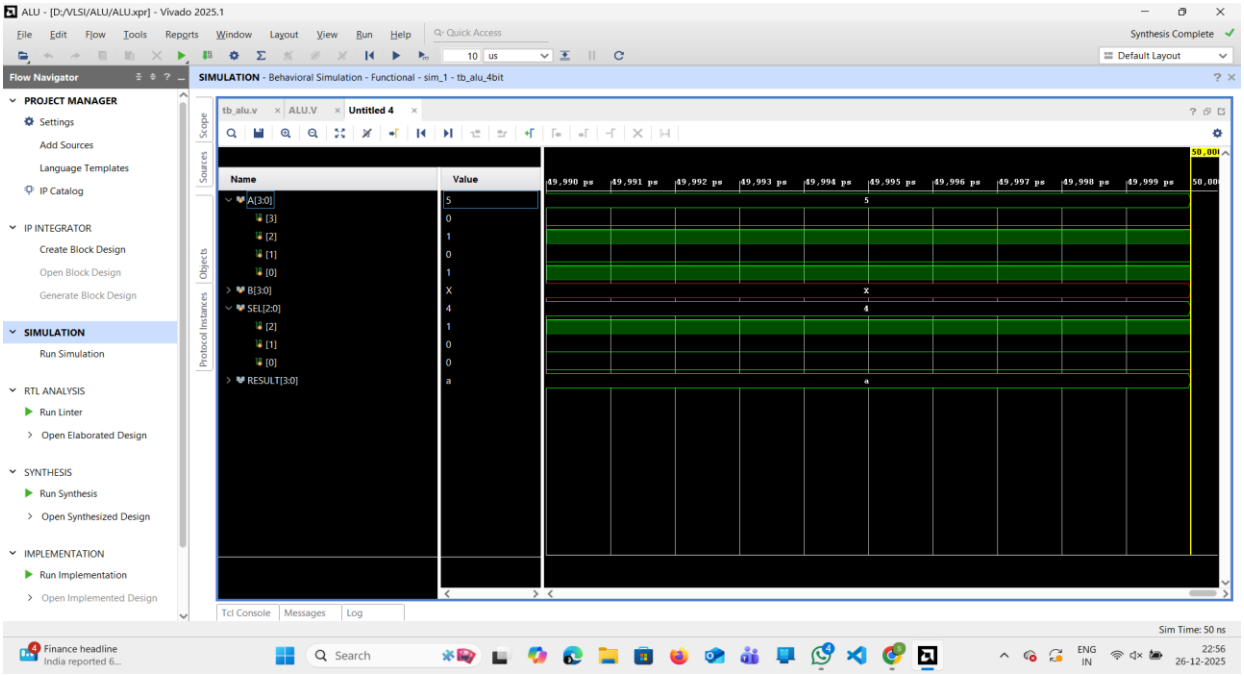


Figure 3: Logical Operations Waveform (AND, NOT)





8. Conclusion

The basic ALU was successfully designed and verified using Verilog HDL. Behavioral simulation results obtained from Vivado confirm correct functionality of all arithmetic and logical operations. The design meets the project requirements and operates as expected.