SRAM Design with Read and Write Operations Using Verilog

➢ Overview

This project focuses on the **design and verification of a Synchronous RAM (SRAM)** using **Verilog HDL**.

The RAM supports **read and write operations controlled by a clock and write enable signal**.

The design is verified using a **testbench and simulation in Vivado**, ensuring correct memory functionality.

➢ Problem Statement

Memory blocks are essential components in digital systems such as processors and controllers.

The challenge is to **design a reliable synchronous RAM module** that correctly stores and retrieves data based on control signals and clock timing, while ensuring predictable behavior during read and write operations.

➢ Objectives

- Design a synchronous RAM using Verilog HDL
- Implement clocked **read and write operations**
- Develop a testbench to verify RAM functionality
- Analyze simulation waveforms for correctness
- Understand RTL memory modeling and FPGA design flow

➢ Tools Used

- Verilog HDL – For RTL Design
- Xilinx Vivado – For Simulation, RTL analysis
- Vivado Simulator – For Behavioral waveform verification

➢ Architecture

The SRAM architecture consists of:

- **Memory Array** implemented using registers
- **Address Bus** to select memory location
- **Data Input (din)** and **Data Output (dout)**
- **Clock (clk)** for synchronous operation
- **Write Enable (we)** for controlling write operation

Signal	Width	Description
clk	1	Clock signal
we	1	Write enable
addr	4	Address input
din	8	Data input
dout	8	Data output

➢ Operation / Methodology

- **Functional Operation Table**

Condition	Operation
we = 1 & rising edge of clk	Data written to memory
we = 0 & rising edge of clk	Data read from memory
Address changes	Selects memory location
Initial state	Output undefined (X)

- **Methodology Flow**

1. On **posedge clk**, check we
2. If we = 1, write din to memory at addr
3. If we = 0, read data from memory at addr
4. Output data through registered output (dout)

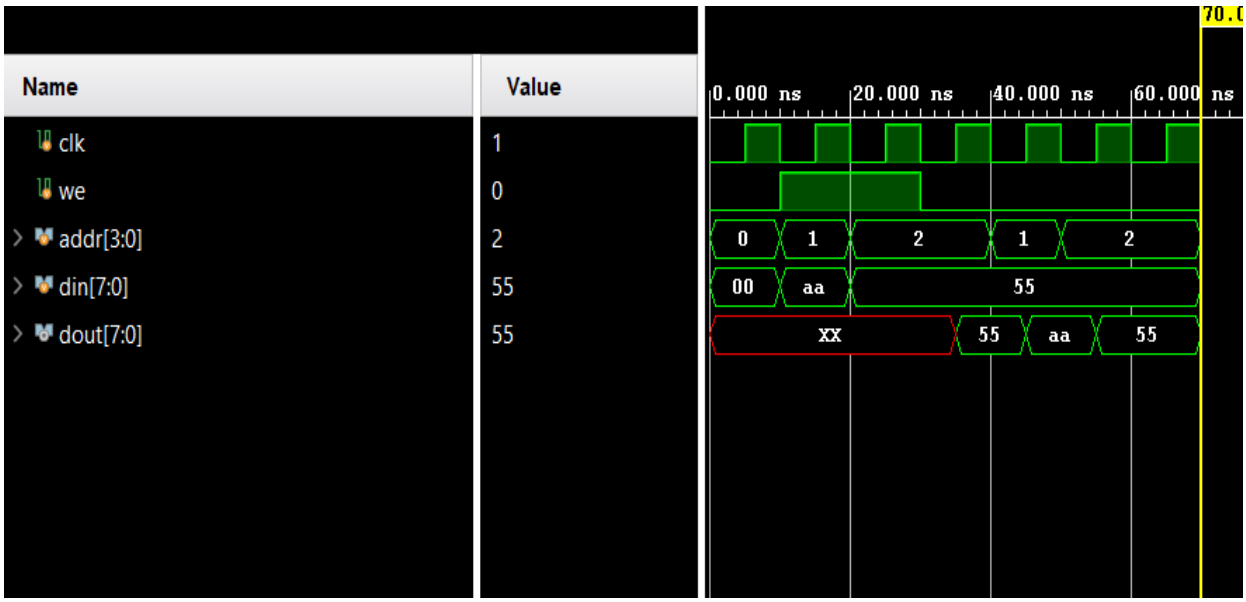
➢ Simulation & Testbench

- A dedicated **testbench** was created to generate:
  - Clock signal
  - Write enable transitions
  - Address and data patterns
- Multiple write operations were performed followed by read operations
- Simulation waveforms were observed to verify correct behavior

➢ Results

- Data was successfully written to the selected memory addresses
- Read operations retrieved the correct stored values
- Simulation waveforms confirmed:
  - Synchronous write behavior
  - Stable and correct data output
- RTL schematic and device views validated correct design inference

Figure 1: SRAM Waveforms



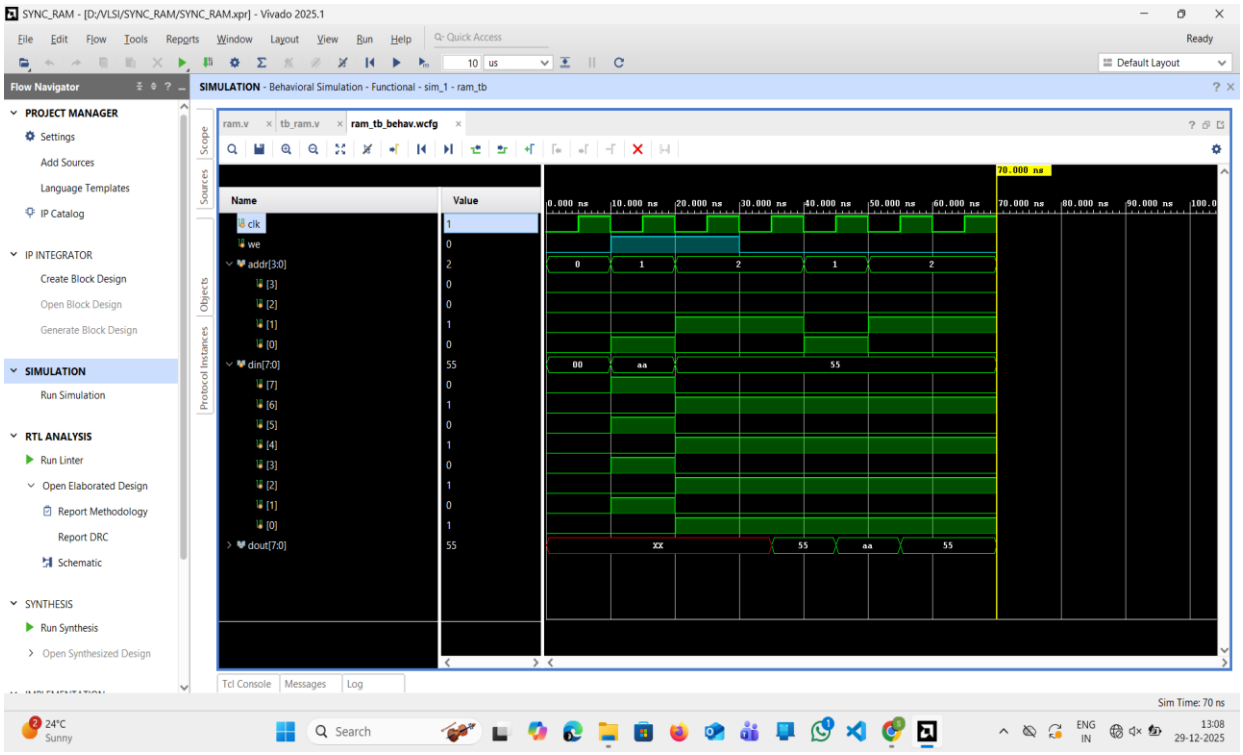
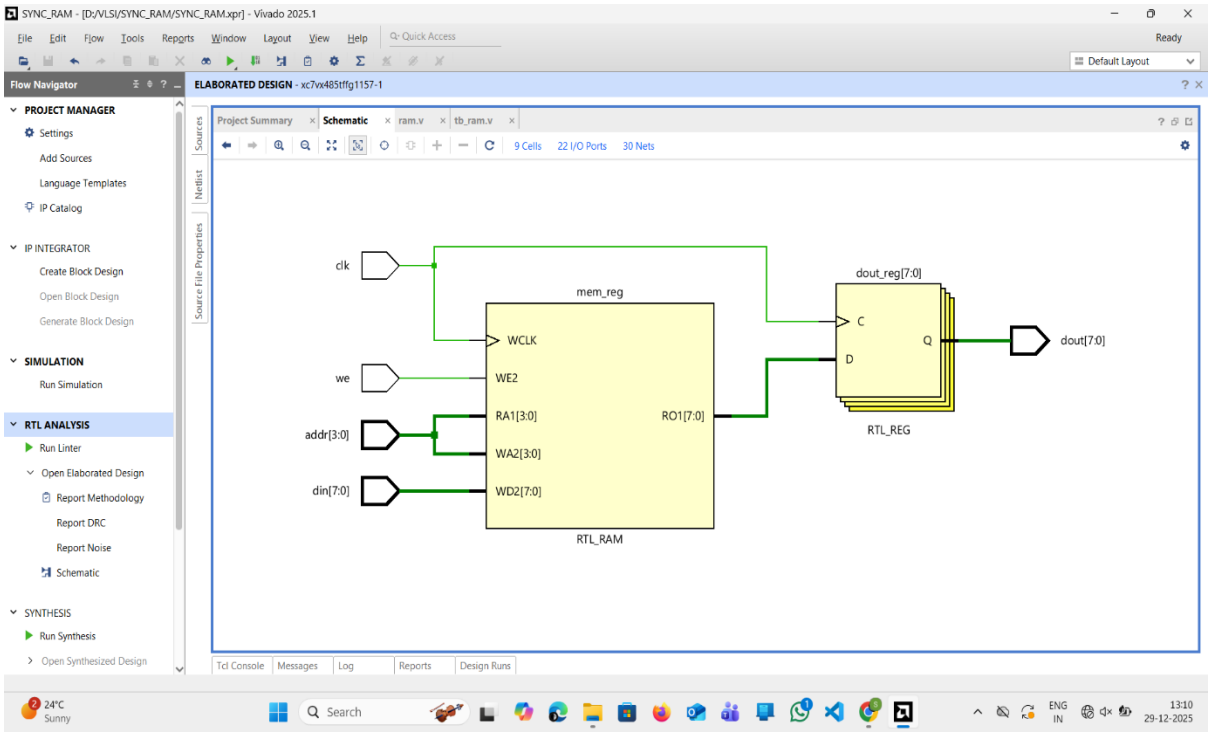
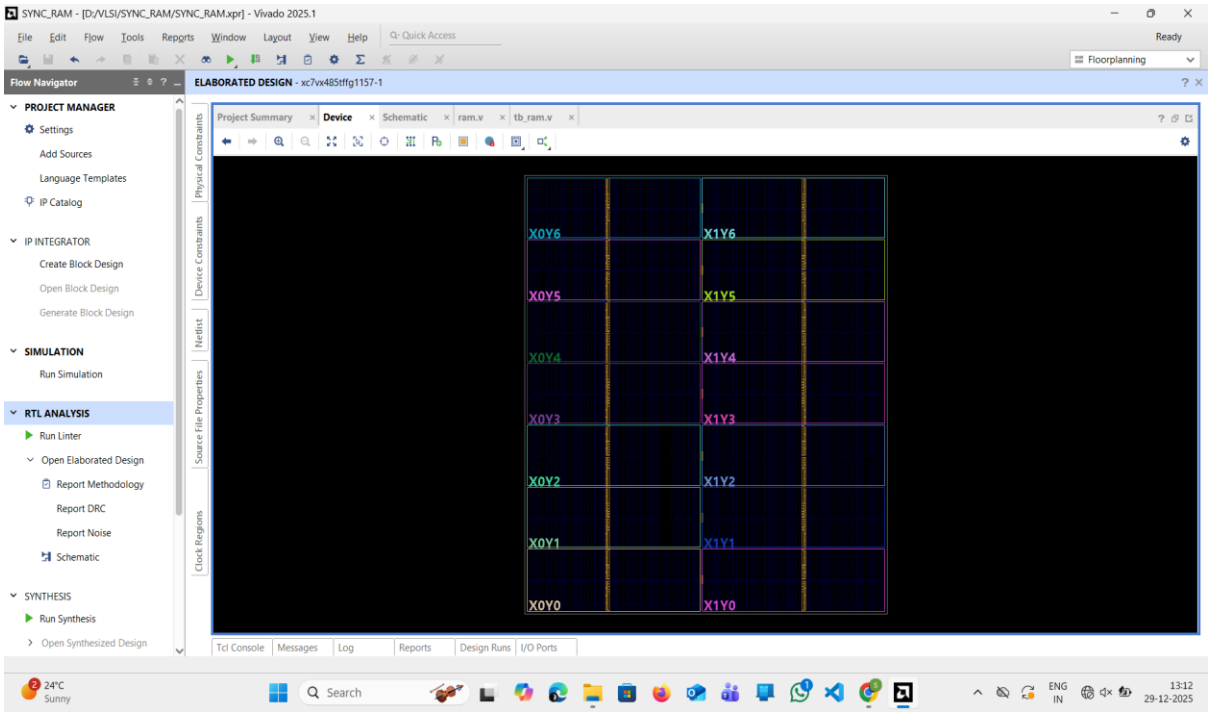


Figure 2: Schematic & Layouts

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File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
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ELABORATED DESIGN - xc7vx485tffg1157-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
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Create Block Design
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SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Project Summary
Device
Schematic
ram.v
tb_ram.v
Physical Constraints
Device Constraints
Netlist
Source File Properties
Clock Regions
X0Y6
X1Y6
X0Y5
X1Y5
X0Y4
X1Y4
X0Y3
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X0Y2
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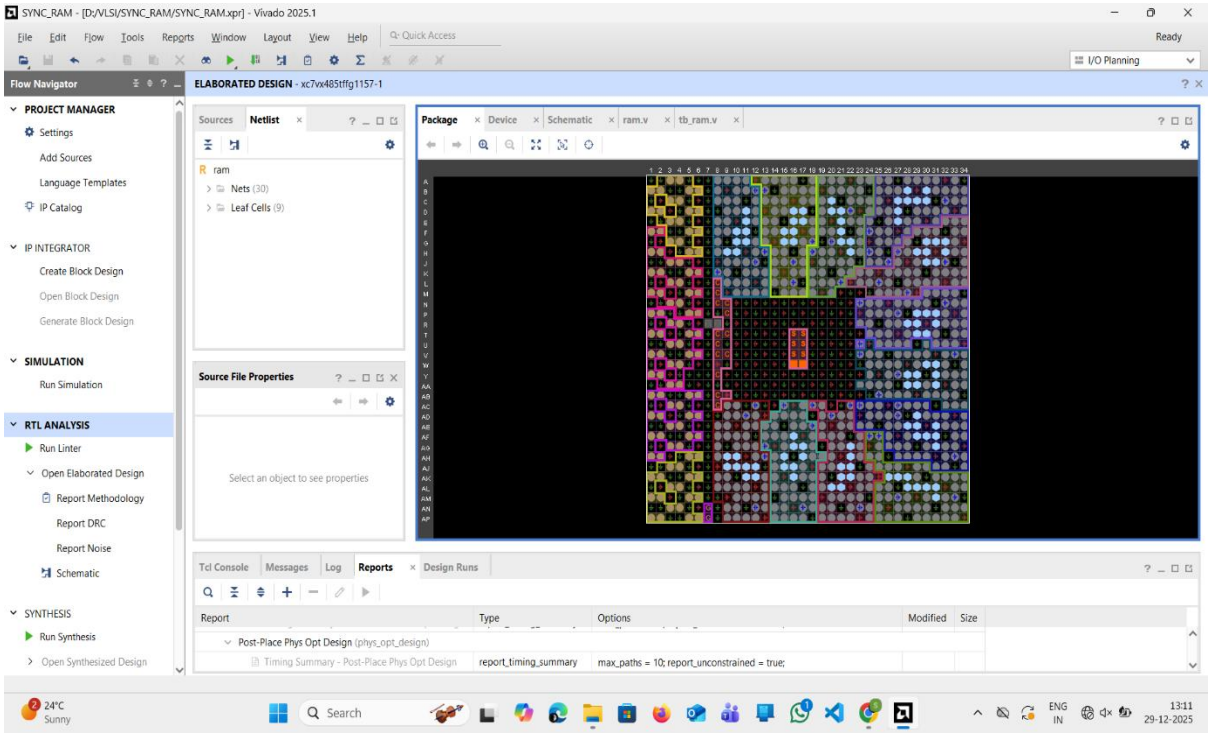
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Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Sources
Netlist
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Leaf Cells (9)
Source File Properties
Select an object to see properties
Package
Device
Schematic
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tb_ram.v
Tcl Console
Messages
Log
Reports
Design Runs
Report
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Options
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➢ Applications

- Memory blocks in digital systems
- FPGA-based designs
- Learning RTL memory modeling
- VLSI and digital design education

➢ Limitations

- Ideal memory model (no timing delays)
- No power or area optimization
- Not optimized for ASIC fabrication
- Single-port memory only

➢ Conclusion

The project successfully demonstrates the **design and verification of a synchronous RAM using Verilog HDL**.
Simulation results confirm correct read and write operations, making this design suitable for educational use and as a foundation for advanced memory architectures in VLSI systems.