Multicore Computers

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- Komputer multi-core adalah sistem yang menggunakan lebih dari satu core dalam satu chip prosesor
- Tujuan: meningkatkan kinerja, efisiensi daya, dan kemampuan multitasking.
- Setiap core: memiliki register, unit aritmatika-logika (ALU), unit kontrol, dan cache L1.
- **Interconnect**: Jalur komunikasi antara core dan komponen lain dalam prosesor serta antara prosesor dan memori utama.

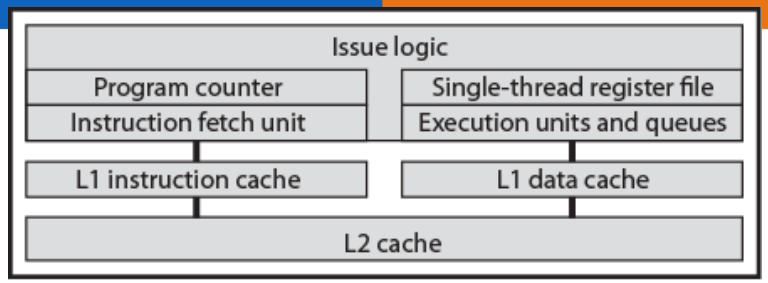
Contoh Prosesor Multi-Core

- Intel Core Series: Prosesor seperti Intel Core i3, i5, i7, dan i9, yang memiliki beberapa core (biasanya 2, 4, 6, 8, atau lebih).
- AMD Ryzen: Prosesor yang juga memiliki beberapa core dan dikenal karena kinerja multi-core yang kuat.
- ARM Cortex-A Series: Digunakan dalam banyak perangkat mobile dan embedded, seperti smartphone dan tablet, dengan berbagai konfigurasi core.

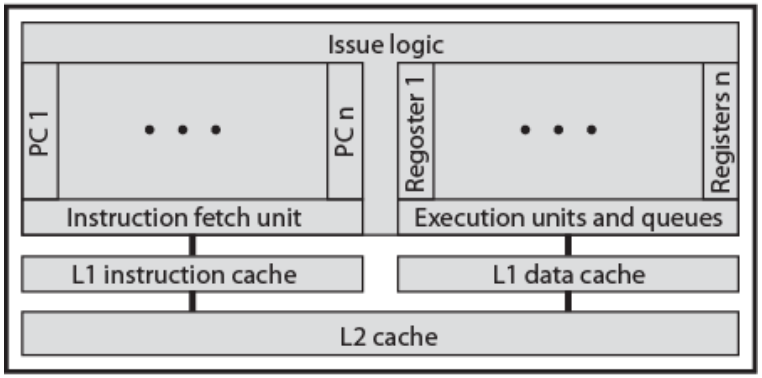
Hardware Performance Issues (masalah)

- Microprocessors telah mengalami peningkatan kinerja secara eksponensial
  - Improved organization
  - Increased clock frequency
- Increase in Parallelism
  - Pipelining
  - Superscalar: terdiri dari beberapa pipeline
  - Simultaneous multithreading (SMT): beberapa thread (utas) dieksekusi secara bersamaan pada satu core prosesor fisik.
- Hasil yang semakin berkurang
  - Kompleksitas yang lebih besar membutuhkan lebih banyak logika
  - Increasing chip area for coordinating and signal transfer logic
    - Harder to design, make and debug

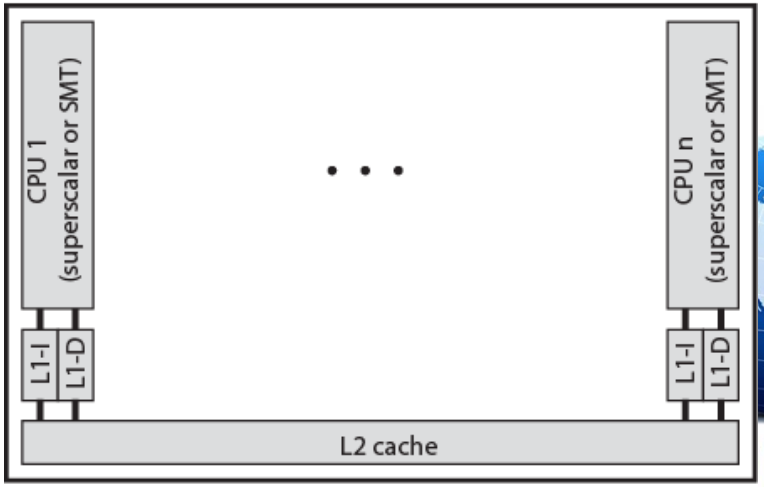
Alternative Chip Organizations



(a) Superscalar



(b) Simultaneous multithreading

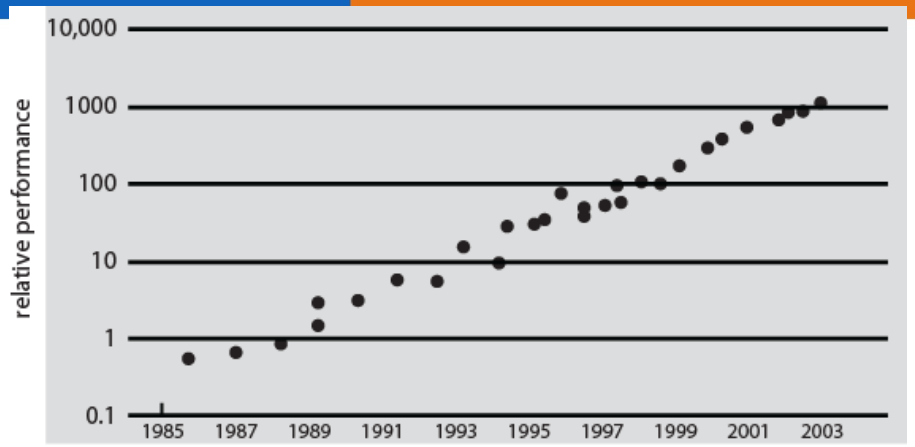


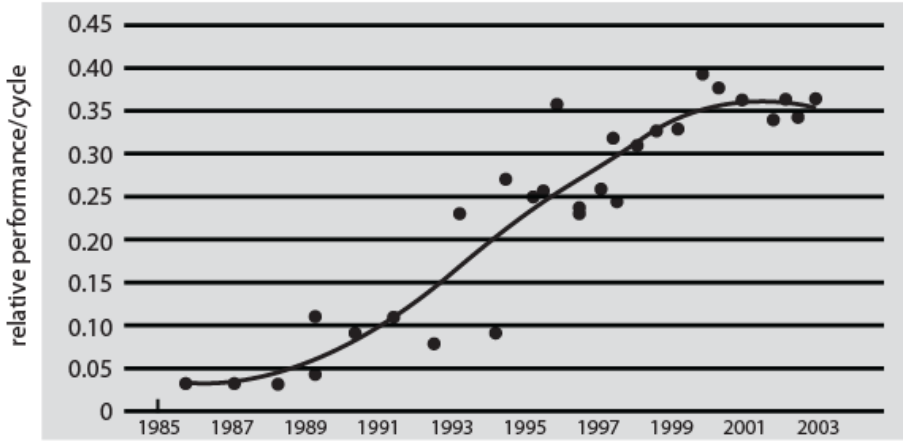
(c) Multicore

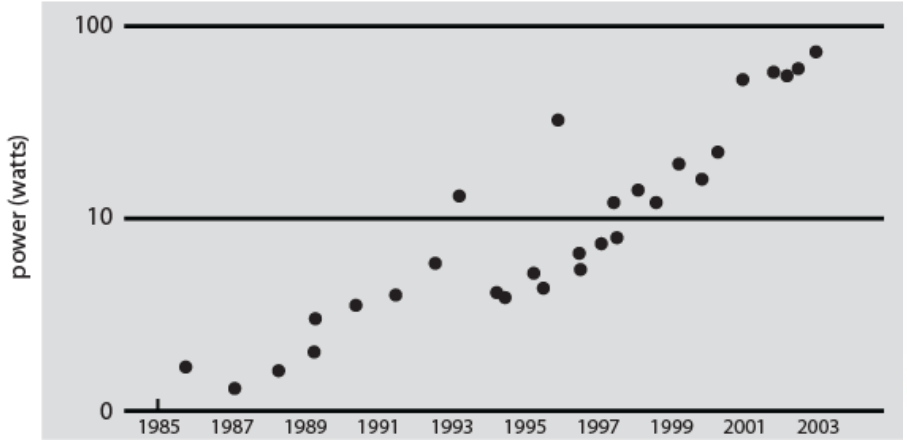
L1-I (Level 1 Instruction Cache):

L1-D (Level 1 Data Cache):

Intel Hardware Trends



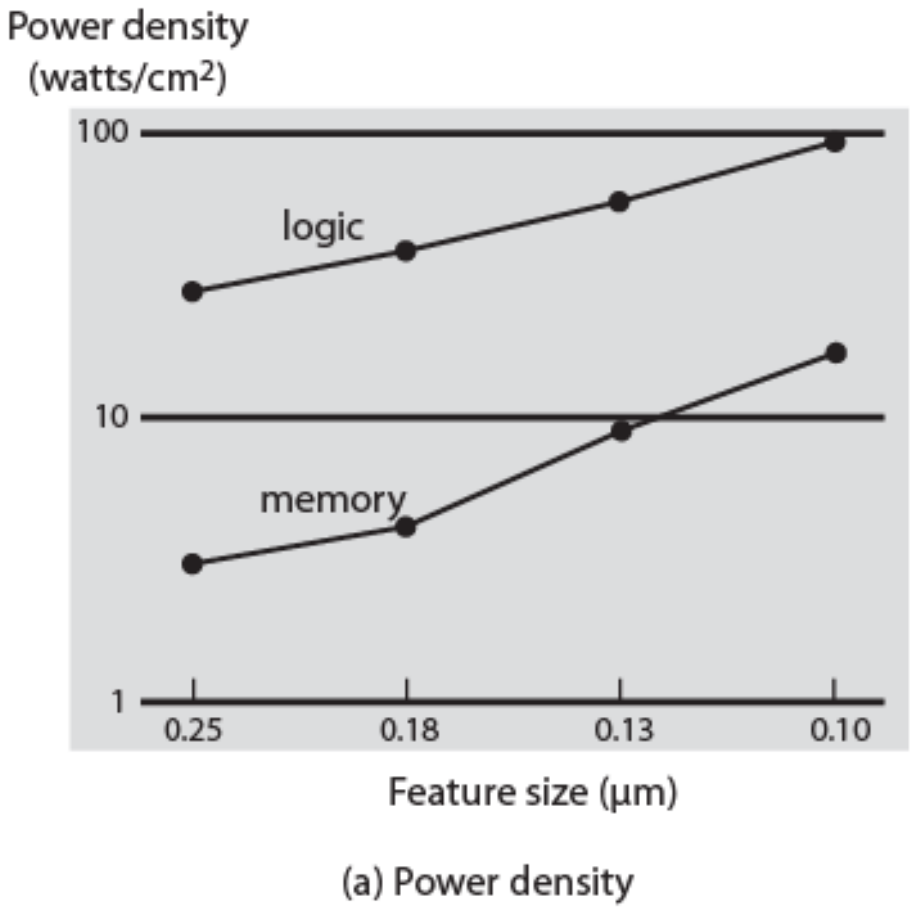




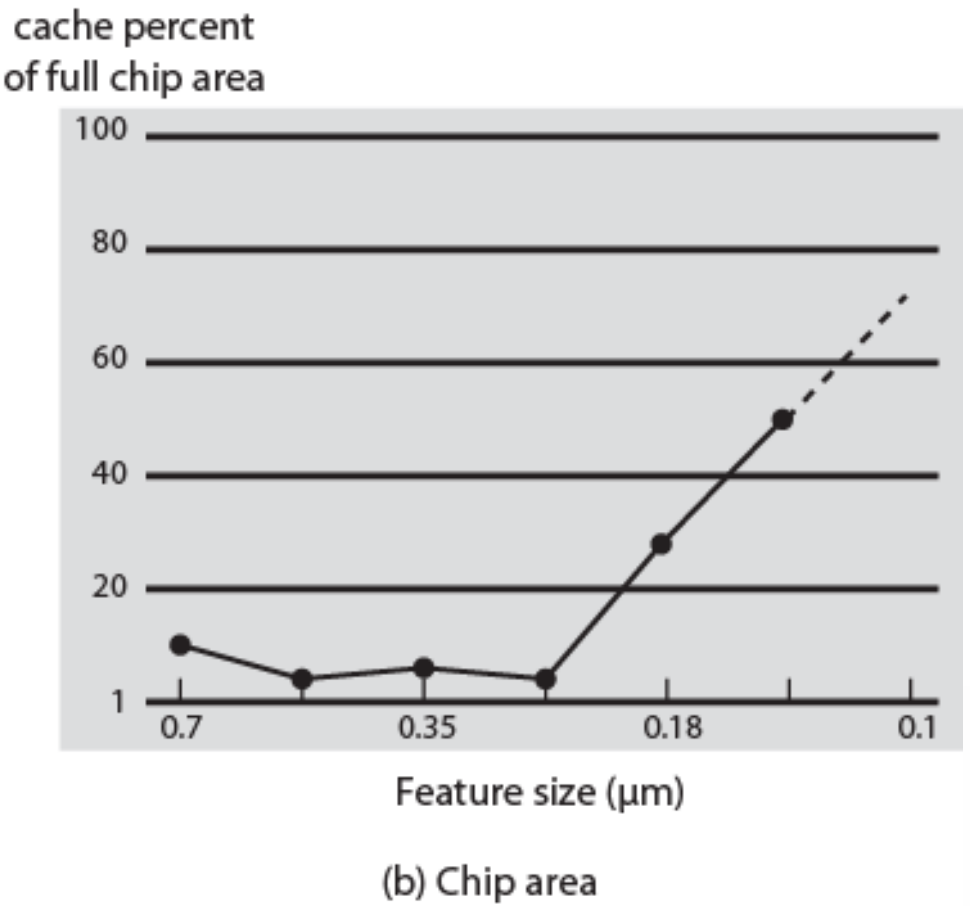
Increased Complexity

- Kebutuhan daya tumbuh secara eksponensial seiring dengan kepadatan chip dan frekuensi clock
  - Dapat menggunakan lebih banyak area chip untuk cahce
    - Lebih kecil
    - Urutan kebutuhan daya yang lebih rendah
- By 2015
  - 100 billion transistors on 300mm^2 die (kepadatan transistor)
    - Cache of 100MB
    - 1 billion transistors for logic
- Pollack's rule:
  - Kinerja kira-kira sebanding dengan akar kuadrat peningkatan kompleksitas
    - Double complexity gives 40% more performance
- Multicore memiliki potensi peningkatan yang hampir linier
- Tidak mungkin satu inti dapat menggunakan semua cache secara efektif

Pertimbangan Power dan Memory

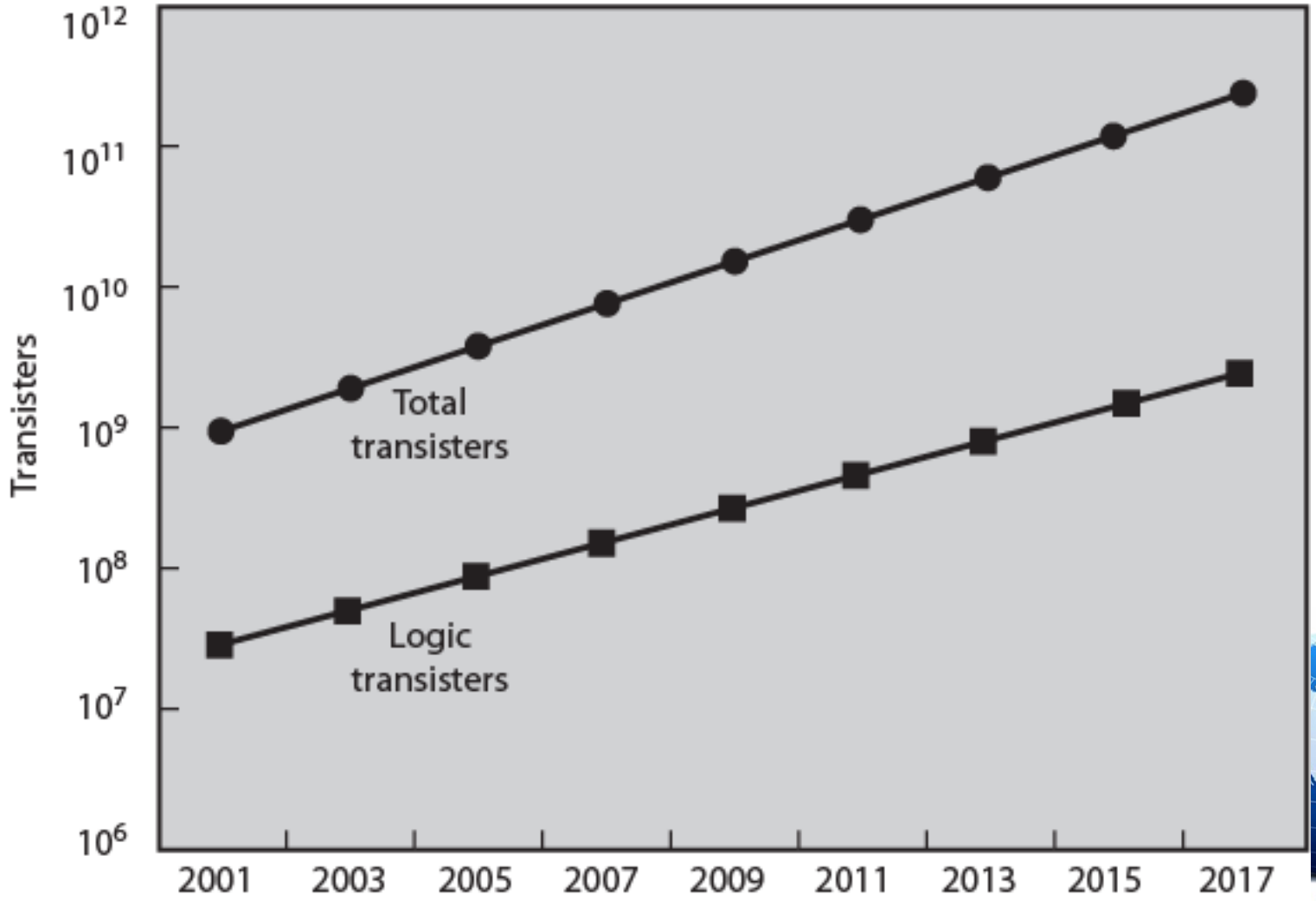


(a) Power density



(b) Chip area

Pemanfatan Chip Transistor



Software Performance Issues

- Manfaat kinerja bergantung pada eksploitasi sumber daya paralel yang efektif
- Bahkan sejumlah kecil kode serial akan berdampak pada kinerja
  - 10% serial inheren pada sistem prosesor 8 hanya memberikan kinerja 4,7 kali lipat
- Communication, distribution of work and cache coherence overheads
- Beberapa aplikasi secara efektif mengeksploitasi prosesor multicore

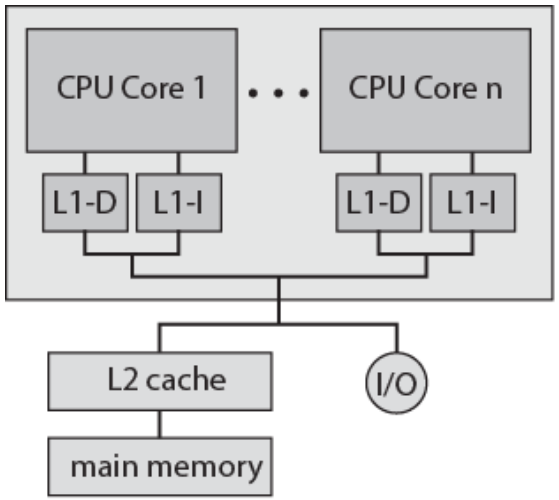
Effective Applications for Multicore Processors

- Database
- Servers handling independent transactions
- Multi-threaded native applications
  - Lotus Domino, Siebel CRM
- Multi-process applications
  - Oracle, SAP, PeopleSoft
- Java applications
  - Java VM is multi-thread with scheduling and memory management
  - Sun's Java Application Server, BEA's Weblogic, IBM Websphere, Tomcat
- Multi-instance applications
  - One application running multiple times
- E.g. Value Game Software

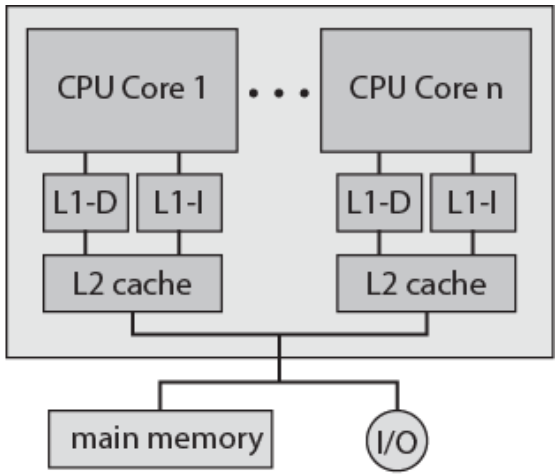
Multicore Organization

- Number of core processors on chip
- Number of levels of cache on chip
- Amount of shared cache
- Next slide examples of each organization:
- (a) ARM11 MPCore
- (b) AMD Opteron
- (c) Intel Core Duo
- (d) Intel Core i7

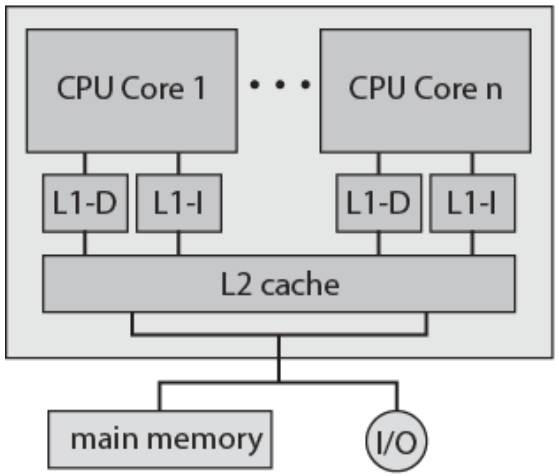
Multicore Organization



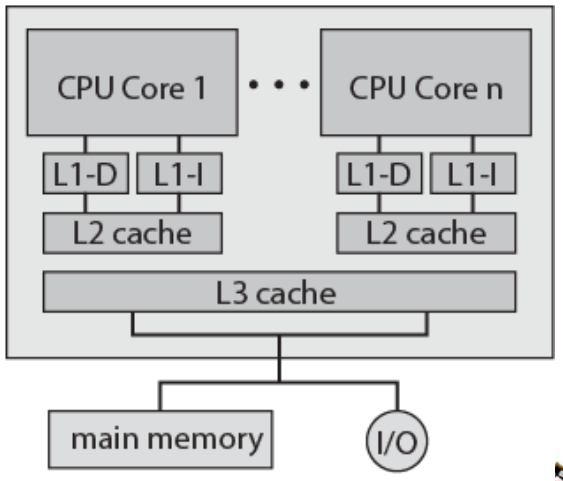
(a) Dedicated L1 cache



(b) Dedicated L2 cache



(c) Shared L2 cache



(d) Shared L3 cache

Advantages of shared L2 Cache

- Interferensi konstruktif mengurangi tingkat kesalahan secara keseluruhan
- Data yang dishare oleh multiple cores tidak direplikasi pada level cache
- Dengan algoritma frame replacement yang tepat berarti jumlah cache bersama yang didedikasikan untuk setiap core bersifat dinamis
  - Threads with less locality can have more cache
- Komunikasi antar proses yang mudah melalui memori bersama
- Cache coherency terbatas pada L1
- Cache L2 khusus memberi setiap core akses yang lebih cepat
  - Good for threads with strong locality
- Cache L3 bersama juga dapat meningkatkan kinerja

Individual Core Architecture

- Intel Core Duo menggunakan superscalar cores
- Intel Core i7 menggunakan simultaneous multi-threading (SMT)
  - Meningkatkan jumlah threads yang disupport
    - 4 SMT cores, masing-masing mendukung 4 threads muncul sebagai 16 core

Intel x86 Multicore Organization - Core Duo (1)

- 2006
- Two x86 superscalar, shared L2 cache
- Dedicated L1 cache per core
  - 32KB instruction and 32KB data
- Unit Thermal control per core
  - Mengelola pembuangan panas chip
  - Memakasimalkan kinerja dalam Batasan.
  - Peningkatan ergonomics
- Advanced Programmable Interrupt Controlled (APIC)
  - Inter-process menginterupsi antar cores
  - Merutekan interupsi ke core yang sesuai
  - Termasuk pengatur timer sehingga OS dapat interupsi core

Intel x86 Multicore Organization - Core Duo (2)

- Power Management Logic
  - Memonitor kondisi panas dan aktivitas CPU
  - Menyesuaikan voltage dan power consumption
  - Dapat mengganti individual logic subsystems
- 2MB shared L2 cache
  - Dynamic allocation
  - MESI support for L1 caches
  - Diperluas untuk mendukung multiple Core Duo in SMP
    - L2 data shared between local cores or external
- Bus interface

Intel x86 Multicore Organization - Core i7

- November 2008
- Empat x86 SMT processors
- Dedicated L2, shared L3 cache
- Speculative pre-fetch for caches
- On chip DDR3 memory controller
  - Tiga 8 byte channels (192 bits) memberikan 32GB/s
  - No front side bus
- QuickPath Interconnection
  - Cache coherent point-to-point link
  - High speed communications antara processor chips
  - 6.4G transfers per second, 16 bits per transfer
  - Dedicated bi-directional pairs
  - Total bandwidth 25.6GB/s

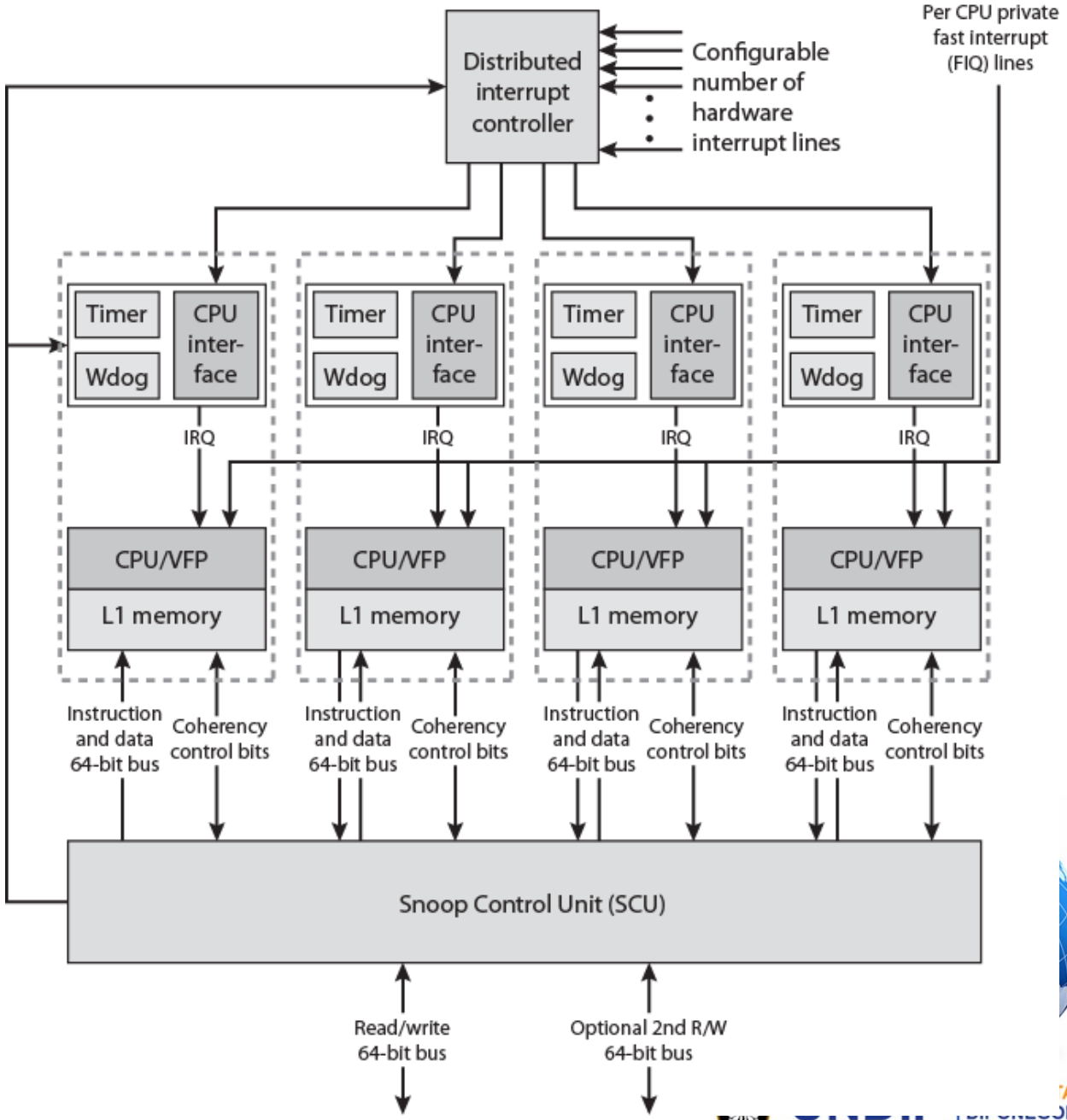
Comparation i7

	Core i7-7820X	Core i7-8700K	Core i9-9900K	Core i7-9700K
Release Date	June 2017	October 2017	October 2018	
Cores / Threads	8/16	6/12	8/16	8/8
Base Frequency	3.6 GHz	3.5 GHz	3.6 GHz	3.6 GHz
Max Boost Frequency	4.3 GHz	4.7 GHz	5.0 GHz	4.9 GHz
L2 Cache	8 MB	1.5 MB	2 MB	2 MB
L3 Cache	11 MB	12 MB	16 MB	12 MB
Memory Config	Quad-Channel	Dual-Channel		
Max Mem Support	DDR4-2666			
TDP	140 W	95 W		
MSRP	$600	$360	$500	$374

ARM11 MPCore

- Up to 4 processors each with own L1 instruction and data cache
- Distributed interrupt controller
- Timer per CPU
- Watchdog
  - Warning alerts for software failures
  - Counts down from predetermined values
  - Issues warning at zero
- CPU interface
  - Interrupt acknowledgement, masking and completion acknowledgement
- CPU
  - Single ARM11 called MP11
- Vector floating-point unit
  - FP co-processor
- L1 cache
- Snoop control unit
  - L1 cache coherency

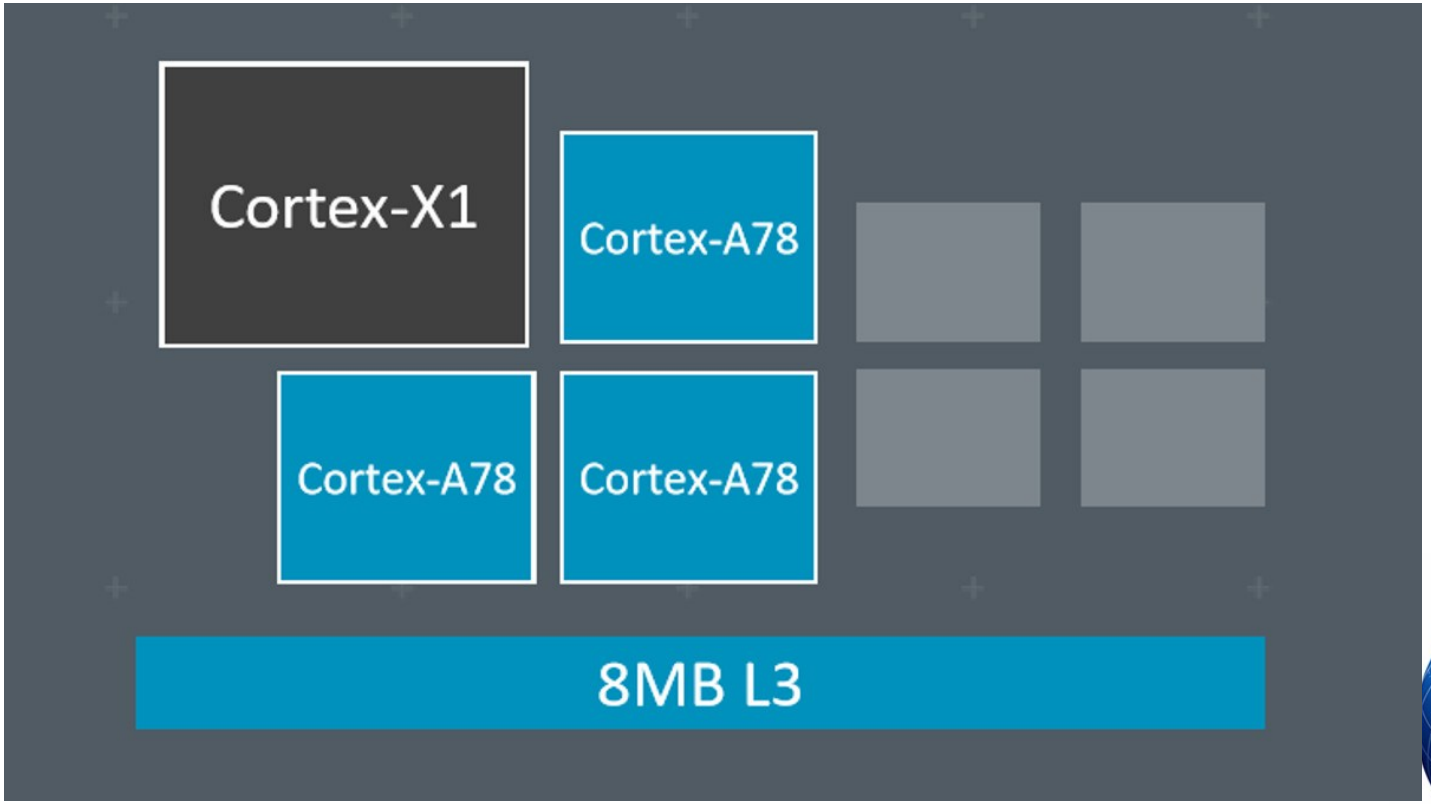
ARM11 MPCore Block Diagram



ARM11 MPCore Interrupt Handling

- Distributed Interrupt Controller (DIC) collates from many sources
- Masking
- Prioritization
- Distribution to target MP11 CPUs
- Status tracking
- Software interrupt generation
- Number of interrupts independent of MP11 CPU design
- Memory mapped
- Accessed by CPUs via private interface through SCU
- Can route interrupts to single or multiple CPUs
- Provides inter-process communication
  - Thread on one CPU can cause activity by thread on another CPU

New ARM Cortex



DIC Routing

- Direct to specific CPU
- To defined group of CPUs
- To all CPUs
- OS can generate interrupt to:
  - All but self
  - Self
  - Other specific CPU
- Typically combined with shared memory for inter-process communication
- 16 interrupt ids available for inter-process communication

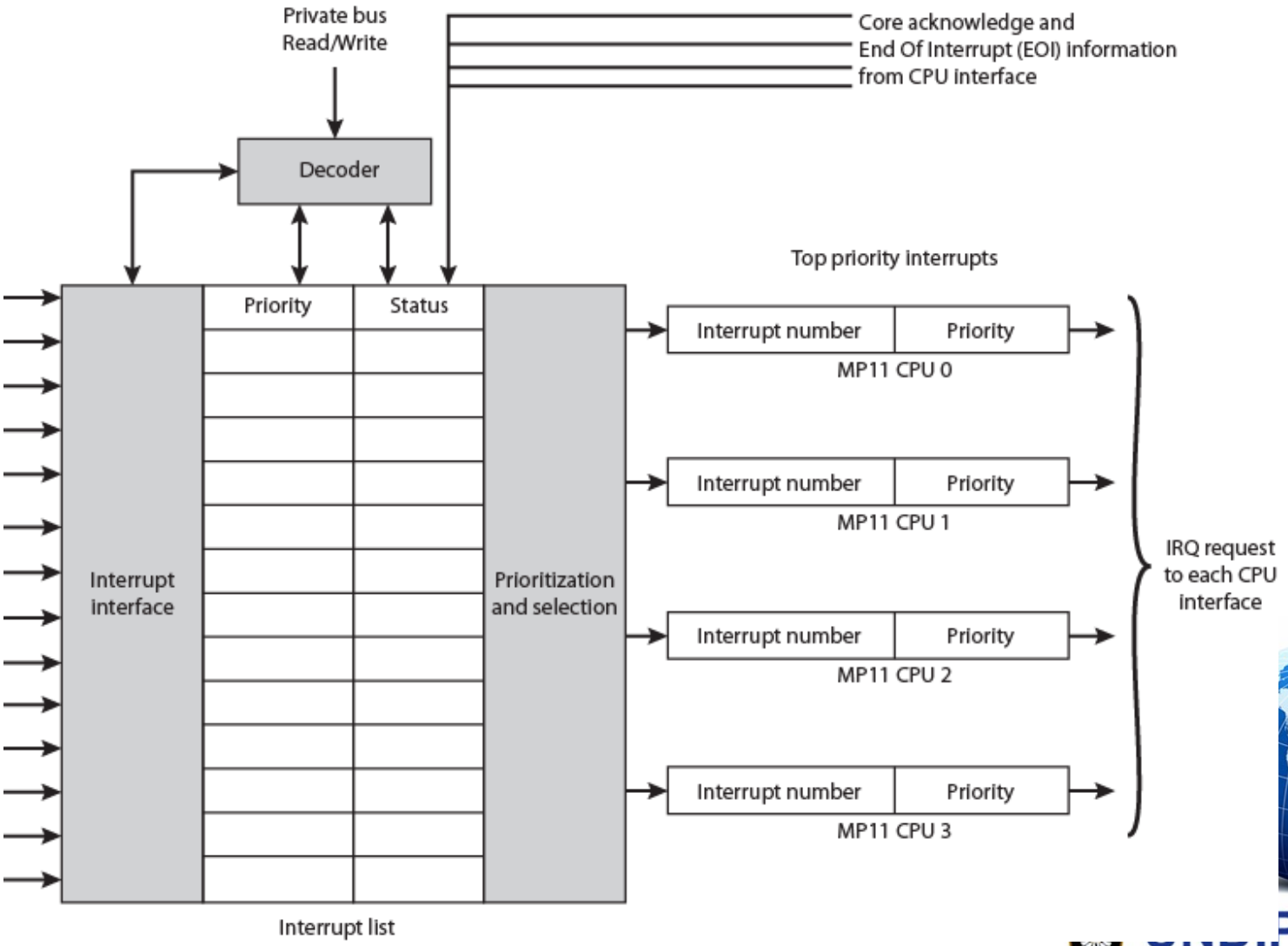
Interrupt States

- Inactive
  - Non-asserted
  - Completed by that CPU but pending or active in others
- Pending
  - Asserted
  - Processing not started on that CPU
- Active
  - Started on that CPU but not complete
  - Can be pre-empted by higher priority interrupt

Interrupt Sources

- Inter-process Interrupts (IPI)
  - Private to CPU
  - ID0-ID15
  - Software triggered
  - Priority depends on target CPU not source
- Private timer and/or watchdog interrupt
  - ID29 and ID30
- Legacy FIQ line
  - Legacy FIQ pin, per CPU, bypasses interrupt distributor
  - Directly drives interrupts to CPU
- Hardware
  - Triggered by programmable events on associated interrupt lines
  - Up to 224 lines
  - Start at ID32

ARM11 MPCore Interrupt Distributor



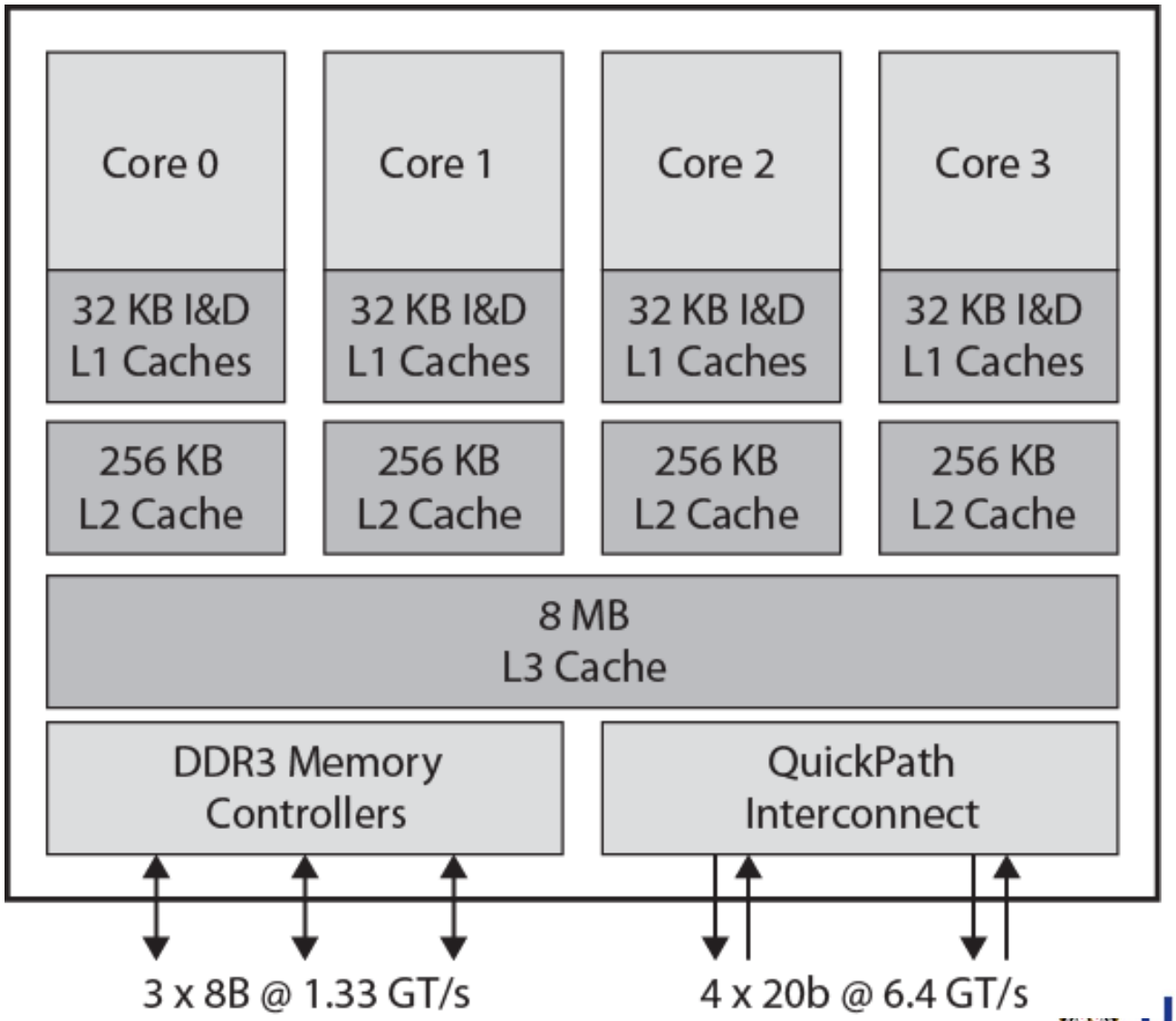
Cache Coherency

- Snoop Control Unit (SCU) resolves most shared data bottleneck issues
- L1 cache coherency based on MESI
- Direct data Intervention
  - Copying clean entries between L1 caches without accessing external memory
  - Reduces read after write from L1 to L2
  - Can resolve local L1 miss from rmote L1 rather than L2
- Duplicated tag RAMs
  - Cache tags implemented as separate block of RAM
  - Same length as number of lines in cache
  - Duplicates used by SCU to check data availability before sending coherency commands
  - Only send to CPUs that must update coherent data cache
- Migratory lines
  - Allows moving dirty data between CPUs without writing to L2 and reading back from external memory

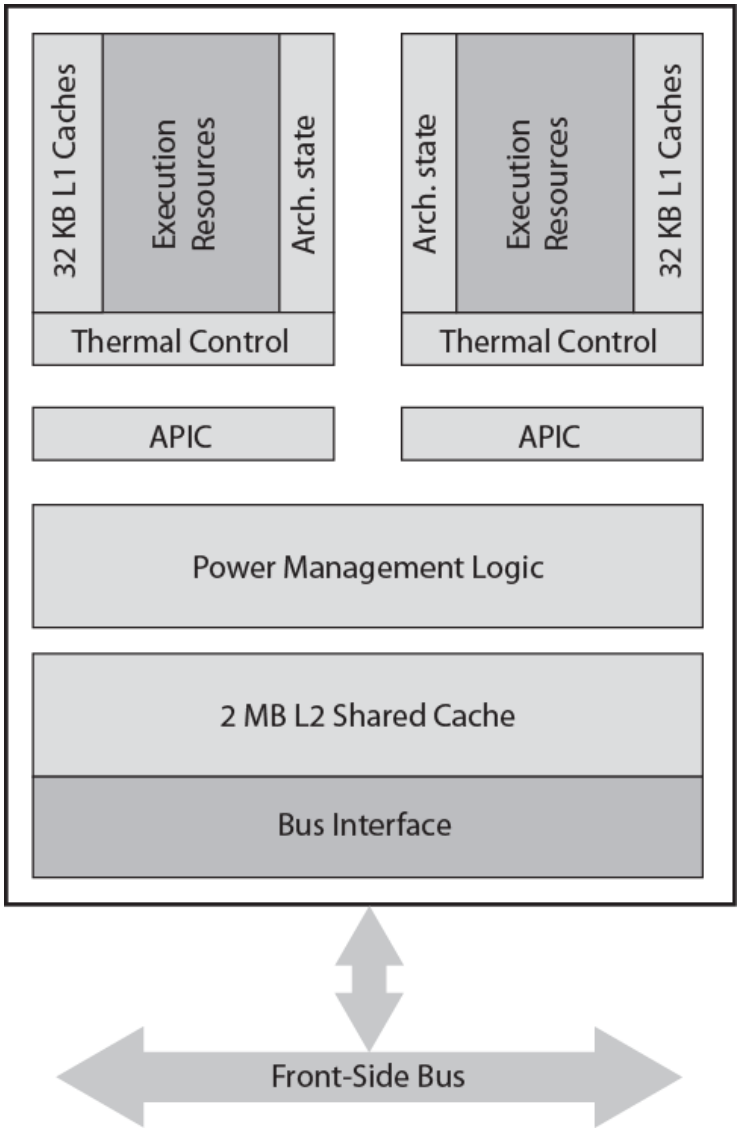
Recommended Reading

- Stallings chapter 18
- ARM web site

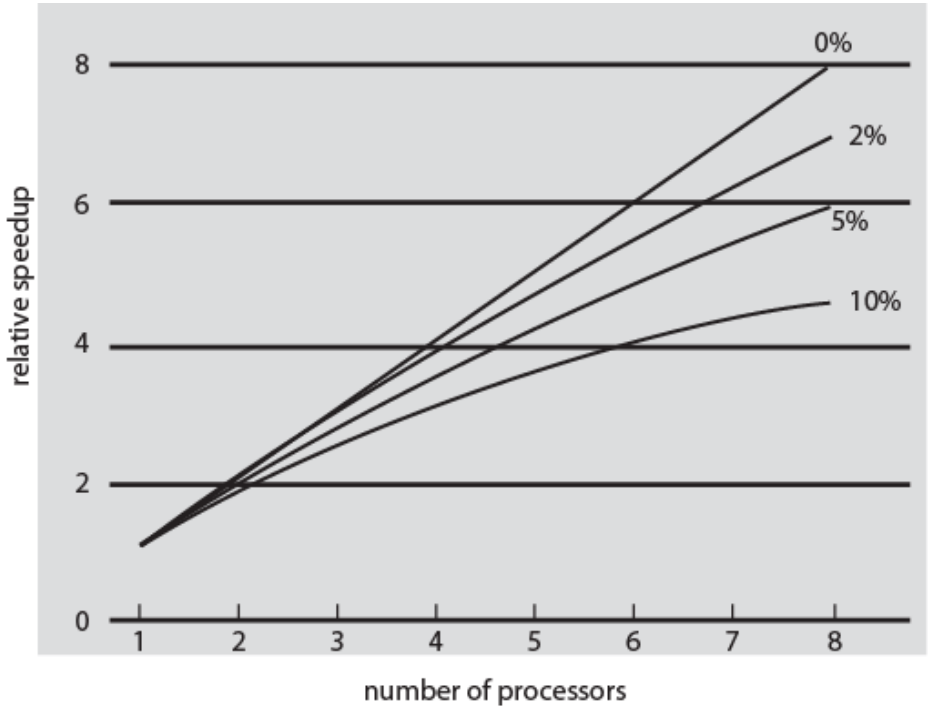
Intel Core i7 Block Diagram



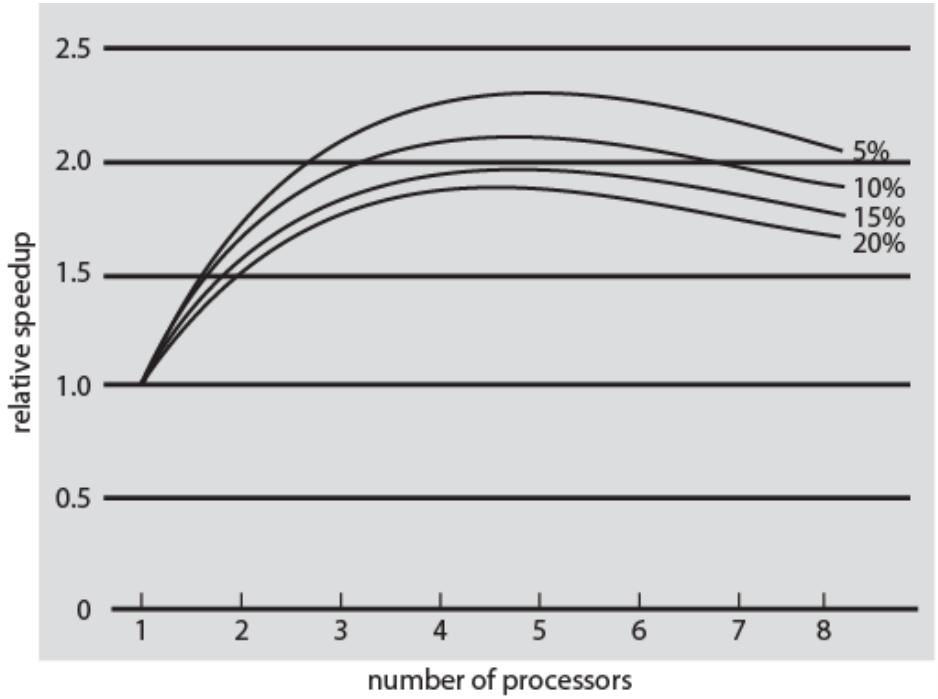
Intel Core Duo Block Diagram



Performance Effect of Multiple Cores



(a) Speedup with 0%, 2%, 5%, and 10% sequential portions



(b) Speedup with overheads

Recommended Reading

- Multicore Association web site
- ARM web site

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