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Lab 8: Synchronous Sequential Circuits

A. Objectives

• Gain a practical understanding of State Diagrams and State Tables.
• Understand the concept of designing Sequential Circuits using Flip-Flops.
• Design and implement a Synchronous Sequential Circuit given a State Diagram.

B. Theory

Synchronous Sequential Circuits: A sequential circuit, consists of a combinational circuit to which storage elements are connected to form a feedback path. The storage elements, usually Flip-Flops are devices capable of storing binary information. The sequential circuit receives binary information from external inputs that, together with the present state of the storage elements, determine the binary value of the outputs. The next state of the storage elements is a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states. In contrast, the outputs of combinational logic depend only on the present values of the inputs.

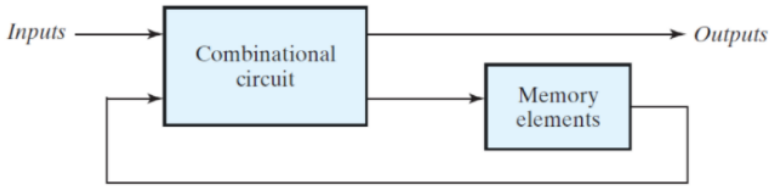


Figure B1: Sequential Circuit: Block Diagram

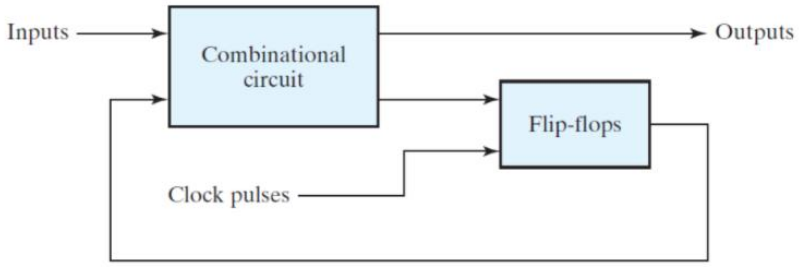


Figure B2: Synchronous Sequential Circuit: Block Diagram

New Apparatus:

- IC 7474 (Dual D Flip-Flops)
- IC 74107 (Dual JK Flip-Flops)

Experiment 1: Constructing a Sequential Circuit using JK Flip-Flops

C.1 Apparatus

- Trainer board
- 1 x IC 74107 JK Flip-Flop
- 1 x IC 7408 2-input AND gates
- 1 x IC 7404 Hex inverters (NOT gates)

Present State		Input	Next State		Output	Flip-Flop Input Functions			
A	**B**	**X**	**A**	**B**	**Y**	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0	0	1	0	0	x	x	0
0	1	1	1	0	1	1	x	x	1
1	0	0	1	0	0	x	0	0	x
1	0	1	0	0	0	x	1	0	x
1	1	0	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x

Table F.1.1: State Table for circuit using JK Flip-Flops

0	1	1	0
x	x	x	x

$J_A = X$

x	x	x	x
0	1	x	x

$K_A = X$

1	0	x	x
0	0	x	x

$J_B = A'X'$

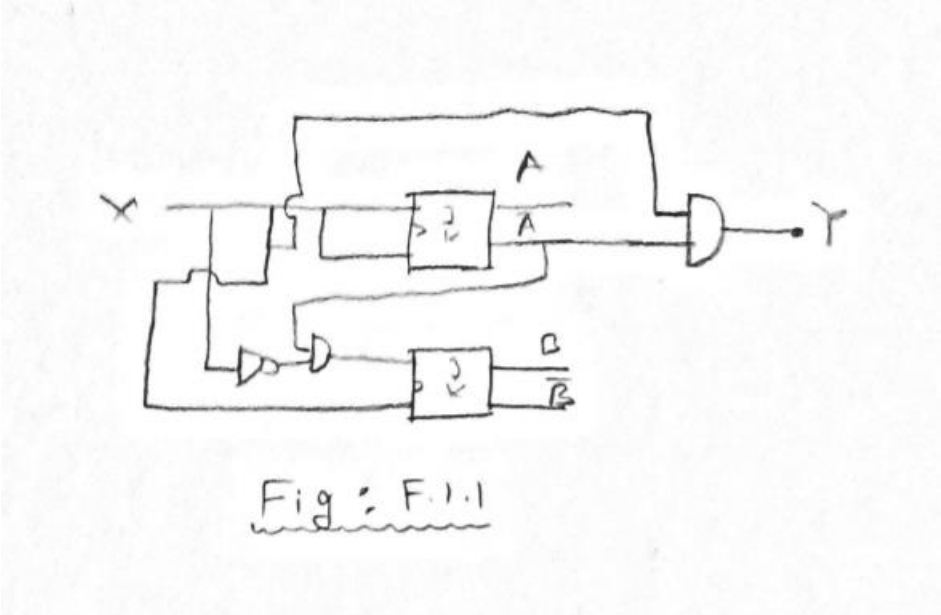
x	x	1	0
x	x	x	x

$K_B = X$

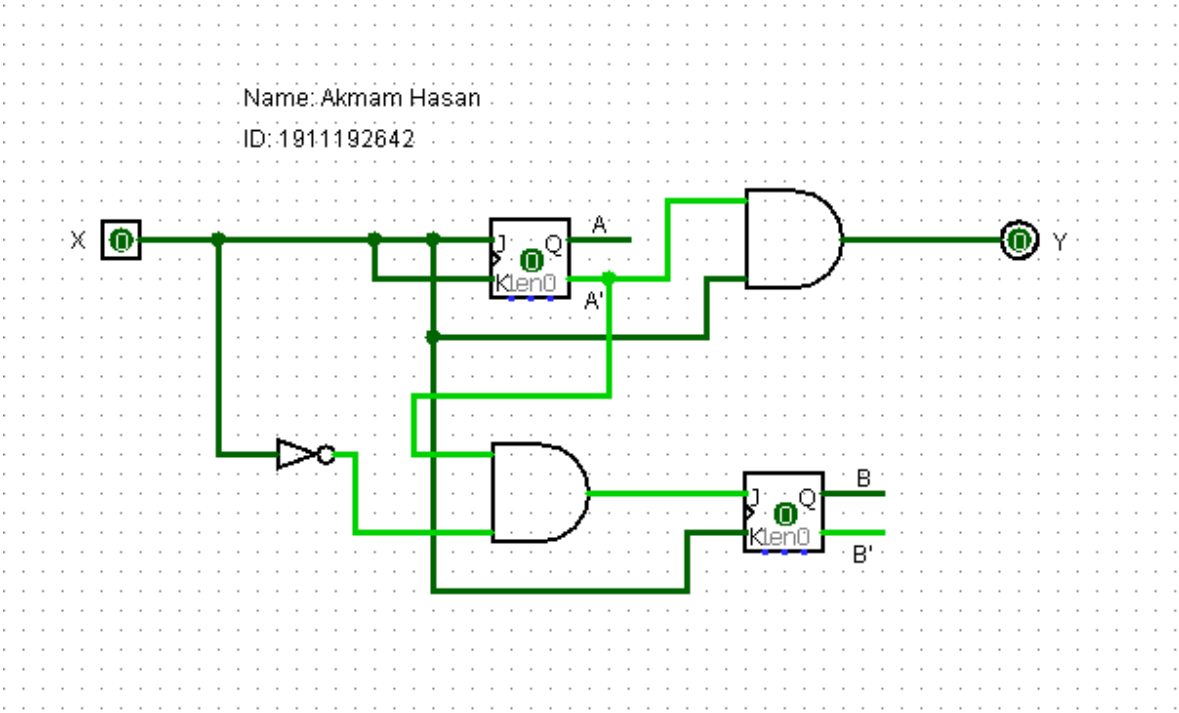
0	1	1	0
0	0	x	x

$Y = A'X$

Q	Q_{next}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Report1: Simulate the sequential circuit you built (Figure F.1.1) using Logisim.



Experiment 2: Constructing a Sequential Circuit using T Flip-Flops

C.2 Apparatus

• Trainer board
• 1 x IC 74107 JK Flip-Flop
• 1 x IC 7408 2-input AND gates
• 1 x IC 7432 2-input OR gates
• 1 x IC 7404 Hex Inverter (NOT gates)

Q	Q_{next}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table D.2.1: T flip-flop: Excitation Table

Present State		Input	Next State		Output	Flip-Flop Input Functions	
A	**B**	**X**	**A**	**B**	**Y**	**T_A**	**T_B**
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	1	1	0	1	1	1
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0
1	1	0	x	x	x	x	x
1	1	1	x	x	x	x	x

Table F.2.1: State Table for circuit using T Flip-Flops

0	1	1	0
0	1	x	x

$T_A = X$

1	0	1	0
0	0	x	x

$T_B = A'B'X' + BX$

0	1	1	0
0	0	x	x

$Y = A'X$

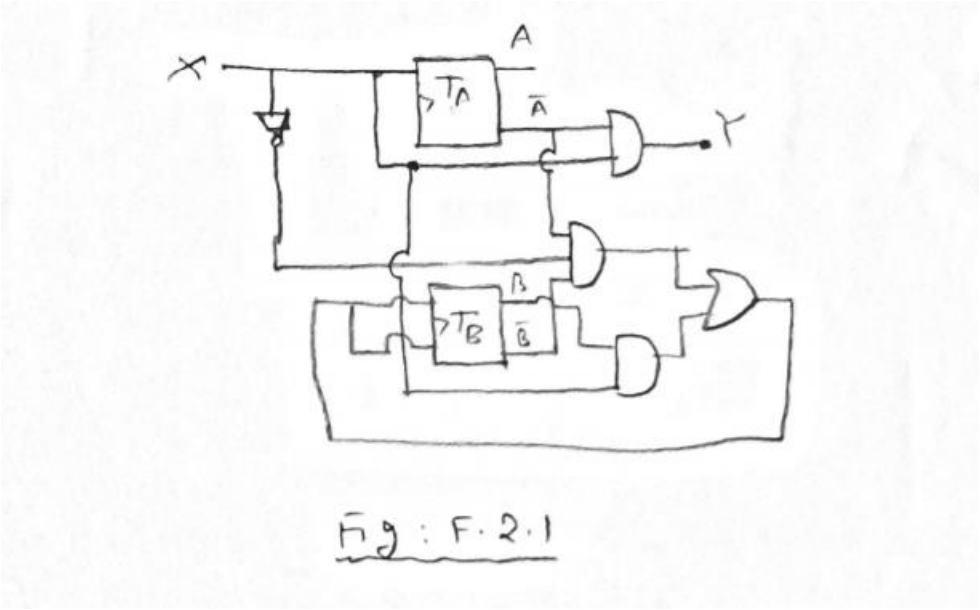


Fig : F·2·1

E.2 Report

1. Is the output equation (Y) of this circuit the same as the equation in the JK Flip-Flop circuit? Explain why.

The statement is TRUE. The output equation (Y) of this circuit is the same as the equation in the JK Flip-Flop circuit. The T flip-flop is a single input version of the JK flip-flop. If both inputs are tied together, T flip-flop is gotten from the JK type. The output Y comes from when A and B go to the next state and the output of the T flip-flop toggles with each clock pulse. Y come from Same source for the both T Flip-Flop and JK Flip-Flop.
That is why, the output equation (Y) of this circuit is the same as the equation in the JK Flip-Flop circuit.

Experiment 3: Constructing a Sequential Circuit using D Flip-Flops

C.3 Apparatus

- Trainer board
- 1 x IC 7474 Dual D Flip-Flops
- 1 x IC 7408 2-input AND gates
- 1 x IC 7432 2-input OR gates
- 1 x IC 7404 Hex Inverter (NOT gates)

Q	Q_{next}	D
0	0	0
0	1	1
1	0	0
1	1	1

Table D.3.1: D flip-flop: Excitation Table

Present State		Input	Next State		Output	Flip-Flop Input Functions	
A	**B**	**X**	**A**	**B**	**Y**	**D_A**	**D_B**
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1
0	1	1	1	0	1	1	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	1	0	x	x	x	x	x
1	1	1	x	x	x	x	x

Table F.3.1: State Table for circuit using D Flip-Flops

0	1	1	0
1	0	x	x

$D_A = AX' + A'X = A \text{ XOR } X$

1	0	0	1
0	0	x	x

$D_B = A'X'$

0	1	1	0
0	0	x	x

$Y = A'X$

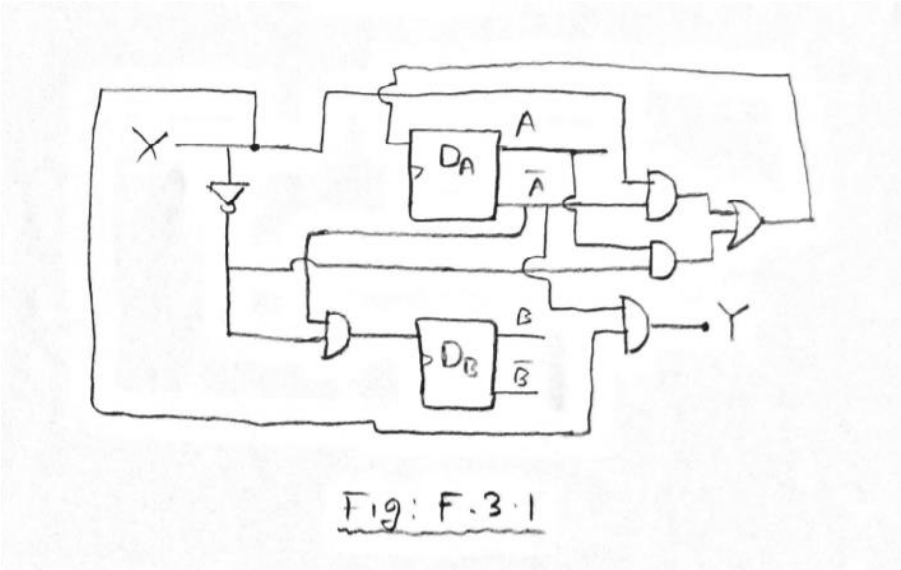
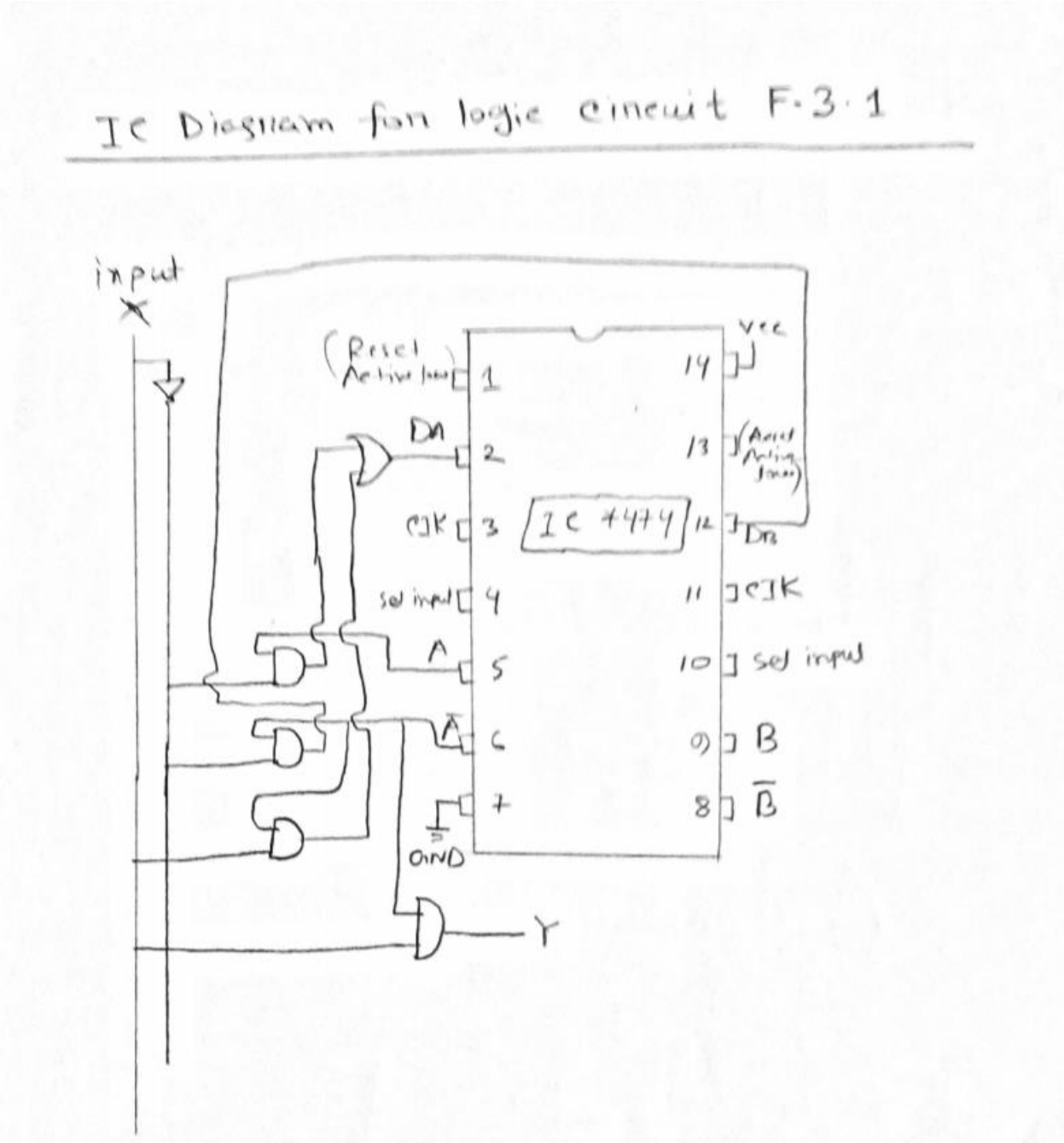


Fig: F.3.1

E.3 Report

1. Draw the IC diagram for the logic circuit in Figure F.3.1



Discussion

Because of human error and equipment error, we did not get the exact results. In today's lab we get a practical understanding of State Diagrams and State Tables. Then we understand the concept of designing Sequential Circuits using Flip-Flops. Finally, we design and implement a Synchronous Sequential Circuit.