Instruction:

Complete all questions in 1 hour.

1.Which one is the characteristic of Harvard Architecture?

A. Program and Data stored in Separate Memory

B. Program and Data stored in the same Memory

C. Program and data stored in Cache Memory

D. All of the Above

2.Which of the following is the working cycle of the CPU?

A. Decode, Execute, Fetch

B. Fetch, Decode, Execute

C. Fetch, Execute, Decode

D. All of the Above

3. Any condition that causes a processor to stall is called _____

A. Hazard

B. Page fault

C. System error

D. None of the mentioned

4.What does the control unit generate to control other units?

A. Transfer signals

B. Command Signal

C. Control signals

D. Timing signals

5. What must the processors of all computers have?

E. Control unit

F. ALU

G. Register

H. All of these

6.Which is the fastest memory in the computer?

A. Cache

B. RAM

C. Register

D. Hard disk

7. With the help of _____, we reduce the memory access time:

I. SDRAM
J. Cache
K. Heaps
L. Higher capacity RAMs

8. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?

M. ISA
N. ANSA
O. Super-scalar
P. All of the mentioned

9. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____

Q. Super-scaling
R. Pipe-lining
S. Parallel Computation
T. None of the mentioned

10. A 24 bit address generates an address space of _____ locations.

U. 1024
V. 4096
W. 2^{48}
X. **16,777,216**

11.The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

For each county,

Name	State	Population	Median
40*8 bits	320 bits	32 bits	32 bits
320 bits	16 bits		

Total for 1 county=320+16+32+32
=400 bits
For 3100 counties=400*3100
=1,240,000bits
In Byte=1,240,000/8
=155,000
In Kilobyte=155,000/1000
=155 Kb

12.The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.

a) Calculate the width of the data bus.
Here we know,
Total memory=2^address bus*width of data bus
16 GB=2^32*width
16*2^30=2^32*width[gb into byte,*2^30]
2^4*2^30*2^3=2^32*width[into bits,*2^3]
2^5=width
Width=32 bits or 4 bytes

b) State the effect that adding one new line to the address bus would have on the maximum addressable memory.

Solution,

Total memory = 2 address bus * width of data bus

X=2^32+1*2^5

X=2^33*2^5

X=2^38 bits

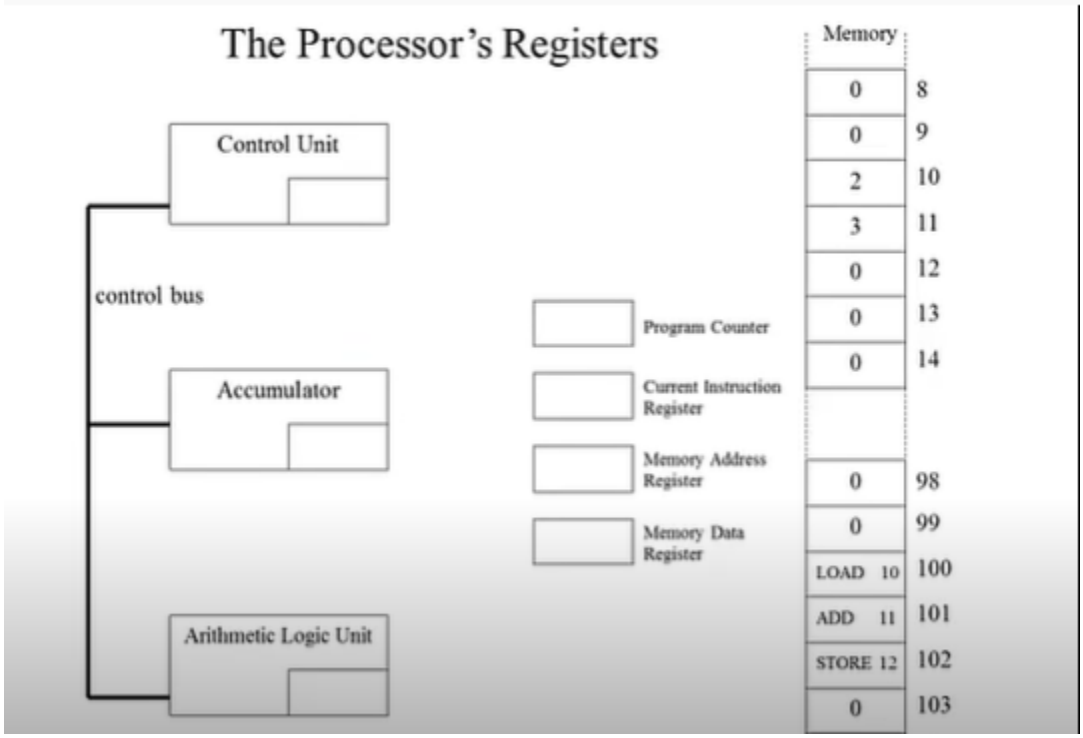
=32gb

13.Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add : [11]

Store: [12]



Here,

10 is stored in memory register. Then the address line of 10 i.e. 100 is stored in Program Counter and memory address register where as 10 is store in current Instruction register and memory data register. After this, Control unit

receives the value 2 from the memory register and store it in the Accumulator.
Then another instruction "Add" i.e.11 is stored in memory register. Then the address line of 11 i.e. 101 is stored in program counter and memory address register where as 11 is stored in current instruction register and memory data register. After this, Control unit receives the value 3 and it transferred to ALU. ALU performs the add operation between 2(from accumulator) and 3 and stores the new output i.e. 5 in accumulator again. Again same process continues, 12 is stored in memory register and the address line of 12 i.e. 102 is stored in program counter and memory address register where as 12 gets stored in the current instruction register and memory data register. Then the CU receives the value 0.

14.Write short notes on the following topic:

a) Von Neumann and Harvard Architecture

A stored program computer system called Von Neumann is an old computer architecture that uses the same physical memory address for data and instructions. For the transport of instructions and data, there is a common bus. As a result, it is less expensive than Harvard Architecture. It is primarily used in

personal and small computers since its CPU cannot access instructions and read or write at the same time.

Modern computer architecture called Harvard Architecture is based on the Harvard Mark I relay-based paradigm and has separate physical memory for storing instructions and data. Due to the utilization of separate buses for data and instruction transfer, it may complete all of its instructions in a single cycle. In comparison to Neumann Architecture, it is more expensive because current technology is integrated. Because of its CPU's ability to access instructions while simultaneously reading and writing, it is mostly employed in micro controllers and signal processing.

b) RISC vs CISC architecture

Reduced Instruction Set Computer Processor is what RISC stands for. The emphasis is on software to optimize the instruction set because it needs many sets to store the instructions. Because the RISC Processor's programming unit is hard wired, it has straightforward decoding and pipeline usage. The execution time of RISC is extremely fast since it has more transistors on memory registers.

A complex instruction set computer is referred to as a CISC. It is a microprogramming device that prioritizes hardware in order to optimize the instruction set. Due to the fact that it employs a single register set to hold instructions, it has complex decoding instructions. Additionally, using the pipeline is more difficult than using CISC. The lengthy execution time is caused by the program's use of load and store instructions in memory-to-memory communication.