Question 29:

Cache Specifications	
Cache Size	1KB
Cache Line Size	16B
Associativity	4
Write Policy	Write Buffer
Replacement policy	LRU counter
Cache Type	Way Halting

Instruction Type	Instruction	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R type		**funct7**							**Im[4:0]**					**rs1**					**funct3**			**rd**				**opcode**						
	srli	0	0	0	0	0	0	0	shamt[4:0]					rs1					1	0	1	rd				0	0	1	0	0	1	1
	Reg[rd] = Reg[rs1] >> shamt																																
		funct7							**rs2**					**rs1**					**funct3**			**rd**				**opcode**						
	sra	0	1	0	0	0	0	0	rs2					rs1					1	0	1	rd				0	1	1	0	0	1	1
	Reg[rd] = Reg[rs1] >>> Reg[rs2][4:0]																																
I type		**Imm[11:0]**												**rs1**					**funct3**			**rd**				**opcode**						
	lw	Imm[11:0]												rs1					0	1	0	rd				0	0	0	0	0	1	1
	Reg[rd] = Mem[[Reg[rs1] + sExt(Imm[11:0])] (32 bits)																																
	addi	Imm[11:0]												rs1					0	0	0	rd				0	0	1	0	0	1	1
	Reg[rd] = Reg[rs1] + sExt(Imm[11:0])																																
	andi	Imm[11:0]												rs1					1	1	0	rd				0	0	1	0	0	1	1
	Reg[rd] = Reg[rs1] & sExt(Imm[11:0])																																
U type		**Imm**																				**rd**				**opcode**						
	AUIPC	imm[31:12]																				rd				0	0	1	0	1	1	1
	Reg[rd] = PC + {imm[31:12],12'd0}																																

Instruction Type	Instruction	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR type		funct4				rd/rs1					rs2					op	
	C.MV	1	0	0	0	rd (≠ 0)					rs2 (≠ 0)					1	0
	Reg[rd] = Reg[rs2]																
CB type		funct3			Imm[8|4:3]			rs1			Imm[7:6|2:1|5]					op	
	C.BNEZ	1	1	1	Imm[8|4:3]			rs1			Imm[7:6|2:1|5]					0	1
	if(Reg[rs1] != 0) PC = PC + sExt(Imm)																
CS type		funct3			Imm[5:3]			rs1			Imm[2|6]		rs2			op	
	C.SW	1	1	0	Imm[5:3]			rs1			Imm[2|6]		rs2			0	0
	Mem[Reg[rs1] + {15'b0,Imm[6:2],2'b0}] = Reg[rs2]																