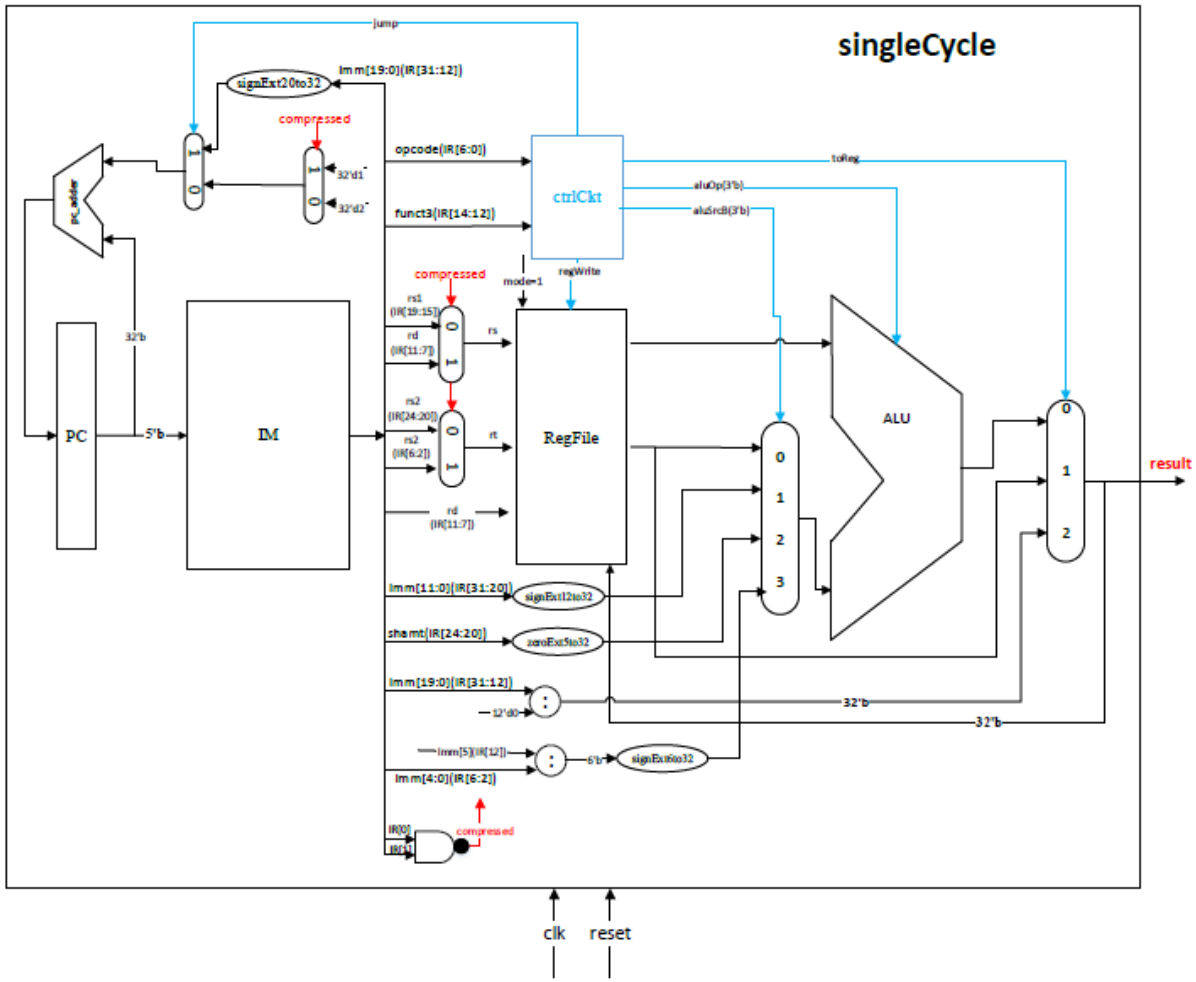
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2017-2018
CS F342 Computer Architecture
Lab – 3, 7th September 2017

Implement the following design using verilog HDL in Xilinx 14.7. **Download singleCycleInterfaces.v file**. Add **singleCycleInterfaces.v** as a source to your project and modify it.



Instruction Format:

Istruction Type	Instruction	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		**Funct7**							**rs2**					**rs1**					**funct3**			**rd**						**opcode**						
	sub	0100000							rs2					rs1					000			rd						0110011						
	or	0000000							rs2					rs1					110			rd						0110011						
I		**Imm[11:0]**												**rs1**					**funct3**			**rd**						**opcode**						
	andi	Imm[11:0]												rs1					111			rd						0010011						
	srai	0100000							shamt					rs1					101			rd						0010011						
U		**Imm[19:0]**																				**rd**						**opcode**						
	lui	Imm[19:0]																				rd						0110111						
J		**Imm[19:0]**																				**rd**						**opcode**						
	j	Imm[19:0]																				00000						1101111						
CI																			**funct3**		**Imm [5]**	**rd/rs1**					**Imm[4:0]**					**opcode**	
	c.addi																		000		Imm [5]	rd/rs1					Imm[4:0]					01	
CR																			**funct3**		**Imm [5]**	**rd/rs1**					**rs2**					**opcode**	
	c.mv																		100		0	rd					rs2					10	

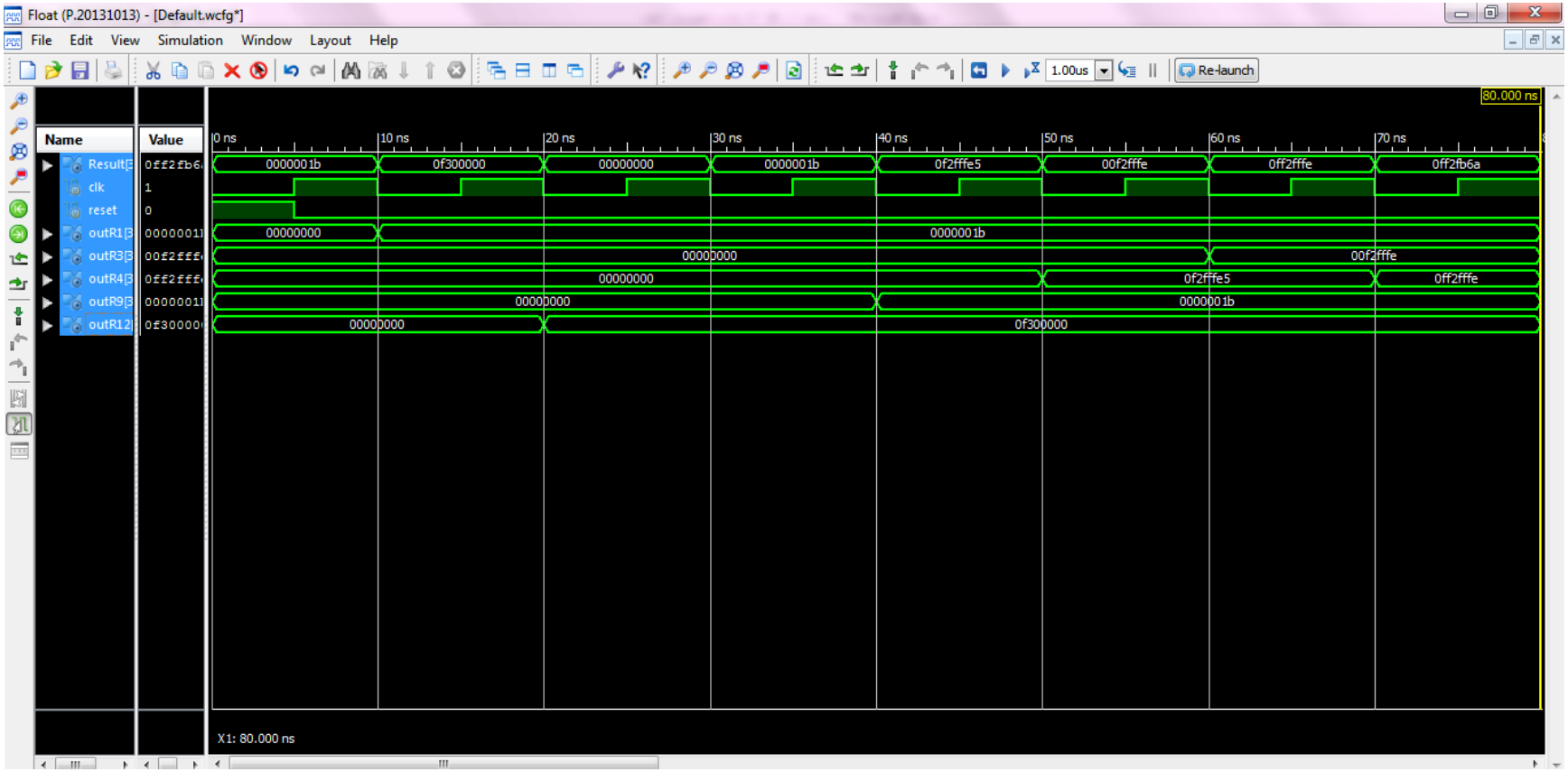
Control Circuit :

Instruction	Opcode (IR[6:0])	Funct3 (IR[14:12])	aluSrcB(2b)	aluOp(3b)	toReg(2b)	regWrite	jump
sub	0110011	000	00	001	00	1	0
or	0110011	110	00	010	00	1	0
andi	0010011	111	01	011	00	1	0
srai	0010011	101	10	100	00	1	0
lui	0110111	XXX	00	000	10	1	0
j	1101111	XXX	00	000	00	0	1
c.addi	XXXXX01	XXX	11	000	00	1	0
c.mv	XXXXX10	XXX	00	000	01	1	0

ALU operations :

Aluop(3b)	Operation
000	Add
001	Subtract
010	Or
011	And
100	Shift right arithmetic

WaveForm:


Float (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
Result[
clk
reset
outR1[
outR3[
outR4[
outR9[
outR12
0ff2fb6
1
0
00000011
00f2fff
0ff2fff
00000011
0f30000
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80.000 ns
0000001b
0f300000
00000000
0000001b
0f2fffe5
00f2fffe
0ff2fffe
0ff2fb6a
X1: 80.000 ns