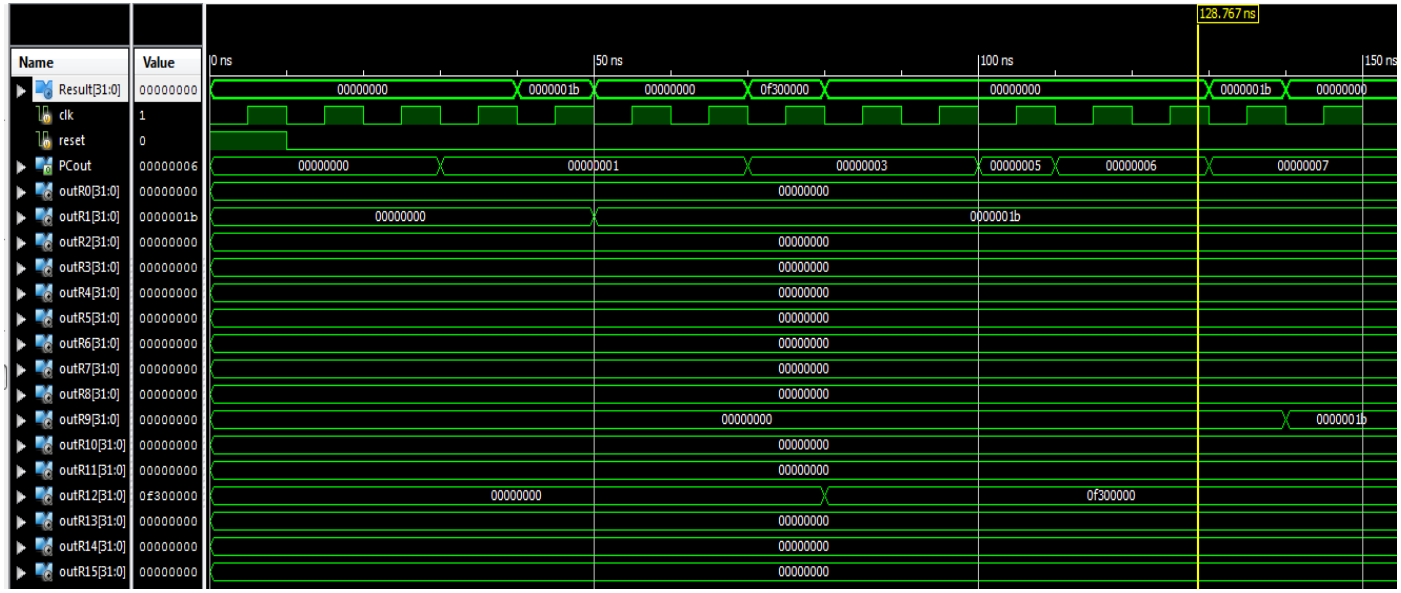
BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI K. K. BIRLA Goa Campus
First Semester 2017-2018
CS F342 Computer Architecture
Lab – 5, 5th October 2017

Implement the following design using verilog HDL in Xilinx 14.7. **Download multiCycleInterfaces.v file**. Add **multiCycleInterfaces.v** as a source to your project and modify it.

WaveForm :




184.705 ns
Name
Value
150 ns
200 ns
250 ns
Result[31:0]
00000000
0f2fffe5
00000000
00797fff
00000000
0f30001b
00000000
0000000a
clk
1
reset
0
PCout
00000006
00000007
00000009
0000000b
0000000d
0000000f
outR0[31:0]
00000000
outR1[31:0]
0000001b
outR2[31:0]
00000000
outR3[31:0]
00000000
00000000
00797fff
outR4[31:0]
00000000
00000000
0f2fffe5
outR5[31:0]
00000000
00000000
0f30001b
outR6[31:0]
00000000
outR7[31:0]
00000000
outR8[31:0]
00000000
outR9[31:0]
0000001b
outR10[31:0]
00000000
outR11[31:0]
00000000
outR12[31:0]
0f300000
outR13[31:0]
00000000
outR14[31:0]
00000000
outR15[31:0]
00000000

Instruction Format:

Istruction Type	Instruction	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R		**Funct7**							**rs2**					**rs1**					**funct3**			**rd**						**opcode**					
	sub	0100000							rs2					rs1					000			rd						0110011					
		Reg[rd] = Reg[rs1] – Reg[rs2]																															
	or	0000000							rs2					rs1					110			rd						0110011					
		Reg[rd] = Reg[rs1] | Reg[rs2]																															
I		**Imm[11:0]**												**rs1**					**funct3**			**rd**						**opcode**					
	andi	Imm[11:0]												rs1					111			rd						0010011					
		Reg[rd] = reg[rs1] & sExt(Imm[11:0])																															
	srai	0100000							shamt					rs1					101			rd						0010011					
		Reg[rd] = reg[rs1] >>> shamt																															
U		**Imm[19:0]**																				**rd**						**opcode**					
	lui	Imm[19:0]																				rd						0110111					
		Reg[rd] = Imm[19:0] : 12’d0																															
J		**Imm[19:0]**																				**rd**						**opcode**					
	j	Imm[19:0]																				00000						1101111					
		PC = sExt(Imm[19:0])																															
CI																			**funct3**		**Imm [5]**	**rd/rs1**					**Imm[4:0]**				**opcode**	
	c.addi																		000		Imm [5]	rd/rs1					Imm[4:0]				01	
		Reg[rd/rs1] = Reg[rd/rs1] + sExt(Imm[5:0])																															
CR																			**funct3**		**Imm [5]**	**rd/rs1**					**rs2**				**opcode**	
	c.mv																		100		0	rd					rs2				10	
		Reg[rd] = Reg[rs2]																															