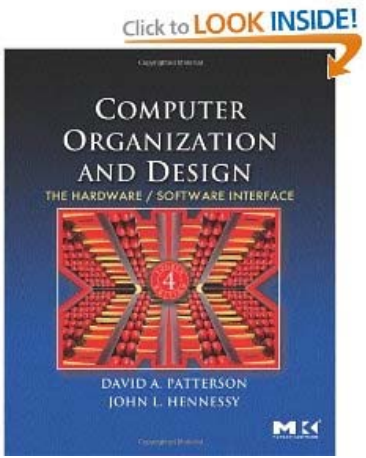
Computer Organization
Course Outline

Course Administration

- Instructor: Ing-Chao Lin (林英超)
  - email: iclin@mail.ncku.edu.tw
  - Tel: +8866-2757575 ext. 62553
- Teaching Assistant: To be announced
  - Lab: 雲平大樓東棟六樓
  - Phone: 06-2757575 ext. 62530-33
  - Email: nckuideallab@gmail.com
- Office hour: To be announced
- Course Website:
  - https://sites.google.com/site/nckuideal/courses/comporg/comporg2014 announces and slides will be posted here
  - http://moodle.ncku.edu.tw – submit your homework there

Textbook

- Textbook
  - Computer Organization and Design: The Hardware/Software Interface, 4th ed., 2009, by David Patterson and John Hennessy

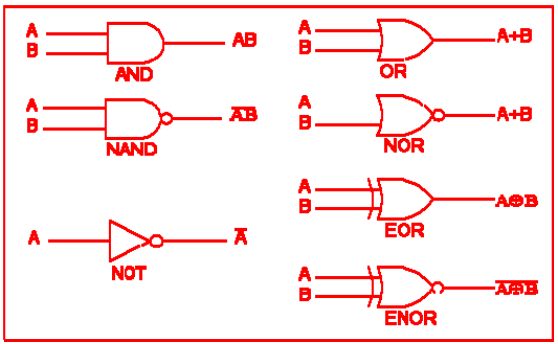


Topics Covered

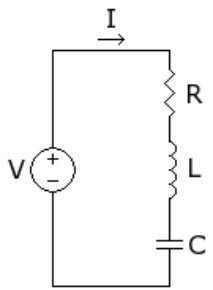
- Computer Abstraction and
  - Performance
  - Power Wall
- Instructions:
- Arithmetic for Computers
  - Addition/Subtraction
  - Multiplication/ Floating point
- The Processor
  - Data path /pipeline
- Memory Hierarchy
  - Cache basics/ Virtual memory
- Storage
- Multiprocessor

Prerequisite

- English
- Introduction to Circuits Theory and Digital Electronics (F720401)
  - Basic Circuit Theory
  - Frequency response and Bode plot
  - Semiconductor and Transistors
  - Transistor Circuitry and Amplifier
  - Logic Circuits



- Introduction to Digital System (F720900)
  - Logic Gates and Gate-Level Minimization
  - Combinational Logic and Synchronous Sequential Logic
- Programming Language: C and Verilog



Tentative Grading (the ratio may vary by 5%)

- Homework and Programming Assignment (25 %)
  - Additional homework hour on Thursday 12:30 ~ 1:00 (not every week, TA will announce in advance)
  - No late submission without justified reasons
- 3~4 Quiz (30%) (No midterm exam)
- Final exam (30%)
- Class Participation (Attendance and In-class quick test, 15%)
  - You need to sign in each class
  - Honesty is the best policy. If someone else sign for you, you will lose 5 points of your final grade for each time.

國立成功大學學則

- 第九條 學生因請假而缺課者，稱為缺席，無故缺席者稱為曠課。學生請假辦法另定之。
- 第十條 學生曠課一小時，扣所缺科目學業成績分數一分，請假缺席三小時，扣所缺科目學業成績分數一分。因公請假，或因病請假而經醫生診斷出具證明書，或因懷孕、生產、哺育三歲以下幼兒而核准之事（病）假、產假，其缺席不扣分。
- More rules
  - 國立成功大學試場規則
  - 國立成功大學學生缺席、曠課扣分、扣考辦法
  - 國立成功大學教室使用守則

  http://cid.acad.ncku.edu.tw/files/11-1056-603.php

Laptop & Tablet issue

- It's ok if you use laptop or tablet for class-related issues, such as reading course slides.
- However, It's not allowed to use laptop or tablet for things that are not related to class.
- I want everyone to be here and present

You will lose 1 point of your final grade for each violation.

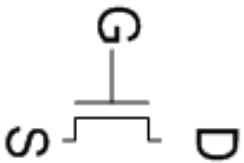
Homework 1 (1% of your final grade)

- Put your head shot picture (大頭照) on Moodle website. A picture that I can recognize you.
- Due date : 2/24 (Monday) 11:50PM

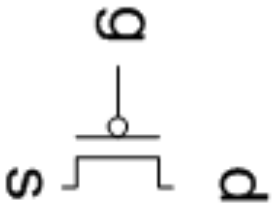
In-class quick test

- In-class quick test is a very simple test.
- Normally take less than 10 minutes.
- Cover what I taught in last class
- Basically, it is random, will not be announced in advance

Recap of basic MOS transistors and logic gates



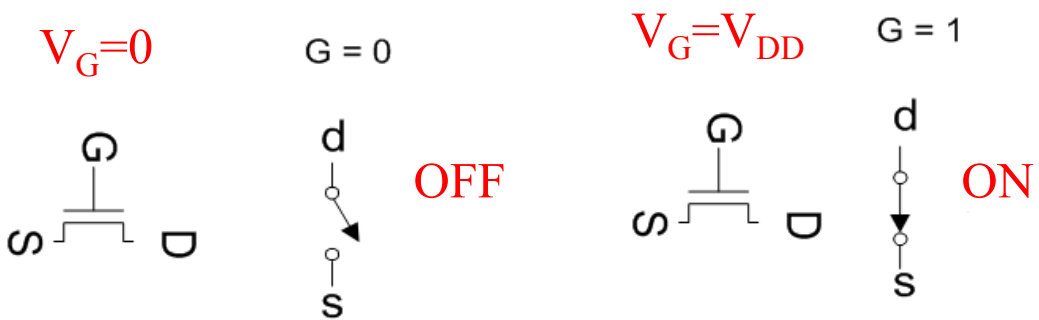
NMOS



PMOS

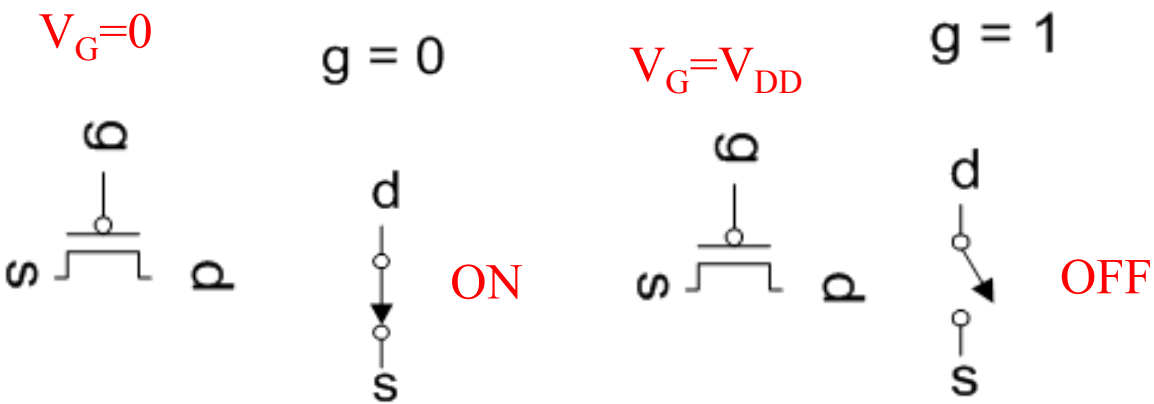
nMOS transistor

- When the gate is at a low voltage (V_G=0):
  - No channel, transistor is off
- When the gate is at a high voltage (V_G=V_{DD}):
  - Positive voltage inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



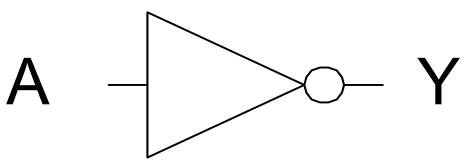
pMOS Transistor

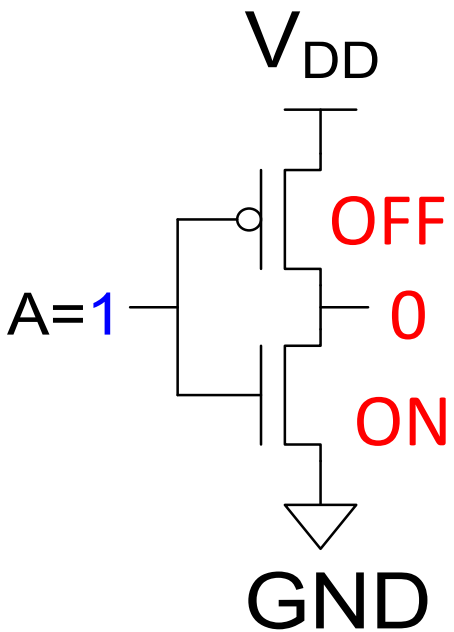
- Similar, but doping and voltages reversed
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



CMOS Inverter

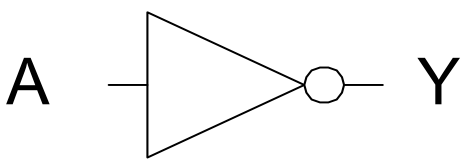
A	Y
0	
1	**0**

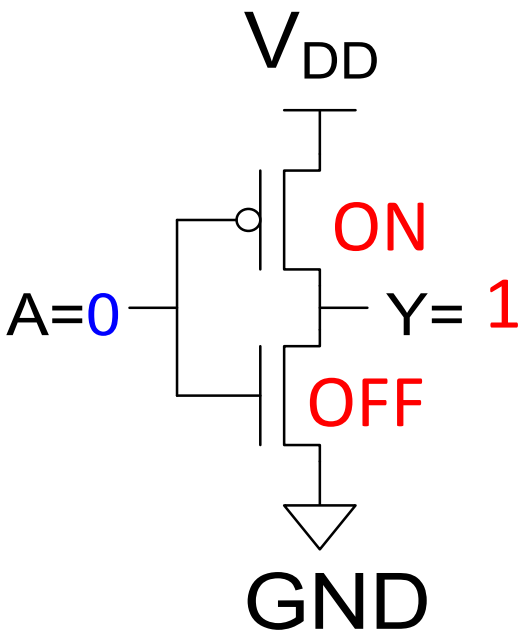




CMOS Inverter

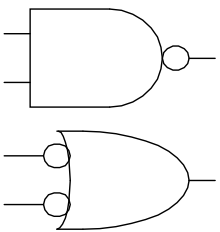
A	Y
0	**1**
1	0

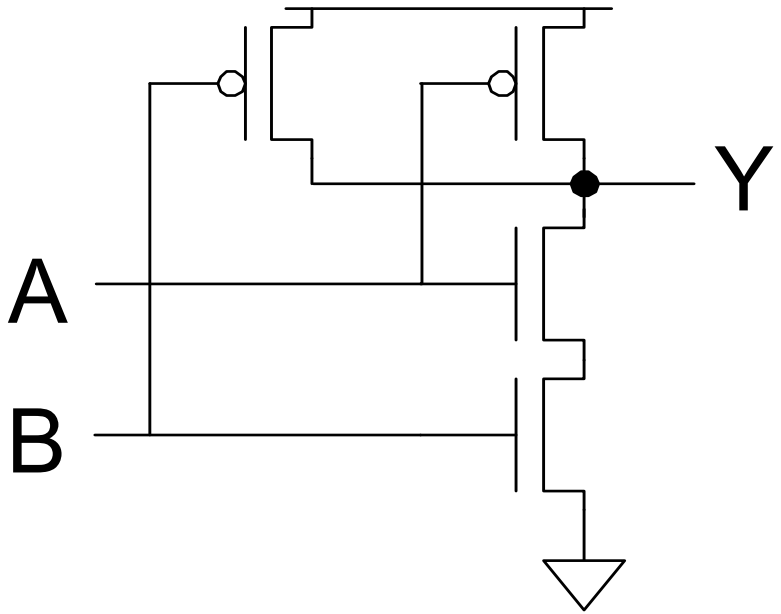




CMOS NAND Gate

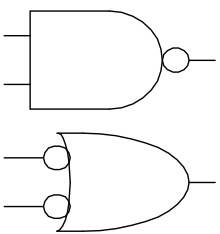
A	B	Y
0	0	
0	1	
1	0	
1	1	

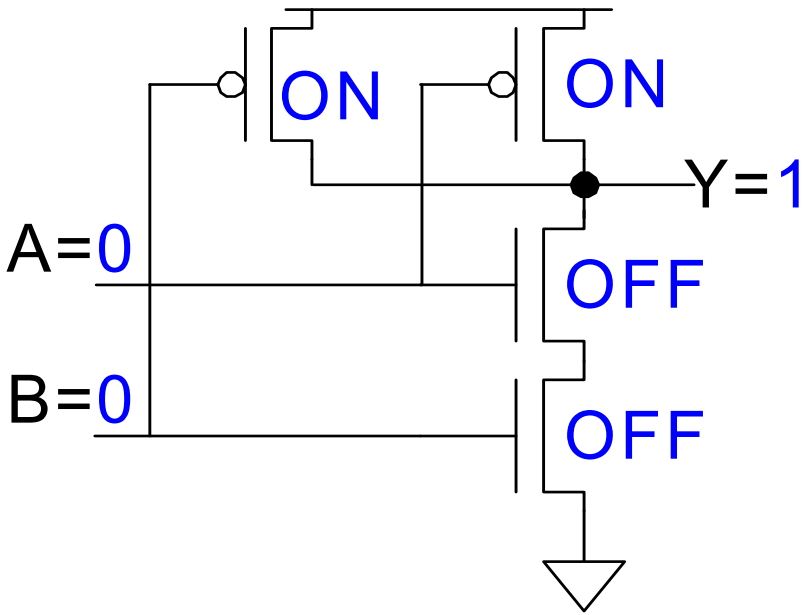




CMOS NAND Gate

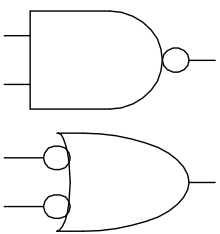
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

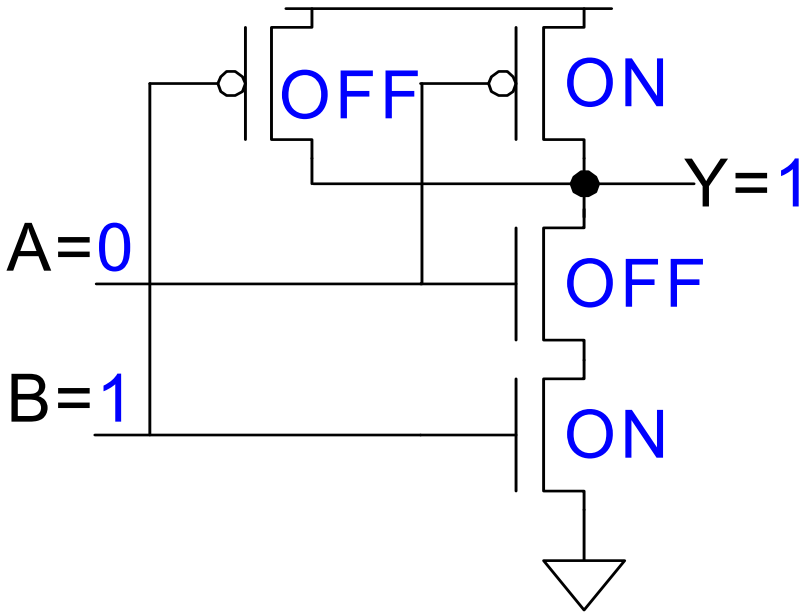




CMOS NAND Gate

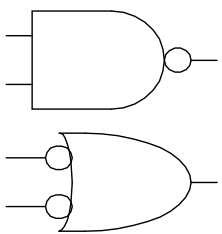
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

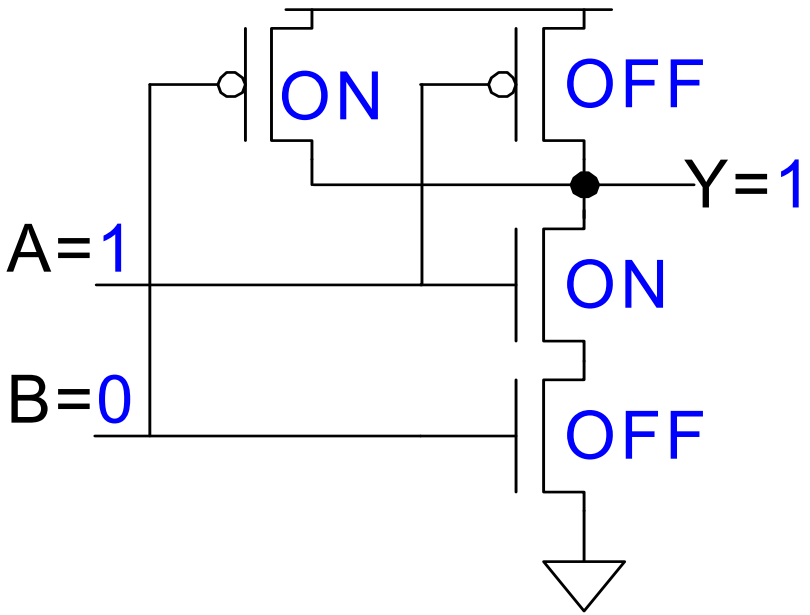




CMOS NAND Gate

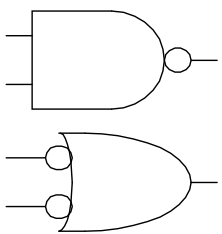
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

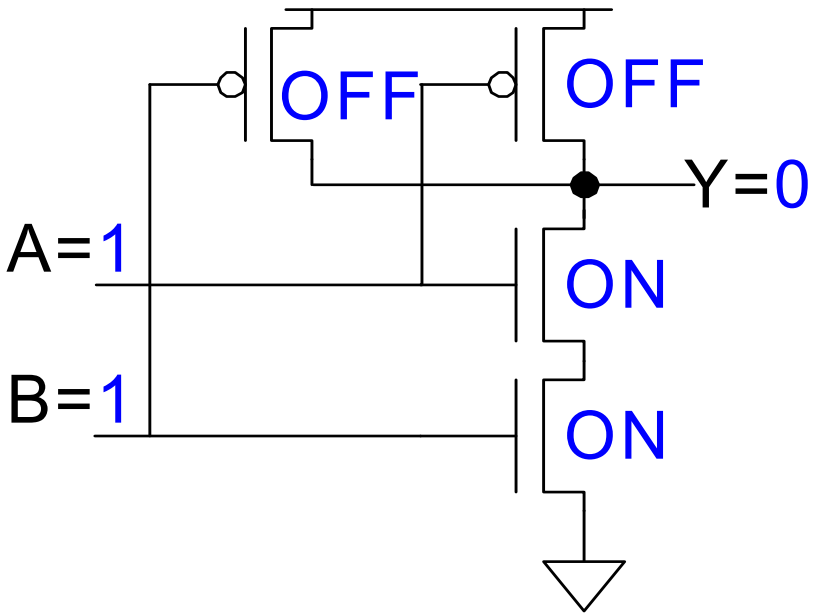




CMOS NAND Gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

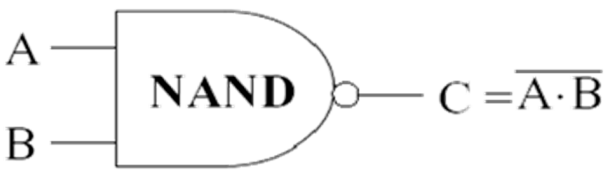


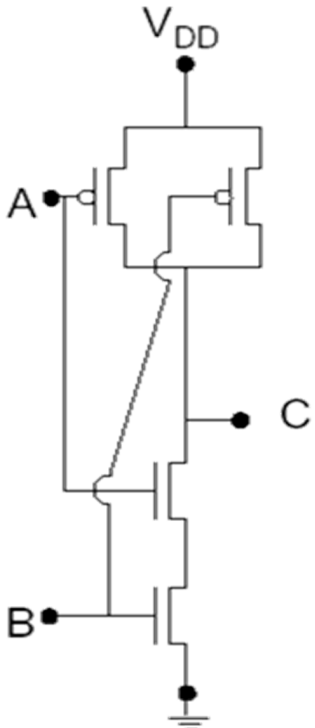


Use Switch to build Gates

- CMOS NAND:

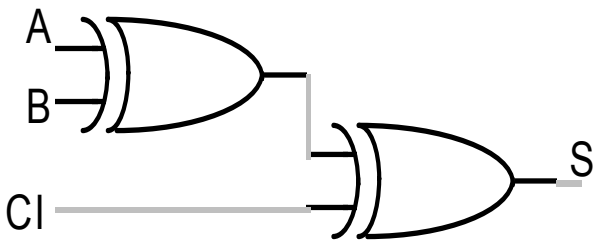
A	B	A B	C= $\overline{A\ B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

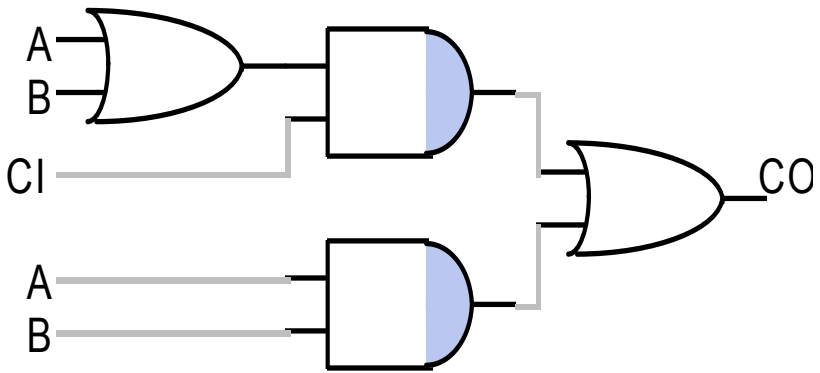




Use gates to build logic blocks

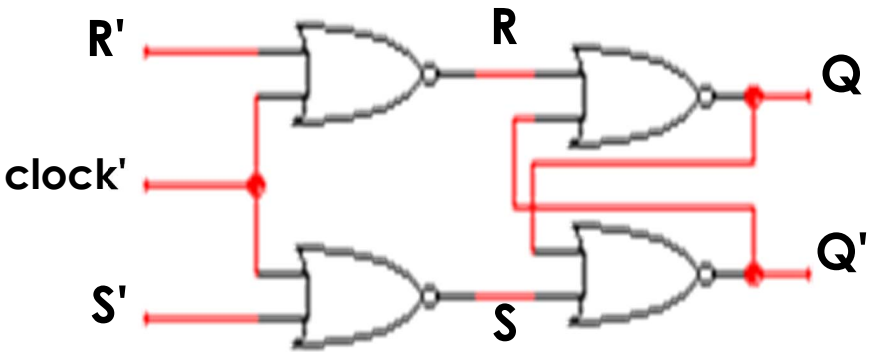
- Adder





Use gates to build memory element

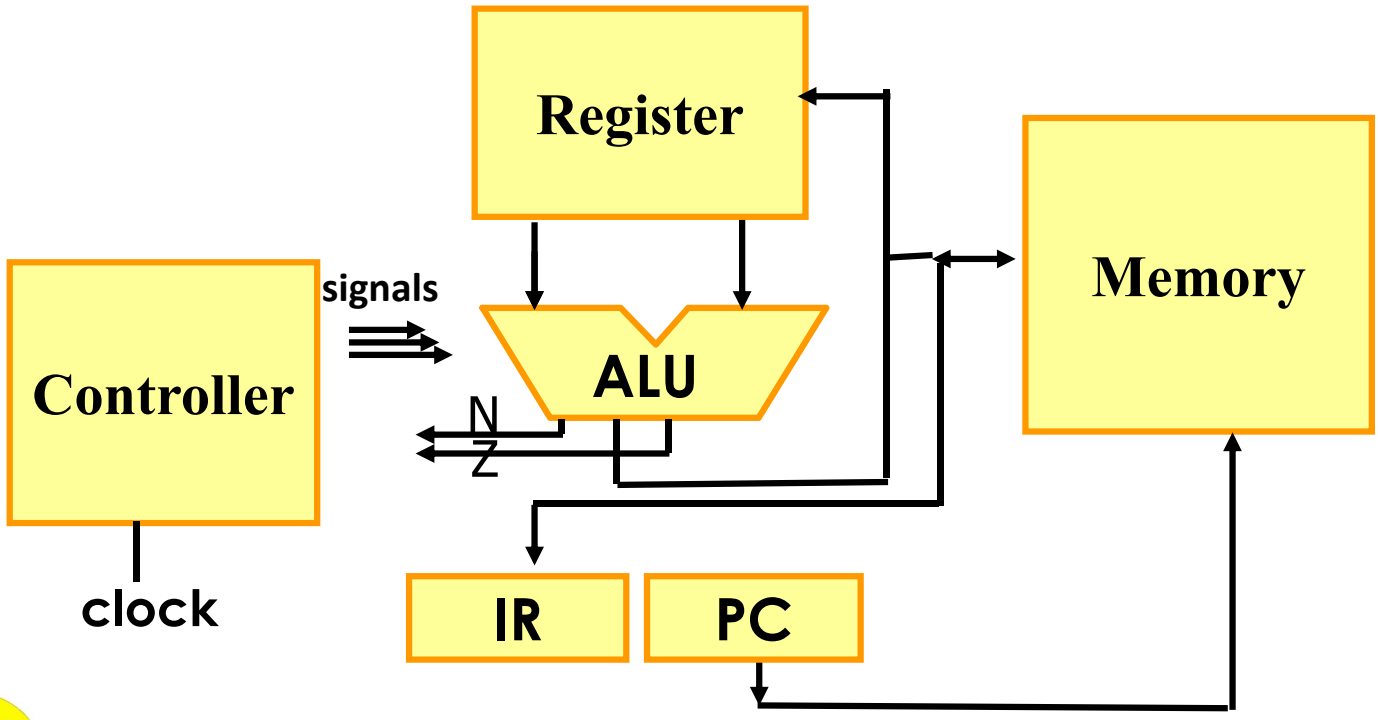
- Circuit to store 1-bit data
  - SR Latch



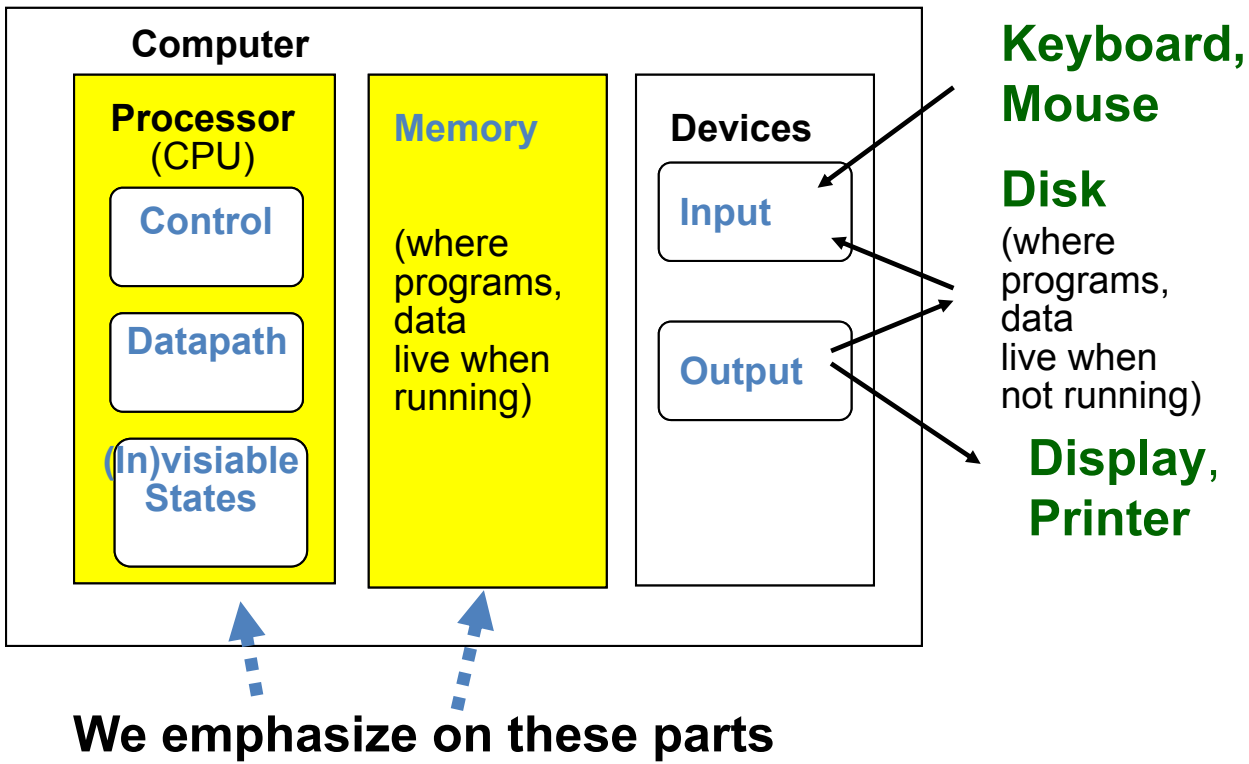
If you are interested in these topics, you can take

- Digital System Design
- Digital IC Design
- FPGA Design
- Hardware Description Language

Use logic blocks to build a CPU

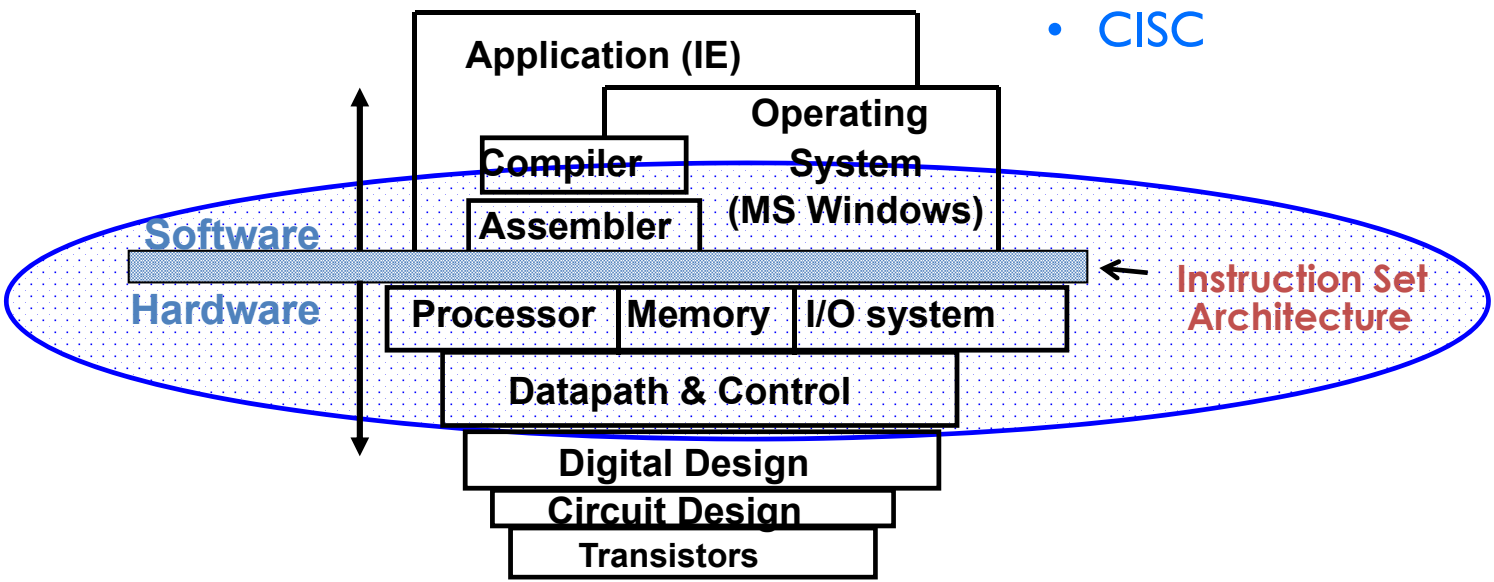


Basic Organization of a Computer

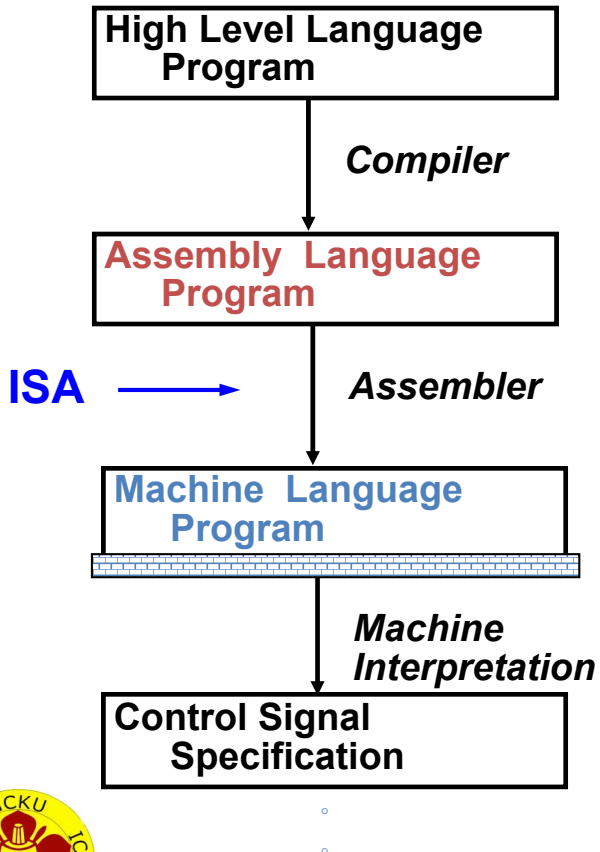


Computer Organization: Hardware/Software Interface

- RISC - MIPS/ARM
- CISC



A little Detail




```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

```
lw      $15,  0($2)
lw      $16,  4($2)
sw $16, 0($2)
sw $15, 4($2)
```

```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

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Why We Learn Computer Organization?

- Required
- It impacts every other aspect of electrical engineering and computer science
- One of the foundations in computer science

Thank you for your listening!

Any Questions?

Backup Slides