Chapter 1 Exercise Problem

Review question.

- Explain the following term
- Explain/discuss the following term: Amdahl's law.
- Explain/discuss the following term: Power Wall
- Explain/discuss the following term: benchmark
- Explain/discuss the following term: throughput, response time, CPU time
- Explain/discuss why MIPS is not a good metric to evaluate performance
- Explain/discuss the following term: compiler
- Explain/discuss the following term: machine language

No solutions are provided.

1.2

1.2.1. For a color display using 8 bits for each of the primary colors(red, green, blue) per pixel and with a resolution of 1280 * 800 pixels, what should be the size (in bytes), of the frame buffer to store a frame?

1.2.2 If a computer has a main memory of 2GB, how many frames could it store, assuming the memory contain no other information?

1.2.3 If a computer connected to a 1 gigabit Ethernet network needs to send a 256 Kbytes file, how long it would take?

1.2.1. 8 bits × 3 colors = 24 bits/pixel = 4 bytes/pixel. 1280 × 800 pixels = 1,024,000 pixels. 1,024,000 pixels × 4 bytes/pixel = 4,096,000 bytes (approx. 4 Mbytes).

1.2.2. 2 GB = 2000 Mbytes. No. frames = 2000 Mbytes/4 Mbytes = 500 frames.

1.2.3. Network speed: 1 gigabit network ==> 1 gigabit/per second = 125 Mbytes/second. File size: 256 Kbytes = 0.256 Mbytes. Time for 0.256 Mbytes = 0.256/125 = 2.048 ms.

1.3<1.4>Consider three different processors P1, P2 and P3 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	**Clock rate**	**CPI**
P1	2 GHz	1.5
P2	1.5 GHz	1.0
P3	3 GHz	2.5

1.3.1 Which processor has the highest performance expressed in instructions per second?

1.3.2 If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

1.3.3 We are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

1.3.1 performance of P1 (instructions/sec) = $2 \times 10^9/1.5 = 1.33 \times 10^9$

performance of P2 (instructions/sec) = $1.5 \times 10^9/1.0 = 1.5 \times 10^9$

performance of P3 (instructions/sec) = $3 \times 10^9/2.5 = 1.2 \times 10^9$

Therefore, P2 has the highest performance

1.3.2 No. cycles = time × clock rate

cycles(P1) = $10 \times 2 \times 10^9 = 20 \times 10^9$ s

cycles(P2) = $10 \times 1.5 \times 10^9 = 15 \times 10^9$ s

cycles(P3) = $10 \times 3 \times 10^9 = 30 \times 10^9$ s

time = (No. instr. × CPI)/clock rate, then No. instructions = No. cycles/CPI

instructions(P1) = $20 \times 10^9/1.5 = 13.33 \times 10^9$

instructions(P2) = $15 \times 10^9/1 = 15 \times 10^9$

instructions(P3) = $30 \times 10^9/2.5 = 12 \times 10^9$

1.3.3 $time_{new} = time_{old} \times 0.7 = 7$ s

CPI = CPI × 1.2, then CPI(P1) = 1.8, CPI(P2) = 1.2, CPI(P3) = 3

f = No. instr. × CPI/time, then

f(P1) = $13.33 \times 10^9 \times 1.8/7 = 3.42$ GHz

f(P2) = 15 × 109 × 1.2/7 = 2.57 GHz

f(P3) = 12 × 109 × 3/7 = 5.14 GHz

1.4 Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table

	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

1.4.1 Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

1.4.2 What is the global CPI for each implementation?

1.4.3 Find the clock cycles required in both case.

1.4.1 P2

Class A: 10^5instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. × CPI/clock rate

P1: Time class A = 0.66×10^{-4}, Time class B = 2.66×10^{-4}

Time class C = 10×10^{-4}, Time class D = 5.33×10^{-4}

Total time P1 = 18.65×10^{-4}

P2: Time class A = 10^{-4}, Time class B = 2×10^{-4}

Time class C = 5×10^{-4}, Time class D = 3×10^{-4}

Total time P2 = 11×10^{-4}

1.4.2 CPI = time × clock rate/No. instr.

CPI(P1) = $18.65 \times 10^{-4} \times 1.5 \times 10^9/10^6 = 2.79$

CPI(P2) = $11 \times 10^{-4} \times 2 \times 10^9/10^6 = 2.2$

1.4.3

clock cycles(P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 4 = 28 \times 10^5$

clock cycles(P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 3 = 22 \times 10^5$

1.8 Suppose we have developed new versions of a processor with the following characteristics.

Version	Voltage	Clock rate
Version 1	5V	0.5 Ghz
Version 2	3.3V	1 Ghz

1.8.1 [5] <1.5> How much has the capacitive load varied between versions if the dynamic power has been reduced by 10%?

1.8.2 [5] <1.5> How much has the dynamic power been reduced if the capacitive load does not change?

1.8.3 [10] <1.5>Assuming that the capacitive load of version 2 is 80% the capacitive load of version 1, find the voltage for version 2 if the dynamic power of version 2 is reduced by 40% from version 1.

1.8.1 $Power_1 = V^2 \times$ clock rate $\times C$. $Power_2 = 0.9\ Power_1$

$C_2/C_1 = 0.9 \times 5^2 \times 0.5 \times 10^9/3.3^2 \times 1 \times 10^9 = 1.03$

1.8.2 $Power_2/Power_1 = V_2^2 \times$ clock $rate_2/V_1^2 \times$ clock $rate_1$

$Power_2/Power_1 = 0.87$ => Reduction of 13%

1.8.3

$Power_2 = V_2^2 \times 1 \times 10^9 \times 0.8 \times C_1 = 0.6 \times Power_1$

$Power_1 = 5^2 \times 0.5 \times 10^9 \times C_1$

$V_2^2 \times 1 \times 10^9 \times 0.8 \times C_1 = 0.6 \times 5^2 \times 0.5 \times 10^9 \times C_1$

$V_2 = ((0.6 \times 5^2 \times 0.5 \times 10^9)/(1 \times 10^9 \times 0.8))^{1/2} = 3.06$ V

1.11.

The following table shows manufacturing data for a processor.

Wafer diameter	Dies per wafer	Defects per unit area	Cost per wafer
15 cm	90	0.018 defects/cm^2	10

1.11.1 [10] <1.7> Find the yield.

1.11.2 [5] <1.7> Find the cost per die.

1.11.3 [10] <1.7> If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.

1.11.1 Wafer area = $\pi \times (d/2)^2$

a. Wafer area = $\pi \times 7.5^2 = 176.7\ cm^2$

Die area = wafer area/dies per wafer

Die area = $176.7/90 = 1.96\ cm^2$

Yield = $1/(1 + (\text{defect per area} \times \text{die area})/2)^2 = 0.97$

1.11.2 Cost per die = cost per wafer/(dies per wafer $\times$ yield)=0.12

1.11.3 Dies per wafer = $1.1 \times 90 = 99$

Defects per area = $1.15 \times 0.018 = 0.021$ defects/cm^2

Die area = wafer area/Dies per wafer = $176.7/99 = 1.78\ cm^2$

Yield = 0.97

1.14. Section 1.8 cites as a pitfall the utilization of a subset of the performance equation as a performance

metric. To illustrate this, consider the following data for the execution of a program in different processors.

Processor	Clock Rate	CPI
P1	4 GHz	1.25
P2	3 GHz	0.75

1.14.1 [5] <1.8> One usual fallacy is to consider the computer with the largest clock rate as having the largest performance. Check if this is true for Pl and P2.

1.14.2 [10] <1.8> another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor Pl is executing a sequence of 10^6 instructions and that the CPI of processor Pl and P2 do not change, determine the number of instructions that P2 can execute in the same time that Pl needs to execute 10^6 instructions.

1.14.3 [10] <1.8>A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors, and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P 1 and P2.

1.14.1 No. instr. = 10^6

$Tcpu(P1) = 10^6 \times 1.25/4 \times 10^9 = 0.315 \times 10^{-3}$ s

$Tcpu(P2) = 10^6 \times 0.75/3 \times 10^9 = 0.25 \times 10^{-3}$ s

clock rate(P1) > clock rate(P2), but performance(P1) < performance(P2)

1.14.2

P1: 10^6 instructions, $Tcpu(P1) = 0.315 \times 10^{-3}$ s

P2: $Tcpu(P2) = N \times 0.75/3 \times 10^9$ then $N = 1.26 \times 10^6$

1.14.3 MIPS = Clock rate $\times 10^{-6}$/CPI

$MIPS(P1) = 4 \times 109 \times 10^{-6}/1.25 = 3200$

$MIPS(P2) = 3 \times 109 \times 10^{-6}/0.75 = 4000$

MIPS(P1) < MIPS(P2), performance(P1) < performance(P2) in this case (from 1.14.1)

1.15

Another pitfall cited in Section 1.8 is expecting to improve the overall performance of a computer by improving only one aspect of the computer. This might be true, but not always. Consider a computer running programs with CPU times shown in the following table.

	FP instr.	INT instr.	L/S instr.	Branch instr.	Total time
a.	35 s	85 s	50 s	30 s	200 s
b.	50 s	80 s	50 s	30 s	210 s

1.15.1 [5] <1.8> How much is the total time reduced if the time for FP operations is reduced by 20%?

1.15.2 [5] <1.8> How much is the time for INT operations reduced if the total time is reduced by 20%?

1.15.3 [5] < 1.8> Can the total time be reduced by 20% by reducing only the time for branch instructions?

1.15.1 $T_{fp} = 35 \times 0.8 = 28$ s, $T_{p1} = 28 + 85 + 50 + 30 = 193$ s. Reduction: 3.5%

1.15.2 $T_{p1} = 200 \times 0.8 = 160$ s, $T_{fp} + T_{l/s} + T_{branch} = 115$ s, $T_{int} = 45$ s. Reduction time INT: 47%

1.15.3 $T_{p1} = 200 \times 0.8 = 160$ s, $T_{fp} + T_{int} + T_{l/s} = 170$ s. NO