Experiment 4: Combinational Circuit 3

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## **ALU**

## Overview of the experiment:

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| The purpose of the experiment is to form a ALU circuit using VHDL behavioural modelling. In this circuit, we have to put the value of S1 and S0, and for different combinational values of S1 and S0, different operations are operated on the input.  I first roughly sketched the schematic diagram of the circuit according to the inputs and the outputs, and written VHDL codes to synthesis the circuit using behavioural modelling and test the outputs corresponding to different inputs using a testbench and verified my circuit from the waveforms in the simulations. After that, with the help of Krypton Board, I had made a scan chain and executed it to verify my results on hardware also.  In this experiment, the circuit schematic diagram, the VHDL codes for the circuit and testbench, RTL view, RTL and Gate-Level simulations, Scan chain results (which are formed using Krypton Board) and the format of the trace-file will be presented. |

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## Approach to the experiment:

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| The approach was to study the truth table of inputs & outputs, study the schematic diagram of the required circuit and form a circuital code according to the requirements. |

## Design document and VHDL code:

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| Now, a DUT is made to form a single input as an input vector of all the 10 inputs and 8 outputs as an output vector. These vectors are passes through a testbench where the outputs are compared with the trace-file of expected outputs. Then, to test the circuit on hardware, to use Krypton Board, dump the svf on it, and the run the scan chain test to verify the results. |

## RTL View:

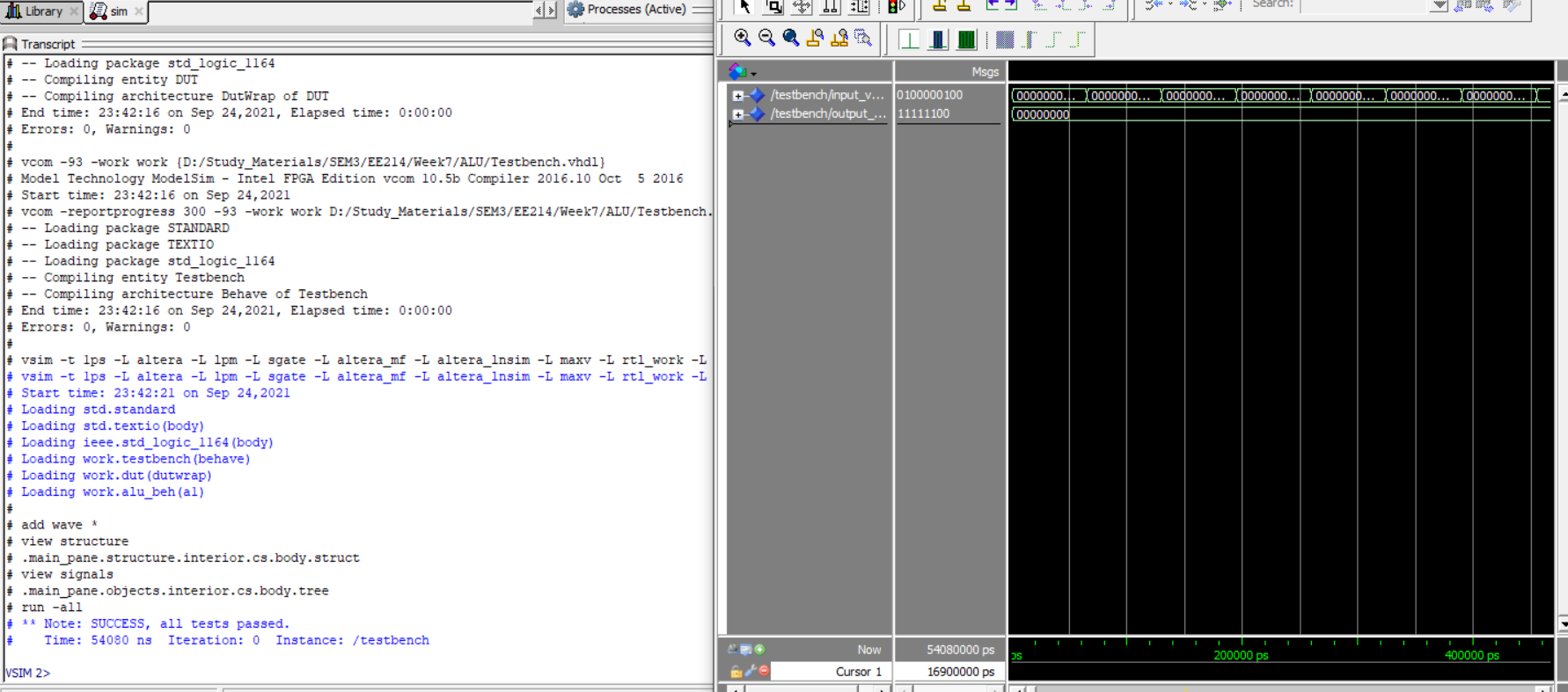
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## DUT Input/Output Format:

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| The format for the input vector is <S1 S0 A3 A2 A1 A0 B3 B2 B1 B0> and for output vector is <Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0>.  Some of the test cases are:  0000010111 10000000 11111111  0011010000 00001101 11111111  0100110001 00000010 11111111  0100110010 00000001 11111111  1010010011 00000100 11111111  1010010100 00000010 11111111  1110000101 00100000 11111111  1110000110 00100000 11111111 |

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## RTL Simulation:



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## Gate-level Simulation:

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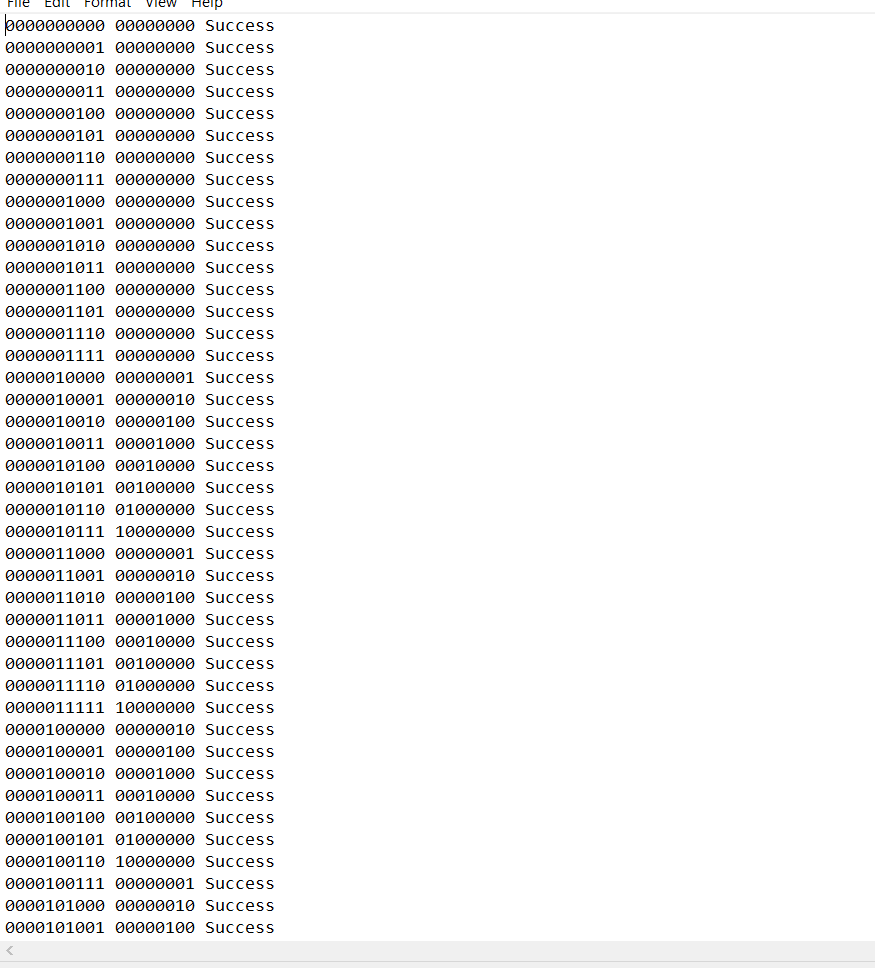
## Krypton board:

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| To test the results on hardware, Krypton Board is used in the experiment. The file named TopLevel.vhdl is made the top-level entity and some files of ScanChain are also added in the Quartus Prime project. After that, a svf file is formed and is dumped on the Krypton Board, and using python, a scan chain process is completed. This process forms a text file named as out.txt which shows that whether the circuit formed on Quartus gives the same output as desired or not. By the end of this, we have checked our experimental output on software as well as hardware. |

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## Observations:

The following is the output file formed by performing scan chain:



## References:

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| * EE113 and EE224 lecture notes. * EE214 Website. |