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VIDYAVIHAR UNIVERSITY
K J Somaiya College of Engineering

K. J. Somaiya College of Engineering, Mumbai-77
(A Constituent College of Somaiya Vidyavihar University)
Department of Computer Engineering

Somaiya
T R U S T

Course Name:	Digital Design Laboratory	Semester:	III
Date of Performance:	16 /09 /2024	Batch No:	A2
Faculty Name:	Shivani Deosthale	Roll No:	16010123032
Faculty Sign & Date:		Grade/Marks:	___/25

Experiment No: 6
Title: Shift Register

Aim and Objective of the Experiment:

To implement the SISO, SIPO, PISO, PIPO shift register using **Universal IC 74194**

COs to be achieved:

CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

Trainer kits

Theory:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop.The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

The basic types of shift registers are
- Serial In - Serial Out
- Serial In - Parallel Out
- Parallel In - Serial Out
- Parallel In - Parallel Out
- Bidirectional shift registers.

Pin diagram of IC 74194 and Function table

74194
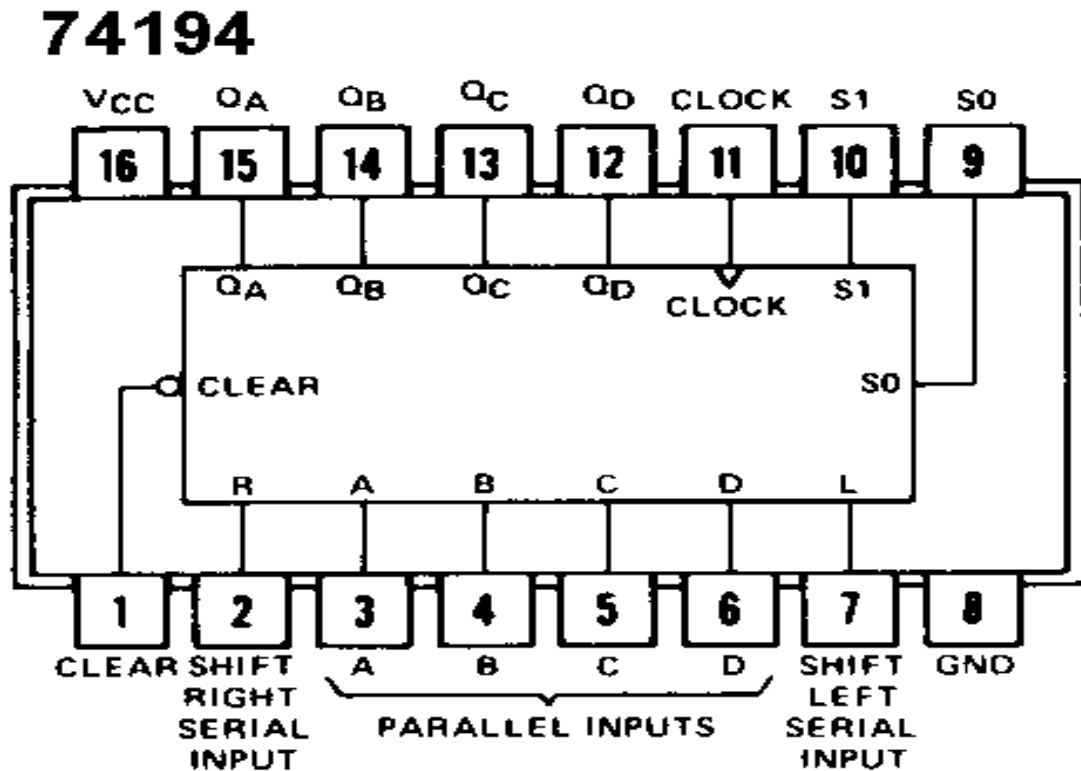
Serial left shift: -

Truth Table

clk	A	B	C	D
1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1

Circuit diagram: Serial right shift

clk	A	B	C	D
1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1

Truth Table

Circuit diagram: Parallel in Parallel out
Truth Table

clk	A	B	C	D
1	a	b	c	d
1	x	x	x	x
1	x	x	x	x
1	x	x	x	x
1	x	x	x	x

Digital Design Laboratory

Semester: III

Academic Year: 2024-25

Roll No:_____

Exp 6 shift register

Universal shift register IC 74194

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CLEAR	Mode		CLK	Serial		||el	Output			
	S_1	S_0		Left	Right	A B C D	Q_A	Q_B	Q_C	Q_D
0	x	x	x	x	x	x x x x	0	0	0	0
1	x	x	⊐	x	x	x x x x	Q_{A_0}	Q_{B_0}	Q_{C_0}	Q_{D_0}
1	1	1	⌐	x	x	a b c d	a	b	c	d
1	0	1	⌐	x	1	x x x x	1	Q_{A_n}	Q_{B_n}	Q_{C_n}
1	0	1	⌐	x	0	x x x x	0	Q_{A_n}	Q_{B_n}	Q_{C_n}
1	1	0	⌐	1	x	x x x x	Q_{B_n}	Q_{C_n}	Q_{D_n}	1
1	1	0	⌐	0	x	x x x x	Q_{B_n}	Q_{C_n}	Q_{D_n}	0
1	0	0	x	x	x	x x x x	Q_{A_0}	Q_{B_0}	Q_{C_0}	Q_{D_0}

Pin diagram

Vcc	Q_A	Q_B	Q_C	Q_D	CLK	S_1	S_0
16	15	14	13	12	11	10	9

IC 74194

1	2	3	4	5	6	7	8
Clear	Shift Right Serial input	A	B	C	D	S.L S.I	GND

16/9

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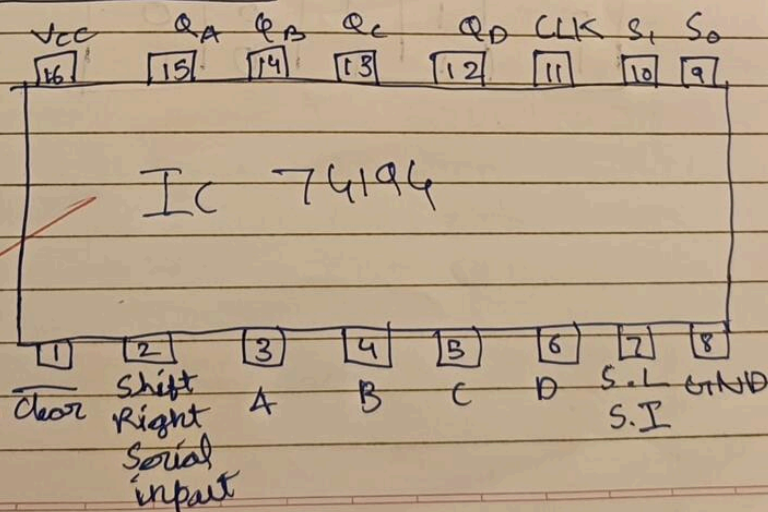
Implementation Details

Procedure
1) Locate IC 74194 on Digital trainer kit
2) Apply various inputs to appropriate pins as per the mode of operation with reference to the pin configuration of the IC.
3) Connect a pulsar switch to the clock input.
4) Verify the respective truth tables for different modes with reference to the truth table given in the data sheet of IC 74194.

Post Lab Subjective/Objective type Questions:

1. What is a universal shift register?
   Answer:

A universal shift register is a versatile digital circuit that can perform both shift and parallel load operations. It's essentially a combination of a shift register and a parallel load register.

Shift Operations:

- **Serial-in, serial-out (SISO):** Data is shifted in and out one bit at a time, typically from left to right.
- **Serial-in, parallel-out (SIPO):** Data is shifted in one bit at a time, but the entire register contents are available in parallel at the output.
- **Parallel-in, serial-out (PISO):** Data is loaded in parallel and then shifted out one bit at a time.
- **Parallel-in, parallel-out (PIPO):** Data is loaded in parallel and then immediately available in parallel at the output.

Universal shift registers can be implemented using various logic gates, such as flip-flops and AND

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gates. The specific implementation depends on the desired shift and load operations and the desired register size.

2. Prepare a truth table for 3 bit SISO left shift with data 011 along with clock pulse

Clock	D	Q2	Q1	Q0
1	0	0	0	0
1	0	0	0	1
1	0	0	1	1
1	0	1	1	1

3. Can a shift register be used as a counter? Give any one application.
   Answer:
Yes, a shift register can be used as a counter. When configured in a specific manner, a shift register can increment or decrement its stored value with each clock pulse. This is achieved by connecting the output of the register back to its input, creating a feedback loop. By controlling the direction of the shift (left or right) and the initial value loaded into the register, the counter can count up or down in a desired sequence. One application of a shift register used as a counter is in digital clocks and timers. The counter can keep track of the elapsed time by incrementing with each clock pulse, providing the necessary information for displaying the hours, minutes, and seconds.

4. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?
   Answer:
   Eight clock pulses are required to enter a byte of data serially into an 8-bit shift register.

Conclusion:

We successfully implemented SISO, SIPO, PISO, PIPO shift register using **Universal IC 74194**