K. J. Somaiya College of Engineering, Mumbai-77
(A Constituent College of Somaiya Vidyavihar University)
Department of Computer Engineering

SOMAIYA
VIDYAVIHAR UNIVERSITY
K J Somaiya College of Engineering

Course Name:	**Digital Design Laboratory**	Semester:	**III**
Date of Performance:	07 / 10 / 2024	Batch No:	A2
Faculty Name:	**Shivani Deosthale**	Roll No:	16010123032
Faculty Sign & Date:		Grade/Marks:	___/25

Experiment No: 8
Title: **1-bit adder on VHDL**

Aim and Objective of the Experiment:

To implement 1-bit adder on VHDL

COs to be achieved:

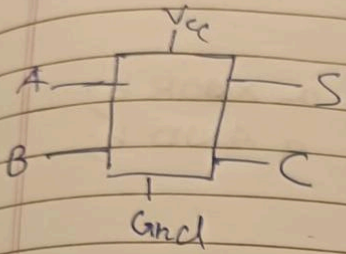**CO4**: Implement digital networks using VHDL

Tools used:

Quartus, ModelSim

Theory:

A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input. Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems.

Implementation Details

Half adder

A	B	XNOR	AND
		S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY half-adder IS
   PORT (
      a :    IN STD_LOGIC;
      b :    IN STD_LOGIC;
      s :    OUT STD_LOGIC;
      c :    OUT STD_LOGIC; )

END half-adder;
```

```
ARCHITECTURE model OF half_adder
IS
BEGIN
        S <= a XOR b;
        c <= a AND b;

END model;
```

Post Lab Subjective/Objective type Questions:

1. How can 1-bit adder be used to implement a 4-bit adder?
   Answer:
   A 4-bit ripple-carry adder can be constructed by cascading four 1-bit adders. The carry output of each adder is connected to the carry input of the next adder, allowing the carry bit to propagate through the chain. The input bits of the two 4-bit numbers are fed to the corresponding input bits of the adders, and the sum and carry bits produced by each adder are combined to form the 4-bit sum.

2. What is VHDL used for?
   Answer:
   VHDL (VHSIC Hardware Description Language) is a hardware description language (HDL) used to design and model digital circuits. It's a popular choice in the electronics industry for several reasons:

   ● **Circuit Description:** VHDL provides a structured way to describe the behavior and structure of digital circuits, making it easier to understand, design, and simulate complex systems.
   ● **Simulation and Verification:** VHDL simulations can be used to test the functionality of a circuit design before it's physically implemented, helping to identify and correct errors early in the development process.
   ● **Reusability:** VHDL modules can be designed and reused in different projects, promoting

efficiency and reducing development time.

Conclusion:

We learnt about VHDL and its uses and implemented it by constructing a 1 bit adder.

Signature of faculty in-charge with Date: