Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**30 /09 /2024**	**Batch No:**	**A2**
Faculty Name:	**Shivani Deosthale**	**Roll No:**	**16010123032**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 7
Title: Asynchronous Counter

Aim and Objective of the Experiment:

To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:

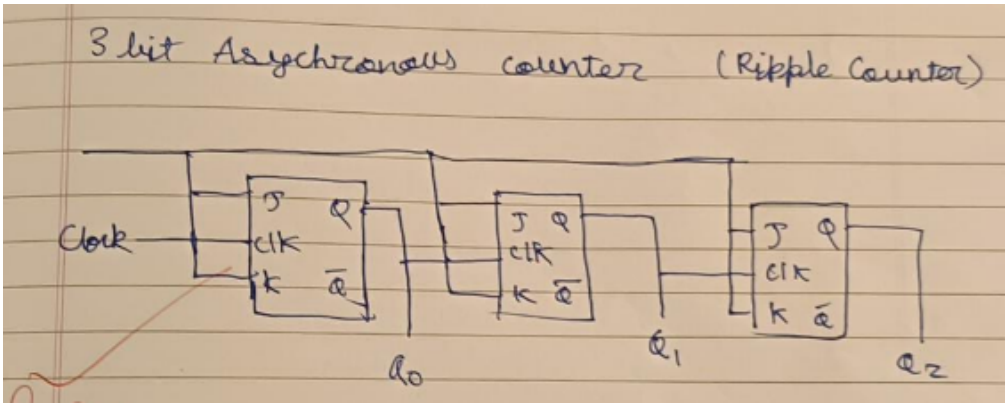
CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

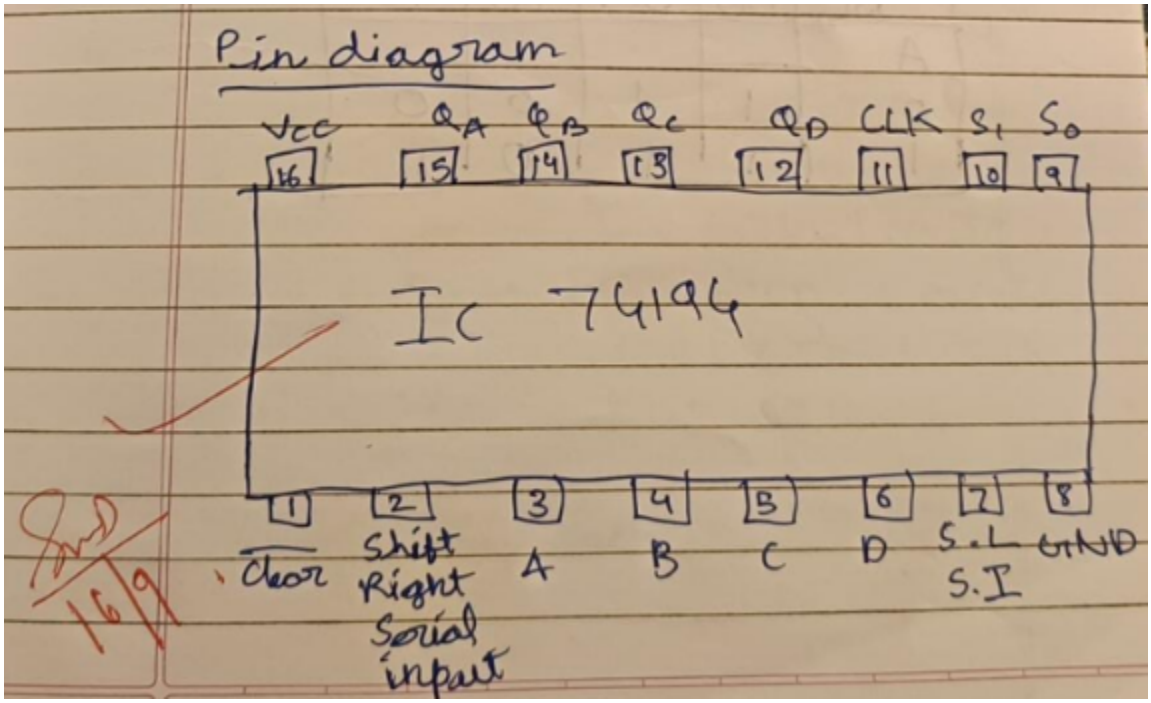
Trainer kits

Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)



Pin diagram of JK FF (IC 7476)



Implementation Details

Procedure

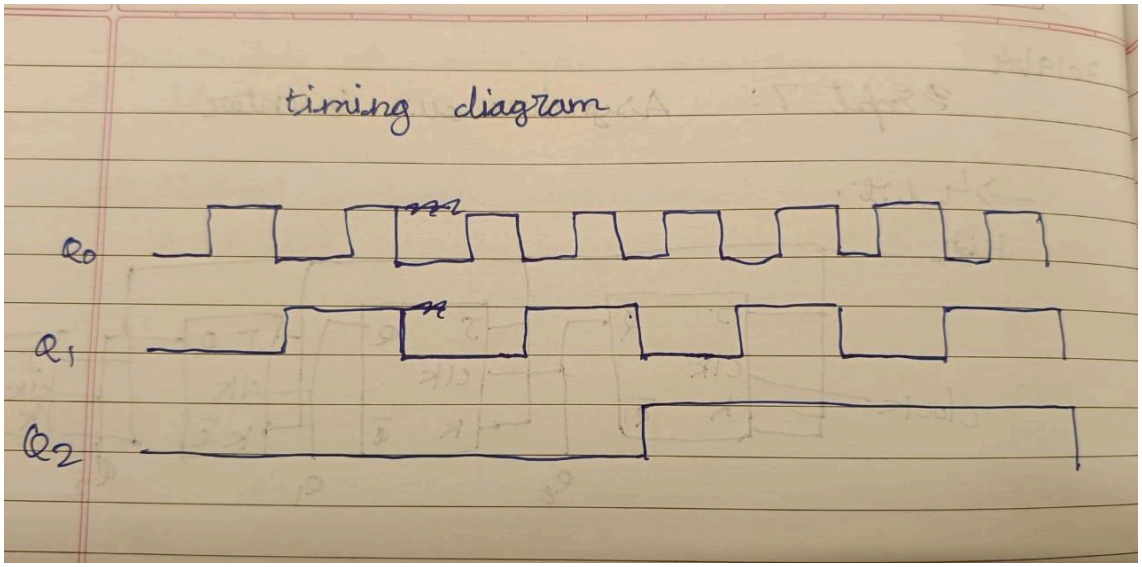
1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

1. How does JK FF need to be configured to use for counter operation?
   Answer:
   To configure a JK flip-flop for counter operation, connect the J and K inputs together to a constant logic 1. This creates a toggle flip-flop that changes its output state (Q) on each rising edge of the clock signal. The Q and Q' outputs can be used to provide the count value, creating a sequence of 0 and 1 values that can represent a binary counter. The clock frequency determines the counting speed, and multiple JK FFs can be connected in series to create larger counters.

2. What changes are required to use the same counter as a 3 bit asynchronous down counter?
   Answer:
   To convert a JK flip-flop counter into a 3-bit asynchronous down counter, invert the clock signal and connect the Q' outputs to the J and K inputs of each flip-flop. This will cause the flip-flops to toggle on the falling edge of the clock, effectively decrementing the count.

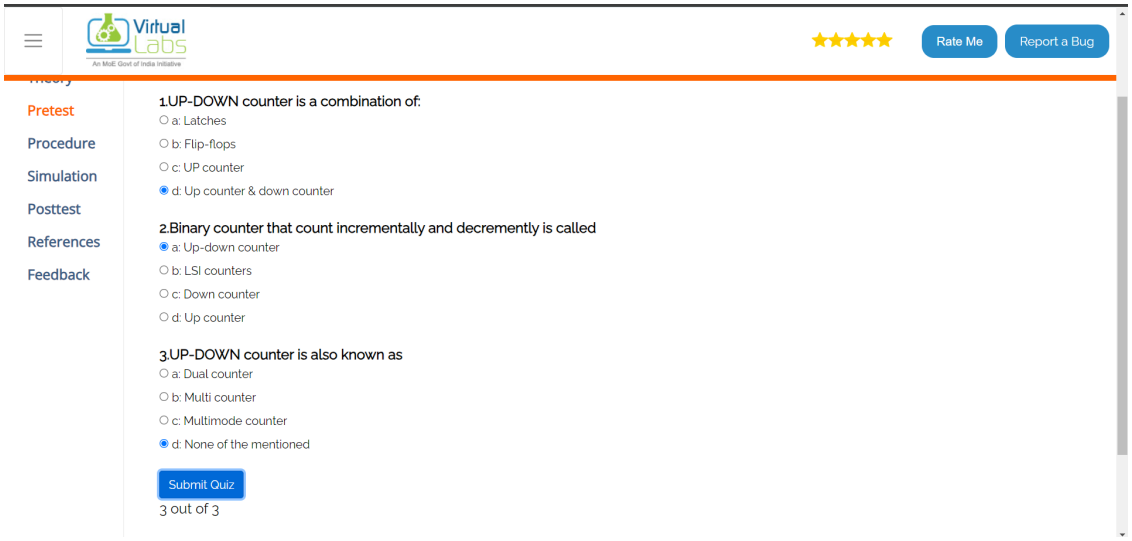
3. Draw the timing diagram of 3 bit Asynchronous up counter.
   Answer:

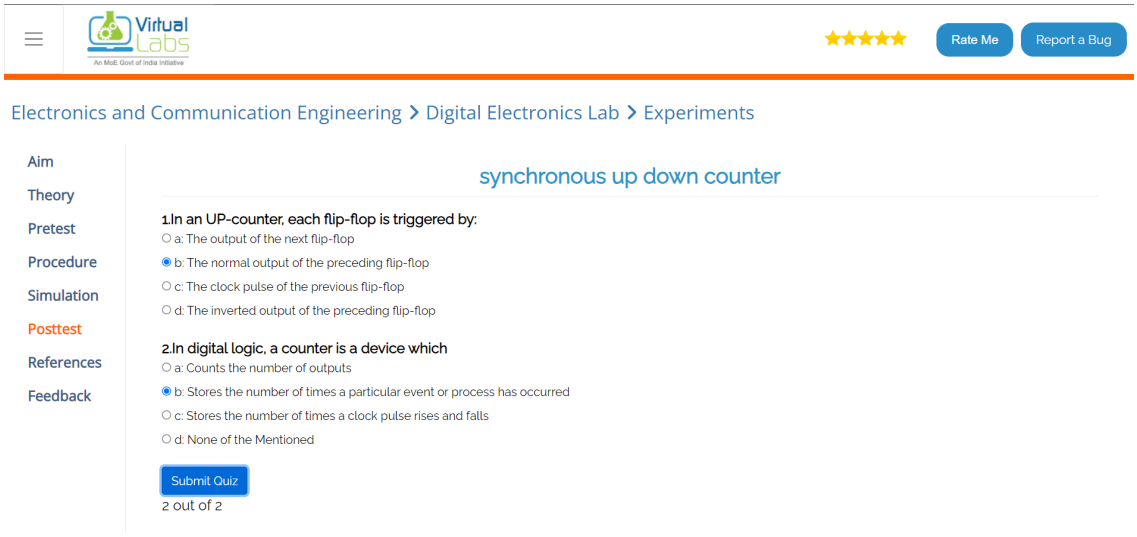


4. What is the mod n concept used in counters?
   Answer:
   Mod-n counters are digital circuits that count from 0 to n-1 and then repeat, where n is a positive integer. They are used when a specific counting sequence is needed. The counter's modulus (n) determines the number of unique states it can reach. Flip-flops and logic gates are used to create mod-n counters, which are applied in various applications like frequency division, digital timers, pattern generators, and phase-locked loops.

5. For Mod-5 counter how many JK FFs are required?
   Answer:
   A mod-5 counter requires **three JK flip-flops**. This is because 2^3 = 8, which is the smallest power of 2 greater than or equal to 5. Three flip-flops can represent 8 unique states (0 to 7), but only the first 5 states (0 to 4) are used in a mod-5 counter. The remaining 3 states (5 to 7) are typically ignored or reset to 0.

6. Virtual Lab for synchronous up down counter. Perform Simulation and give feedback.
   Virtual Labs (vlabs.ac.in)
   Answer:





Conclusion:
We successfully designed and implemented a 3 bit Asynchronous up counter using JK Flip Flop

Signature of faculty in-charge with Date: