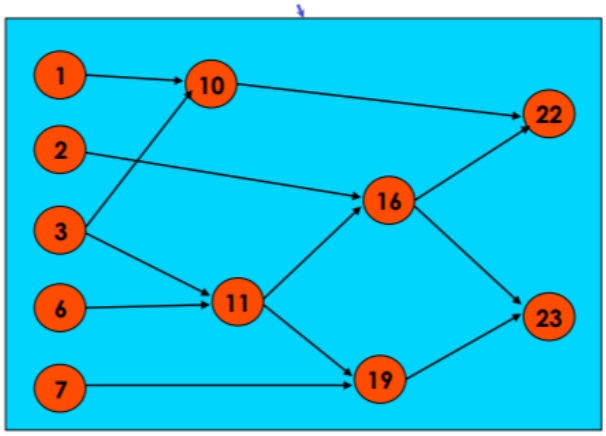
```
// Verilog
// c17
// Ninputs 5
// Noutputs 2
// NtotalGates 6
// NAND2 6

module c17 (N1,N2,N3,N6,N7,N22,N23);

input N1,N2,N3,N6,N7;

output N22,N23;

wire N10,N11,N16,N19;

nand NAND2_1 (N10, N1, N3);
nand NAND2_2 (N11, N3, N6);
nand NAND2_3 (N16, N2, N11);
nand NAND2_4 (N19, N11, N7);
nand NAND2_5 (N22, N10, N16);
nand NAND2_6 (N23, N16, N19);

endmodule
```




Write an MPI program for the following
Step1: Construct a graph for the above code/circuit by considering primary I/Os and wires as nodes

Step2: Given an output (consider either1/0), you need to generate all possible input test vectors required for that particular output with a constraint that atleast one toggling should happen at each node (gate in circuit). For example there are ‘n’ possible test vectors without any constraints , after applying the above stated constraint of toggling you may get ‘t’ test vectors in the range $0 \leq t \leq n$
Toggling constraint:
Example1: NAND Gate
If the circuit has a nand gate with inputs (a,b), the given output (out) to be produced is 1, then all the possible test vectors are 00/01/10. Here atleast one toggle happens from inputs to output i.e
a=> out is 0=>1 (toggle) for two cases . And b=> out is 0=>1 (toggle) for one case.

Example2 :AND gate
If the circuit has a and gate with inputs (a,b), the given output (out) to be produced is 1, then all the possible test vectors are 11. Here there is no possible toggle to happen from input to output.

NB: Consider both cases for output i.e out=0,1 and generate test vectors for both cases .

Important Links:
http://www.pld.ttu.ee/~maksim/benchmarks/iscas85/verilog/c7552.v
http://www.pld.ttu.ee/~maksim/benchmarks/iscas85/verilog/c17.v