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**MSPM’S**

**Deogiri Institute of Engineering and Management Studies, Aurangabad**

**Project Topic**

Laptops

Lenovo L340 laptop

Submitted By

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CERTIFICATE

This is to Certify that Patil Ajay Jamsing has Completed Word Document Presentation of Computer Architecture And Organisation on **\*\*\*\*\*** For the partial fulfillment of Continuous Assessment on date 31/08/2019

**Name and Signature of Student Name and Signature of Subject Teacher**

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INTRODUCTION

Liu Chuanzhi founded Lenovo on 1 November 1984 with a group of ten engineers in Beijing with 200,000 yuan. The Chinese government approved Lenovo's incorporation on the same day. Jiǎ Xùfú , one of the founders of Lenovo, indicates the first meeting in preparation for starting the company was held on 17 October of the same year. Eleven people, the entirety of the initial staff, attended. Each of the founders was a middle-aged member of the Institute of Computing Technology attached to the Chinese Academy of Sciences. The 200,000 yuan used as start-up capital was approved by Zēng Màocháo . The name for the company agreed upon at this meeting was the Chinese Academy of Sciences Computer Technology Research Institute New Technology Development Company.

Lenovo became publicly traded after a 1994 Hong Kong listing that raised nearly US$30 million. Prior to its IPO, many analysts were optimistic about Lenovo. The company was praised for its good management, strong brand recognition, and growth potential. Analysts also worried about Lenovo's profitability. Lenovo's IPO was massively over-subscribed. On its first day of trading, the company's stock price hit a high of HK$2.07 and closed at HK$2.00. Proceeds from the offering were used to finance sales offices in Europe, North America and Australia, to expand and improve production and research and development, and to increase working capital.

Features

One serious gaming laptop

All the power and performance you need to test your wits against the very best. A full-sized keyboard with ambient backlighting. And a slick, stylish design. The IdeaPad L340 Gaming (15) is a real gamer's laptop, from the inside out.

Brings out the gamer in you

With up to 9th Gen Intel® Core™ i7 processing, the IdeaPad L340 Gaming has all the power you need to outshoot, outrun, and outsmart anyone. For an even better gaming experience, go with the Intel® Optane™ option for faster start-up times and quicker game launches.



The new supercharger

GeForce® GTX 1650 gaming laptops are built with the breakthrough graphics performance of the award-winning NVIDIA Turing™ architecture to supercharge your favorite games.

Lose yourself in the game

Hardwired into every IdeaPad L340 is Dolby Audio™. This advanced sound technology is there to take your mobile gaming experience to new levels— and ensure that you have a real blast along the way.



Call all the shots

The IdeaPad L340 has two distinct modes: ‘Quick’ for gaming and ‘Quiet’ for working. Each mode looks, feels, and acts differently. Simply flick between the two based on what you need to do.

Because your privacy counts

Livestream with ease on the IdeaPad L340—and keep your private things private. With a physical shutter on the webcam, you can shut off your camera from the outside world at any time.



Put eye fatigue to bed

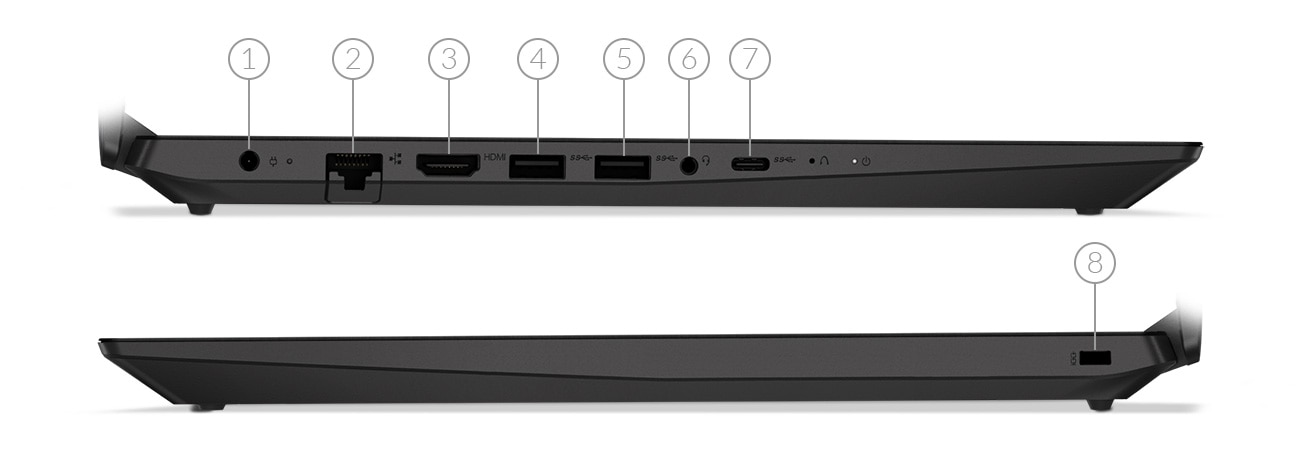
Too many hours gaming can affect your eyes. But with Lenovo Vantage’s Eye Care Mode, you can reduce blue light emission and adjust your display’s color tone, countering the risk of eye strain and fatigue.

Why waste valuable gaming time?

With up to 9 hours' battery life, the IdeaPad L340 lets you battle it out all day. Even better, the battery recharges rapidly to 80% within 60 minutes and to 100% within 120 minutes.



Ports/Slots



* 1. DC power jack
* 2. RJ45
* 3. HDMI 2.0
* 4. USB 3.1 (Gen. 1)
* 5. USB 3.1 (Gen. 1)
* 6. Headphone / mic combo
* 7. USB Type-C
* 8. Kensington lock slot

Tech Specs

|  |
| --- |
|  |
| Processor | Up to 9th Gen Intel® Core™ i7-9750H |
| Operating System | Windows 10 Home |
| Graphics | NVIDIA® GeForce® GTX 1650 |
| Memory | * 4GB DDR4 |
| Battery | Up to 9 hours\*, with Rapid Charge technology  \* Based on MobileMark 2014, an industry standard PC performance benchmark. Actual results will vary depending on your system’s usage and settings, including power management and screen brightness. |
| Storage | * 1TB HDD * 128GB SSD |
| Display | * 15.6" FHD (1920 x 1080), IPS, antiglare, 250 nits, 45% color gamut |
| Security | * TrueBlock Privacy Shutter * TPM * Kensington lock slot |
| Audio | 2x 1.5W speakers with Dolby® Audio® |
| Camera | HD 720p with dual-array mic and physical shutter |
| Dimensions (W x D x H) | 14.3″ x 10.0″ x 0.9″/ 363mm x 254.6mm x 23.9mm |
| Weight | Starting at 2.2kg / 4.8lbs |
| Color Options | Granite Black |
| Connectivity | * 1 x 1 WiFi 802.11 ac * 2 x 2 WiFi 802.11 ac4 + Bluetooth® 4.2 |
| Ports / Slots | * 2 x USB 3.1 (Gen. 1) * USB-C * Headphone / mic combo * HDMI 2.0 * RJ45 |
| Preloaded Software | * Lenovo Antivirus Plus * Lenovo PC Manager * Lenovo Utility * Lenovo Vantage * LinkedIn * McAfee LiveSafe™ |

PROCESSOR ARCHITECTURE

When learning assembly for a given platform, the first place to start is to learn the register set.

**General Architecture**

Since the 64-bit registers allow access for many sizes and locations, we define a byte as 8 bits, a word as 16 bits, a double word as 32 bits, a quad word as 64 bits, and a double quad word as 128 bits. Intel stores bytes “little endian,” meaning lower significant bytes are stored in lower memory address.

[Figure 1](file:///C:\Users\Jai-Hanuman\Downloads\Introduction_to_x64_Assembly.docx#page2)

shows sixteen general purpose 64-bit registers, the first eight of which are labeled (for historical reasons) RAX, RBX, RCX, RDX, RBP, RSI, RDI, and RSP. The second eight are named R8-R15. By replacing the initial R with an E on the first eight registers, it is possible to access the lower 32 bits (EAX for RAX).

Similarly, for RAX, RBX, RCX, and RDX, access to the lower 16 bits is possible by removing the initial R (AX for RAX), and the lower byte of the these by switching the X for L (AL for AX), and the higher byte of the low 16 bits using an H (AH for AX).

The new registers R8 to R15 can be accessed in a similar manner like this: R8 (qword), R8D (lower d word), R8W (lowest word), R8B (lowest byte MASM style, Intel style R8L).

Note there is no R8H.

**SIMD Architecture**

Single Instruction Multiple Data (SIMD) instructions execute a single command on multiple pieces of data in parallel and are a common usage for assembly routines. MMX and SSE commands (using the MMX and XMM registers respectively) support SIMD operations, which perform an instruction on up to eight pieces of data in parallel. For example, eight bytes can be added to eight bytes in one instruction using MMX.

The eight 64-bit MMX registers MMX0-MMX7 are aliased on top of FPR0-7, which means any code mixing FP and MMX operations must be careful not to overwrite required values. The MMX instructions operate on integer types, allowing byte, word, and double word operations to be performed on values in the MMX registers in parallel. Most MMX instructions begin with „P‟ for “packed”. Arithmetic, shift/rotate, comparison, e.g.: PCMPGTB “Compare packed signed byte integers for greater than”.

The sixteen 128-bit XMM registers allow parallel operations on four single or two double precision values per instruction.

Some instructions also work on packed byte, word, double word, and quad word integers. These instructions, called the Streaming SIMD Extensions (SSE), come in many flavors: SSE, SSE2, SSE3, SSSE3, SSE4, and perhaps more by the time this prints. Intel has announced more extensions along these lines called Intel® Advanced Vector Extensions (Intel® AVX), with a new 256-bit-wide data path. SSE instructions contain move, arithmetic, comparison, shuffling and unpacking, and bitwise operations on both floating point and integer types. Instruction names include such beauties as PMULHUW and RSQRTPS.

Finally, SSE introduced some instructions for memory pre-fetching (for performance) and memory fences (for multi-threaded safety).

[Table](file:///C:\Users\Jai-Hanuman\Downloads\Introduction_to_x64_Assembly.docx#page5) lists some command sets, the register types operated on, the number of items manipulated in parallel, and the item type. For example, using SSE3 and the 128-bit XMM registers, you can operate on 2 (must be 64-bit) floating point values in parallel, or even 16 (must be byte sized) integer values in parallel.

To find which technologies a given chip supports, there is a CPUID instruction that returns processor-specific information.

**Table**

|  |  |  |  |
| --- | --- | --- | --- |
| Technology | Register size/type | Item type | Items in Parallel |
| MMX | 64 MMX | Integer | 8,4,2,1 |
| SSE | 64 MMX | Integer | 8,4,2,1 |
| SSE | 128 XMM | Float | 4 |
| SSE2/SSE3/SSSE3… | 64 MMX | Integer | 2,1 |
| SSE2/SSE3/SSSE3… | 128 XMM | Float | 2 |
| SSE2/SSE3/SSSE3… | 128 XMM | Integer | 16,8,4,2,1 |

**Addressing Modes**

Before covering some basic instructions, you need to understand addressing modes, which are ways an instruction can access registers or memory. The following are common addressing modes with examples:

* Immediate: the value is stored in the instruction.

**ADD EAX, 14; add 14 into 32-bit EAX**

* Register to register

**ADD R8L, AL** **; add 8 bit AL into R8L**

* Indirect: this allows using an 8, 16, or 32 bit displacement, any general purpose registers for base and index, and a scale of 1, 2, 4, or 8 to multiply the index.

Technically , these also be prefixed with segment FS: or GS: but this is rarely required.

**MOV R8W, 1234[8\*RAX+RCX]; move word at address 8\*RAX+RCX+1234 into R8W**

There are many legal ways to write this. The following are equivalent

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **MOV** | **ECX, dword ptr table[RBX][RDI]** | | | |
| **MOV** | **ECX, dword ptr table[RDI][RBX]** | | | |
| **MOV** | **ECX,** | **dword** | **ptr** | **table[RBX+RDI]** |
| **MOV** | **ECX,** | **dword** | **ptr** | **[table+RBX+RDI]** |

The **dword ptr** tells the assembler how to encode the **MOV** instruction.

* RIP-relative addressing: this is new for x64 and allows accessing data tables and such in the code relative to the current instruction pointer, making position independent code.

Easier to implement.

**MOV AL, [RIP]; RIP points to the next instruction aka NOP NOP**

INSTRUCTIONS SET

Table lists some common instructions. \* denotes this entry is multiple opcodes where the \* denotes a suffix.

**Table – Common Opcodes**

|  |  |  |  |
| --- | --- | --- | --- |
| Opcode | Meaning | Opcode | Meaning |
| MOV | Move to/from/between | AND/OR/XOR/NOT | Bitwise operations |
|  | memory and registers |  |  |
| CMOV\* | Various conditional moves | SHR/SAR | Shift right logical/arithmetic |
| XCHG | Exchange | SHL/SAL | Shift left logical/arithmetic |
| BSWAP | Byte swap | ROR/ROL | Rotate right/left |
| PUSH/POP | Stack usage | RCR/RCL | Rotate right/left through carry |
|  |  |  | bit |
| ADD/ADC | Add/with carry | BT/BTS/BTR | Bit test/and set/and reset |
| SUB/SBC | Subtract/with carry | JMP | Unconditional jump |
| MUL/IMUL | Multiply/unsigned | JE/JNE/JC/JNC/J\* | Jump if equal/not |
|  |  |  | equal/carry/not carry/ many |
|  |  |  | others |
| DIV/IDIV | Divide/unsigned | LOOP/LOOPE/LOOPNE | Loop with ECX |
| INC/DEC | Increment/Decrement | CALL/RET | Call subroutine/return |
| NEG | Negate | NOP | No operation |
| CMP | Compare | CPUID | CPU information |

**RAM (Random Access Memory)**

RAM is a form of computer memory that can be read and changed in any order, typically used to store working data and machine code. A random-access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. In contrast, with other direct-access data storage media such as hard disks, CD-Rs, DVD-RWs and the older magnetic tapes and drum memory, the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.

RAM contains multiplexing and de-multiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be "8-bit" or "16-bit", etc. devices.

Both static and dynamic RAM are considered *volatile*, as their state is lost or reset when power is removed from the system. By contrast, read-only memory (ROM) stores data by permanently enabling or disabling selected transistors, such that the memory cannot be altered. Writeable variants of ROM (such as EEPROM and flash memory) share properties of both ROM and RAM, enabling data to persist without power and to be updated without requiring special equipment. These persistent forms of semiconductor ROM include USB flash drives, memory cards for cameras and portable devices, and solid-state drives. ECC memory (which can be either SRAM or DRAM) includes special circuitry to detect and/or correct random faults (memory errors) in the stored data, using parity bits or error correction codes.

In general, the term *RAM* refers solely to solid-state memory devices (either DRAM or SRAM), and more specifically the main memory in most computers.

**Read-only memory (ROM)**

ROM is a type of non-volatile memory used in computers and other electronic devices. Data stored in ROM cannot be electronically modified after the manufacture of the memory device. Read-only memory is useful for storing software that is rarely changed during the life of the system, sometimes known as firmware. Software applications for programmable devices can be distributed as plug-in cartridges containing read-only memory.

Erasable programmable read-only memory (EPROM) and electrically erasable programmable read-only memory (EEPROM) can be erased and re-programmed, but usually this can only be done at relatively slow speeds, may require special equipment to achieve, and is typically only possible a certain number of times.

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WORKING ON CONTROL UNIT

The **control unit** (CU) is a component of a computer's central processing unit (CPU) that directs the operation of the processor. It tells the computer's memory, arithmetic and logic unit and input and output devices how to respond to the instructions that have been sent to the processor.

The Control unit (CU) is digital circuitry contained within the processor that coordinates the sequence of data movements into, out of, and between a processor's many sub-units.

The result of these routed data movements through various digital circuits (sub-units) within the processor produces the manipulated data expected by a software instruction (loaded earlier, likely from memory).

It controls (conducts) data flow inside the processor and additionally provides several external control signals to the rest of the computer to further direct data and instructions to/from processor external destinations (i.e. memory).

The Control Unit (CU) is generally a sizable collection of complex digital circuitry interconnecting and directing the many execution units (i.e. ALU, data buffers, registers) contained within a CPU.

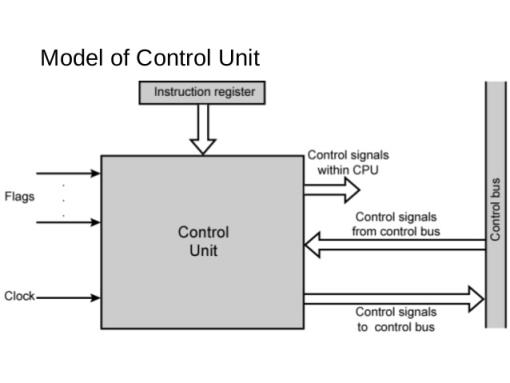
The CU is normally the first CPU unit to accept from an externally stored computer program a single instruction (based on the CPU's instruction set).

The CU then decodes this individual instruction into several sequential steps (fetching addresses/data from registers/memory, managing execution ([i.e. data sent to the ALU or I/O]), and storing the resulting data back into registers/memory) that controls and coordinates the CPU's inner works to properly manipulate the data.

The design of these sequential steps is based on the needs of each instruction and can range in number of steps, the order of execution, and which units are enabled.

Thus by only using a program of set instructions in memory, the CU will configure all the CPU's data flows as needed to manipulate the data correctly between instructions.

This result in a computer that could run a complete program and require no human intervention to make hardware changes between instructions (as had to be done when using only punch cards for computations before stored

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INPUT/OUTPUT MECHANISM

The process of giving input to computer and giving output from computer is called input/ output. The mechanism almost same for input and output. The operating system is mainly responsible for input output operating interrupt and error handling is important terms related to input/outputs.

*I/O devices are divided into two categories*:-

1. **Block devices**: -

  A block devices is one that store information in fixed-sized blocks, each one, with its own address common blocked size ranges from 512 bytes to 32768 bytes. The essential property of a block device is that it is possible to read or write each block independently of all the other ones. In other word, at any instant, the program can read or write any of the blocks. The common examples of block device are disk. A disk is block addressable device because no matter where the arm currently is, it is always possible to seek to another cylinder and then wait for another block to rotate the head.

1. **Character devices**: -

  A character device is one that delivers or accepts a stream of characters, without regards to any blocks structure. It is not accessible and does not have any such operation. The examples of character devices are printers, paper tapes, network interface card, mice and most other devices that are not disk like can be seen as.

**Device controller**

I/O units typically consist of mechanical part and the electronic part. The electronic part is also called the device controller or adapter. On pc, device controller takes the form of printed circuit card that can be inserted into an expansion slots. The controller card actually has a connected on it, into which a cable leading to the device itself can be plugged many controllers can handle more than one identical devices. The standard for interface between controller and device are ANSI, ICE, IDE, SCSI, ISO etc.

The interface between the controller and device is often a very low level interface.The controller job is to convert the serial bit stream into a block of bytes andperform any error.

**COMPONENTS**

**HDD**

Smaller than their desktop and enterprise counterparts, they tend to be slower and have lower capacity. Mobile HDDs spin at 4,200 rpm, 5,200 rpm, 5,400 rpm, or 7,200 rpm, with 5,400 rpm being typical. 7,200 rpm drives tend to be more expensive and have smaller capacities, while 4,200 rpm models usually have very high storage capacities. Because of smaller platter(s), mobile HDDs generally have lower capacity than their desktop counterparts.

There are also 2.5-inch drives spinning at 10,000 rpm, which belong to the enterprise segment with no intention to be used in laptops

**GRAPHICS**

**GPU Engine Specs:**

896 NVIDIA CUDA® Cores

NA Giga Rays/s

1665 Boost Clock (MHz)

1485 Base Clock (MHz)

**Memory Specs:**

8 Gbps Memory Speed

4GB GDDR5 Standard Memory Config

128-bit Memory Interface Width

128 Memory Bandwidth (GB/sec)

Technology Support: :No

Real-Time Ray Tracing :Yes

NVIDIA® GeForce Experience :Yes

NVIDIA Ansel :Yes

NVIDIA® Highlights :Yes

NVIDIA® G-SYNCCompatible :Yes

Game Ready Drivers Yes

Microsoft® DirectX® 12 API, Vulkan API, OpenGL 4.6 : Yes

DisplayPort 1.4a, HDMI 2.0b (2) : Yes

HDCP 2.2 : Yes

NVIDIA® GPU Boost™ : No

VR Ready :No

Designed for USB Type-C and VirtualLink :Yes

:

**Display Support:**

7680x4320@120Hz Maximum Digital Resolution(1)

HDMI 2.0b, DL-DVI-D Standard Display Connectors : Yes

Multi Monitor :Yes

**Graphics Card Dimensions:**

4.37" Height

5.1" Length

2-Slot Width

Thermal and Power Specs:

92 Maximum GPU Temperature (in C)