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**MSPM’S**

**Deogiri Institute of Engineering and Management Studies,**

**Aurangabad**

Project Topic

**Hp Laptop**

**1) HP Pavilion X360 14-CD0050TX**

**2) HP Pavilion 13-AN0046TU**

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2018-2019

**CERTIFICATE**

This is to Certify that **Akshay Tambat** and **Isha Jaiswal** has Completed Word Document Presentation of Computer Architecture And Organisation on Hp laptop For the partial fulfillment of Continuous Assessment on date 31-8-19.

Name and Signature of Student Name and Signature of Subject Teacher

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***1)Introduction:***

***Hewlett-Packard (Hp)***

The Hewlett-Packard Company (commonly referred to as HP, and stylized as hp)or Hewlett-Packard was an American multinational information technology company headquartered in Palo Alto, California. It developed and provided a wide variety of hardware components as well as software and related services to consumers ,small- and medium-sized businesses (SMBs) and large enterprises, including customers in the government, health and education sectors. The company was founded in a one-car garage in Palo Alto by Bill Hewlett and David Packard, and initially produced a line of electronic test equipment. HP was the world&#39;s leading PC manufacturer from 2007 to Q2 2013, at which time Lenovo ranked ahead of HP.

 HP specialized in developing and manufacturing computing, data storage, and networking hardware, designing software and delivering services. Major product lines included personal computing devices, enterprise and industry standard servers, related storage devices, networking products, software and a diverse range of printers and other imaging products. HP directly marketed its products to households, small- to medium-sized businesses and enterprises as well as via online distribution, consumer-electronics and office-supply retailers, software partners and major technology vendors. HP also had services and consulting business around its products and partner products. Hewlett-Packard company events included the spin-off of its electronic and bio-analytical measurement instruments part of its business as Agilent Technologies in 1999, its merger with Compaq in 2002, and the acquisition of EDS in 2008, which led to combined revenues of $118.4 billion in 2008 and a Fortune 500 ranking of 9 in 2009. In November 2009, HP announced the acquisition of 3Com, with the deal closing on April 12, 2010. On April 28, 2010, HP announced the buyout of Palm, Inc. for $1.2 billion. OnSeptember 2, 2010, HP won its bidding war for 3PAR with a $33 a share offer ($2.07 billion), which Dell declined to match.Hewlett-Packard spun off its enterprise products and services business as HewlettPackard Enterprise on November 1, 2015. &quot;We are gradually shaping HP into a more nimble, lower-cost, more customer and partner-centric company that can successfully compete across a rapidly changing IT landscape,&quot; CEO Meg Whitman said at the time. In June 2014, during the HP Discover customer event in Las Vegas, Meg Whitman and Martin Fink announced a project for a radically new computer architecture called The Machine.



***HP Pavilion***

HP Pavilion is a line of personal computers produced by Hewlett-Packard and introduced in 1995. The name is applied to both [desktops](https://en.wikipedia.org/wiki/Desktop_computer) and [laptops](https://en.wikipedia.org/wiki/Laptop) for the Home and Home Office product range. The Pavilion mainly competes against computers such as [Acer](https://en.wikipedia.org/wiki/Acer_Inc.)'s [Aspire](https://en.wikipedia.org/wiki/Acer_Aspire), [Dell](https://en.wikipedia.org/wiki/Dell)'s [Inspiron](https://en.wikipedia.org/wiki/Inspiron) and [XPS](https://en.wikipedia.org/wiki/Dell_XPS), [Lenovo](https://en.wikipedia.org/wiki/Lenovo)'s [IdeaPad](https://en.wikipedia.org/wiki/IdeaPad) and [Toshiba](https://en.wikipedia.org/wiki/Toshiba)'s [Satellite](https://en.wikipedia.org/wiki/Toshiba_Satellite).

When [HP](https://en.wikipedia.org/wiki/Hewlett-Packard) merged with [Compaq](https://en.wikipedia.org/wiki/Compaq) in 2002, it took over Compaq's existing naming rights agreement. As a result, HP sold both HP and Compaq-branded machines until 2013.

**

***2)Specifications:***

***HP Pavilion X360 14-CD0050TX***

HP Pavilion X360 14-CD0050TX is a Windows 10 Home laptop with a 14.00-inch display. It is powered by a Core i3 processor and it comes with 4GB of RAM. The HP Pavilion X360 14-CD0050TX packs 8GB of HDD storage.

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## Full Specifications

**General**

|  |  |
| --- | --- |
| Brand | HP |
| Model | Pavilion X360 14-CD0050TX |
| Model Number | X360 14-CD0050TX |
| Series | Pavilion |
| Colours | Mineral Silver |
| Operating system | Windows 10 Home |

**Display**

|  |  |
| --- | --- |
| Size | 14.00-inch |

**Processor**

|  |  |
| --- | --- |
| Processor | Intel Core i3 |

**Memory**

|  |  |
| --- | --- |
| RAM | 4GB |

**Storage**

|  |  |
| --- | --- |
| Hard disk | 8GB |
| SSD | No |

***HP Pavilion 13-an0046tu***

laptop is loaded with all the essential features. It has a good configuration that works pretty well along with a good RAM capacity that makes multitasking so much easier. It is designed in a compact size and is very lightweight that makes it a perfect option for long business trips. The device is wrapped up at a mid range price but it lacks sufficient storage capacity and a good battery backup. However the addition of a bigger storage capacity and a better battery would have completed the package.

**General Information**

|  |  |  |
| --- | --- | --- |
| Brand |  | HP |
| Model |  | 13-an0046tu (5SE72PA) |
| Dimensions(WxHxD) |  | 311 x 211 x 15.4  mm |
| Weight |  | 1.3 Kg |
| Colors |  | Mineral Silver |
| Operating System |  | Windows 10 Home Basic |
| Operating System Type |  | 64-bit |

**Display Details**

|  |  |  |
| --- | --- | --- |
| Display Size |  | 13.3 Inches (33.78 cm) |
| Display Resolution |  | 1920 x 1080 Pixels |
| Display Type |  | LED |
| Display Features |  | Diagonal FHD IPS BrightView Micro-edge WLED-Backlit Display |
| Display Touchscreen |  | no No |

**Performance**

|  |  |  |
| --- | --- | --- |
| Processor |  | Intel Core i5-8265U (8th Gen) |
| Clock-speed |  | 1.6 Ghz |
| Graphic Processor |  | Intel UHD 620 |

**Memory**

|  |  |  |
| --- | --- | --- |
| Capacity |  | 8 GB |
| RAM type |  | DDR4 |
| RAM speed |  | 2400 Mhz |
| Memory Slots |  | 1 |

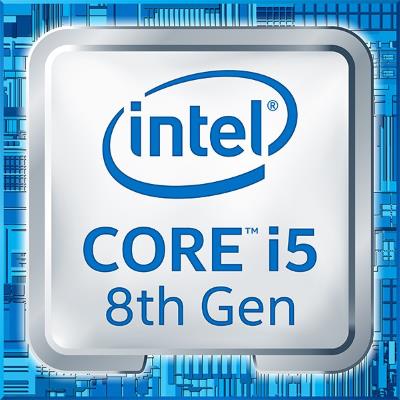
***3)Processor***

**8th Generation (Coffee Lake)**

8th Generation-core based on the [Coffee Lake](https://en.wikichip.org/wiki/intel/microarchitectures/coffee_lake) microarchitecture were introduced in early 2018. Those parts offer are manufactured on Intel's third generation [14 nm++ process](https://en.wikichip.org/wiki/14_nm_process) which allowed for higher clock frequencies. [Coffee Lake](https://en.wikichip.org/wiki/intel/microarchitectures/coffee_lake)-based Core i5s were introduced in late 2017 with a number of high-end SKUs. A larger number of SKUs were introduced in April 2018. Although they still use standard [Socket LGA-1151](https://en.wikichip.org/wiki/intel/lga-1151), those parts are no longer backwards compatible with earlier 100/20series [chipsets](https://en.wikichip.org/w/index.php?title=chipsets&action=edit&redlink=1) and must be paired with an appropriate [300-series chipset](https://en.wikichip.org/w/index.php?title=intel/300-series_chipset&action=edit&redlink=1). A significant configuration change has taken place with the introduction of Coffee Lake including bumping the core count for the Core i5s from [4 cores](https://en.wikichip.org/wiki/4_cores) to [6](https://en.wikichip.org/wiki/6_cores) and appropriately increasing the [L3 cache](https://en.wikichip.org/w/index.php?title=L3_cache&action=edit&redlink=1) which has significantly increased the performance of those parts over the prior generation. Note that with the doubling of the core, Intel has dropped [hyper-threading](https://en.wikichip.org/w/index.php?title=intel/hyper-threading&action=edit&redlink=1) support from those models. All models have the following features in common:

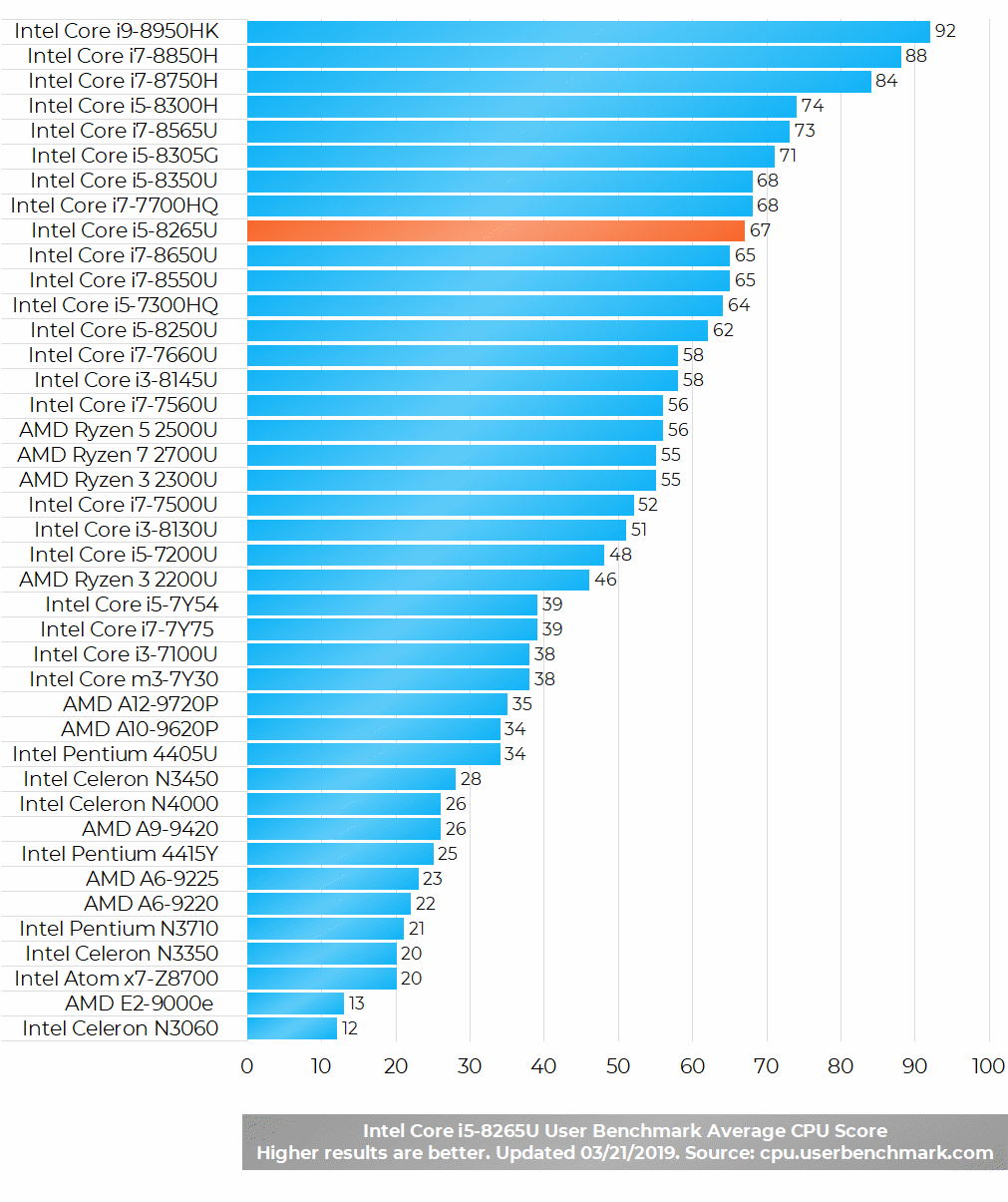
* [Hexa-core](https://en.wikichip.org/wiki/Hexa-core) without [Hyper-threading](https://en.wikichip.org/w/index.php?title=intel/hyper-threading&action=edit&redlink=1), 9 MiB [L3$](https://en.wikichip.org/w/index.php?title=L3$&action=edit&redlink=1)
* **Mem:** Up to 64 [GiB](https://en.wikichip.org/wiki/GiB) of 2666 MT/s [DDR4](https://en.wikichip.org/w/index.php?title=DDR4&action=edit&redlink=1)
* **I/O:** PCIe Gen 3.0 x16 lanes
* **TDP:** 95 W (HP), 65 W (SP), 35 W (LP)
* **GPU:** [UHD Graphics 630](https://en.wikichip.org/wiki/intel/uhd_graphics_630) @ 350 MHz with bursts of 1.05-1.15 GH

# **Intel Core i5-8265U 8th Gen Quad-Core Laptop CPU**

[](https://laptoping.com/cpus/wp-content/uploads/2019/03/Inte-Core-i5-8265U-8th-Gen.jpg)

The 8th Generation **Intel Core i5-8265U** is a mid-range laptop processor. It replaces the widely adopted 8th Gen [i5-8250U](https://laptoping.com/cpus/product/intel-core-i5-8250u/). Both of these quad-core processors belong to the same 8th Gen Intel Core family, so it’s not surprise they are very similar in terms of specs and performance. The only notable difference is that the 8th Gen i5-8265U “Whiskey Lake” chip offers a higher maximal clock speed “TurboBoost” frequency of 3.9 GHz instead of 3.4 GHz.

**Intel Core i5-8265U CPU Benchmark**



Indeed, the benchmarks show a slight advantage of the i5-8265U over the i5-8250U. But in the real-world use, it’s questionable whether you’ll be able to tell the difference at all. Both chips are perfectly suitable for the regular daily computing duties like web browsing, text and spreadsheet processing, video playback, and similar. They also offer a good potential for some heavier stuff like video editing.

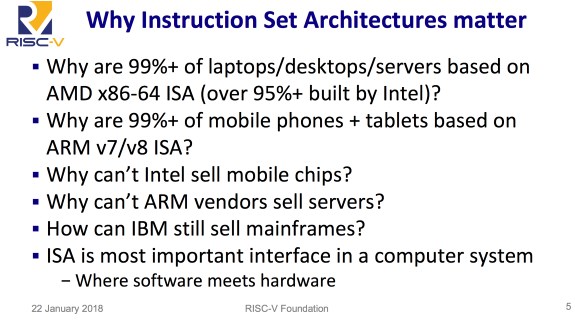
As for gaming, the Core i5-8265U features the same integrated graphics processor as the i5-8250U, without change of the specs. It’s the [Intel UHD 620](https://laptoping.com/gpus/product/intel-uhd-620-graphics-review/) integrated graphics, which is capable of rendering light games and some more demanding titles but on low detail settings. Thanks to the higher clock speed, the i5-8265U can have a slight advantage in some games and gaming scenarios that greatly utilize the main processing cores.

## Specifications of the Intel Core i5-8265U

|  |  |
| --- | --- |
| **Processor Name** | *Intel Core i5-8265U* |
| **CPU Family** | *8th Generation Intel Core "Whiskey Lake"* |
| **Number of Cores** | *Quad-core / 2 threads per core* |
| **CPU Clock Speed** | *1.6 – 3.9 GHz* |
| **Cache Size** | *6MB* |
| **Memory Support** | *DDR3 2133MHz DDR4 2400MHz* |
| **Integrated Graphics** | *Intel UHD 620* |
| **Power Consumption** | *15W* |
| **Production Technology** | *14-nanometer* |

# ***4)Instruction set***

# The **instruction set**, also called **ISA** (**instruction set architecture**), is part of a computer that pertains to programming, which is basically [machine language](https://www.computerhope.com/jargon/m/machlang.htm). The instruction set provides commands to the processor, to tell it what it needs to do. The instruction set consists of addressing modes, instructions, native data types, registers, memory architecture, interrupt, and exception handling, and external [I/O](https://www.computerhope.com/jargon/i/io.htm). An example of an instruction set is the [x86](https://www.computerhope.com/jargon/x/x86.htm) instruction set, which is common to find on computers today. Different computer processors can use almost the same instruction set while still having very different internal design. Both the [Intel](https://www.computerhope.com/comp/intel.htm) Pentium and [AMD](https://www.computerhope.com/comp/amd.htm) Athlon processors use nearly the same x86 instruction set. An instruction set can be built into the hardware of the processor, or it can be emulated in software, using an interpreter. The hardware design is more efficient and faster for running programs than the emulated software version.



**RAM (Random Access Memory)**

RAM is a form of computer memory that can be read and changed in any order,typically used to store working data and machine code. A random-access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. In contrast, with other direct-access data storage media such as hard disks, CD-Rs, DVD-RWs and the older magnetic tapes and drum memory, the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.

RAM contains multiplexing and de-multiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be &quot;8-bit&quot; or &quot;16-bit&quot;, etc. devices.

Both static and dynamic RAM are considered volatile, as their state is lost or reset when power is removed from the system. By contrast, read-only memory (ROM) stores data by permanently enabling or disabling selected transistors, such that the memory cannot be altered. Writeable variants of ROM (such as EEPROM and flash memory) share properties of both ROM and RAM, enabling data to persist without power and to be updated without requiring special equipment. These persistent forms of semiconductor

ROM include USB flash drives, memory cards for cameras and portable devices, and solid-state drives. ECC memory (which can be either SRAM or DRAM) includes special circuitry to detect and/or correct random faults (memory errors) in the stored data, using parity bits or error correction codes. In general, the term RAM refers solely to solid-state memory devices (either DRAM or SRAM), and more specifically the main memory in most computers.

**Read-only memory (ROM)**

ROM is a type of non-volatile memory used in computers and other electronic devices. Data stored in ROM cannot be electronically modified after the manufacture of the memory device. Read-only memory is useful for storing software that is rarely changed during the life of the system, sometimes known as firmware. Software applications for programmable devices can be distributed as plug-in cartridges containing read-only memory. Erasable programmable read-only memory (EPROM) and electrically erasable programmable read-only memory (EEPROM) can be erased and re-programmed, but usually this can only be done at relatively slow speeds, may require special equipment to achieve, and is typically only possible a certain number of times.

***5)Memory***

# **DDR4 SDRAM**

|  |  |
| --- | --- |
| **DDR4 SDRAM Double Data Rate 4 Synchronous Dynamic Random-Access Memory** | |
| Type of [RAM](https://en.wikipedia.org/wiki/RAM) | |
| 8 [GiB](https://en.wikipedia.org/wiki/Gibibyte) DDR4-2133 ECC 1.2 V [RDIMM](https://en.wikipedia.org/wiki/RDIMM) | |
| **Developer** | [JEDEC](https://en.wikipedia.org/wiki/JEDEC) |
| **Type** | [Synchronous dynamic random-access memory](https://en.wikipedia.org/wiki/Synchronous_dynamic_random-access_memory) (SDRAM) |
| **Generation** | 4th generation |
| **Release date** | 2014 |
| **Standards** | * DDR4-1600 (PC4-12800) * DDR4-1866 (PC4-14900) * DDR4-2133 (PC4-17000) * DDR4-2400 (PC4-19200) * DDR4-2666 (PC4-21333) * DDR4-2933 (PC4-23466) * DDR4-3200 (PC4-25600) |
| [**Clock rate**](https://en.wikipedia.org/wiki/Clock_rate) | 800–2133 MHz |
| [**Voltage**](https://en.wikipedia.org/wiki/Voltage) | 1.2~1.4 V |
| **Predecessor** | [DDR3 SDRAM](https://en.wikipedia.org/wiki/DDR3_SDRAM) |

**Double Data Rate 4 Synchronous Dynamic Random-Access Memory**, officially abbreviated as **DDR4 SDRAM**, is a type of [synchronous dynamic random-access memory](https://en.wikipedia.org/wiki/Synchronous_dynamic_random-access_memory) with a high [bandwidth](https://en.wikipedia.org/wiki/Bandwidth_(computing)) ("[double data rate](https://en.wikipedia.org/wiki/Double_data_rate)") interface.

Released to the market in 2014, it is one of the latest variants of [dynamic random-access memory](https://en.wikipedia.org/wiki/Dynamic_random-access_memory) (DRAM), of which some have been in use since the early 1970s, and a higher-speed successor to the [DDR2](https://en.wikipedia.org/wiki/DDR2_SDRAM) and [DDR3](https://en.wikipedia.org/wiki/DDR3_SDRAM) technologies.

DDR4 is not compatible with any earlier type of random-access memory (RAM) due to different signaling voltage and physical interface, besides other factors.

DDR4 SDRAM was released to the public market in Q2 2014, focusing on [ECC memory](https://en.wikipedia.org/wiki/ECC_memory), while the non-ECC DDR4 modules became available in Q3 2014, accompanying the launch of [Haswell-E](https://en.wikipedia.org/wiki/Haswell-E) processors that require DDR4 memory

# **Solid-state drive (SDD)**

|  |  |
| --- | --- |
| **Solid-state drive** | |
| A 2.5-inch [Serial ATA](https://en.wikipedia.org/wiki/Serial_ATA) solid-state drive | |
| **Usage of**[**flash memory**](https://en.wikipedia.org/wiki/Flash_memory) | |
| **Introduced by:** | [SanDisk](https://en.wikipedia.org/wiki/SanDisk) |
| **Introduction date:** | 1991; 28 years ago |
| **Capacity:** | 20 MB (2.5-in form factor) |
| **Original concept** | |
| **By:** | [Storage Technology Corporation](https://en.wikipedia.org/wiki/Storage_Technology_Corporation) |
| **Conceived:** | 1978; 41 years ago |
| **Capacity:** | 45 MB |
| **In 2019 capacities available up to 60 - 100TB** | |
|  | |

A **solid-state drive** (**SSD**) is a [solid-state storage](https://en.wikipedia.org/wiki/Solid-state_storage) device that uses [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) assemblies as [memory](https://en.wikipedia.org/wiki/Computer_storage) to store data [persistently](https://en.wikipedia.org/wiki/Persistence_(computer_science)), typically using [flash memory](https://en.wikipedia.org/wiki/Flash_memory). It is also sometimes called a **solid-state device** or a **solid-state disk**,[[1]](https://en.wikipedia.org/wiki/Solid-state_drive#cite_note-1) although SSDs lack the physical spinning [disks](https://en.wikipedia.org/wiki/Hard_disk_drive_platter) and movable [read-write heads](https://en.wikipedia.org/wiki/Disk_read-and-write_head) used by the conventional [electromechanical](https://en.wikipedia.org/wiki/Electromechanical) storage such as [hard drives](https://en.wikipedia.org/wiki/Hard_drive) ("HDD") or [floppy disks](https://en.wikipedia.org/wiki/Floppy_disk).

Compared with the electromechanical drives, SSDs are typically more resistant to physical shock, run silently, and have quicker [access time](https://en.wikipedia.org/wiki/Access_time) and lower [latency](https://en.wikipedia.org/wiki/Latency_(engineering)). SSDs store data in [semiconductor](https://en.wikipedia.org/wiki/Semiconductor) cells. As of 2019, cells can contain between 1 and 4 [bits](https://en.wikipedia.org/wiki/Bit_(computing)) of data. SSD storage devices vary in their properties according to the number of bits stored in each cell, with single bit cells ("SLC") being generally the most reliable, durable, fast, and expensive type, compared with 2 and 3 bit cells ("MLC" and "TLC"), and finally quad bit cells ("QLC") being used for consumer devices that do not require such extreme properties and are the cheapest of the four. In addition, [3D X-Point](https://en.wikipedia.org/wiki/3D_XPoint) memory (sold by [Intel](https://en.wikipedia.org/wiki/Intel) under the Optane brand), stores data by changing the electrical resistance of cells instead of storing electrical charges in cells, and SSDs made from [RAM](https://en.wikipedia.org/wiki/Random-access_memory) can be used for high speed, when data persistence after power loss is not required, or may use battery power to retain data when its usual power source is unavailable.[[4]](https://en.wikipedia.org/wiki/Solid-state_drive#cite_note-SNIA-101-4) [Hybrid drives](https://en.wikipedia.org/wiki/Hybrid_drive) or [solid-state hybrid drives](https://en.wikipedia.org/wiki/Solid-state_hybrid_drive) (SSHDs), such as [Apple's](https://en.wikipedia.org/wiki/Apple_Inc.) [Fusion Drive](https://en.wikipedia.org/wiki/Fusion_Drive), combine features of SSDs and HDDs in the same unit using both [flash memory](https://en.wikipedia.org/wiki/Flash_memory) and a HDD in order to improve the performance of frequently-accessed data.

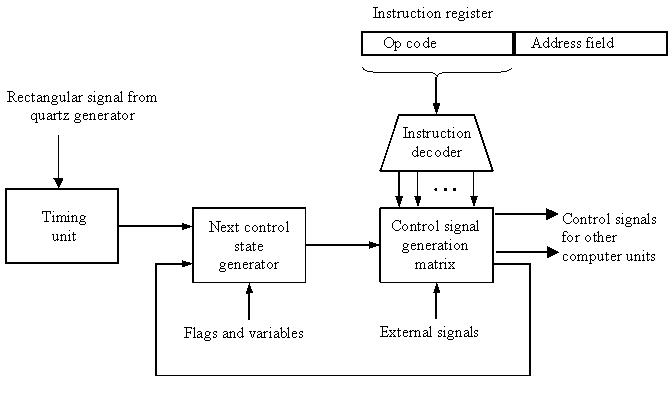
***6)Working of control unit***

A computer control unit is the control unit that is a part of the computer processor. The control unit fetches internal instructions of programs from the main memory to the processor (computer) instruction register and, based on this register contents, generates control signals that supervise execution of these instructions. The control signals are distributed to all smaller and larger elements of the computer that participate in execution of instructions and need to be controlled. The control signals are usually transmitted by the part of the overall system bus called the **control bus**.

There are two types of control units in computers:

* **hardwired control units**
* **micro-programmable (microprogrammed) control units.**

A general block diagram of the hardwired control unit is shown in the figure below.



Block diagram of a hardwired control unit of a computer

The name - hardwired control unit originates from the fact that a part of the control unit - the control signal generator, is hardwired. It means that the control signals that are necessary for instruction execution control are generated by specially designed hardware logical circuits, in which we can not modify the signal generation method without physical change (redesign) of the circuit structure.

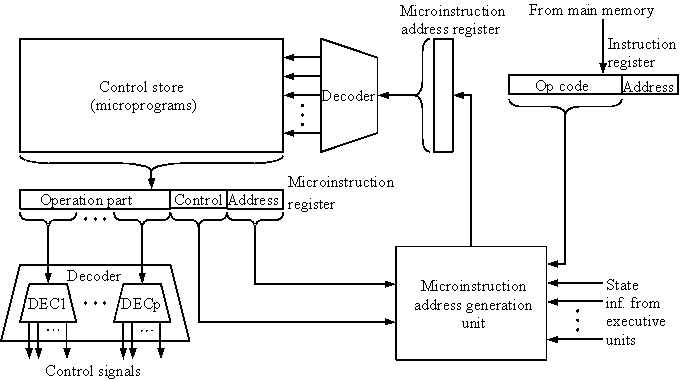
Basic data for control signal generation are contained in the operation code (op code) of an instruction. The operation code is decoded in the instruction decoder. The instruction decoder constitutes (in general) a set of many decoders that decode different fields of the instruction op code. As a result, usually several output lines going out from the instruction decoder obtain active signal values. These lines are connected to the inputs of the matrix that generates control signals for executive units of the computer. This matrix implements logical combinations of the decoded signals from the instruction op code with the outputs from the matrix that generates signals representing consecutive control unit states and with signals coming from the outside of the processor, e.g. interrupt signals. The matrices are built in a similar way as programmable logical arrays.

Control signals for an instruction execution have to be generated not in a single time point but during entire time interval that corresponds to the instruction execution cycle. Following the structure of this cycle, the appropriate sequence of internal states is organized in the control unit. A number of signals generated by the control signal generator matrix is sent back to inputs of the next control state generator matrix. This matrix combines these signals with the timing signals generated by the timing unit based on the rectangular patterns usually supplied by the quartz generator. When a new instruction arrives to the control unit, the control units is in the initial state of new instruction fetching. Instruction decoding makes the control unit enter the first state relating execution of the new instruction, which lasts as long as the timing signals and other input signals as flags and state information of the computer, remain unchanged. A change of any of the mentioned signals stimulates the change of the control unit state. This causes that a new respective input is generated for the control signal generator matrix. When an external signal appears, e.g. an interrupt, the control unit enters a next control state that is the state concerned with the reaction to this external signal, e.g. interrupt processing. The values of flags and state variables of the computer are used to select appropriate states for the instruction execution cycle. The last states in the cycle are control states that initiate fetching the next instruction of the program: sending the program counter content to the main memory address buffer register and next, reading the instruction word to the instruction register of the computer. When the current instruction is the stop instruction that ends program execution, the control unit enters an operating system state, in which it waits for a next user directive.

The block diagrams of microprogrammed control units are shown in next two figures. The basic difference between these unit structures and the structure of the hardwired control unit is the existence of the **control store** (**microprogram memory**) that is used for storing words containing encoded control signals necessary for instruction execution.In microprogrammed control units, subsequent instruction words are fetched into the instruction register in a usual way. However, the operation code of each instruction is not directly decoded to enable immediate control signal generation but it constitutes the initial address of a microprogram contained in the control store.

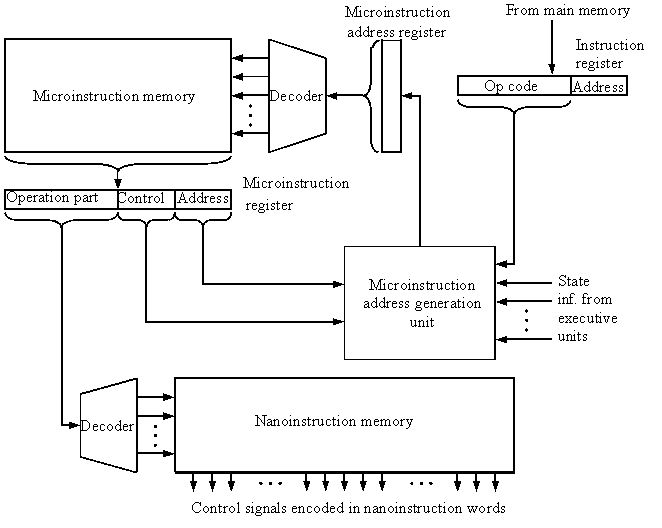
We will now discuss the functioning of the microprogrammed control unit with a single level control unit (see the block diagram below).

The instruction op code from the instruction register is sent to the control store address register. Based on this address, the first microinstruction of a microprogram that **interprets** execution of this instruction is read to the microinstruction register. This microinstruction contains in its operation part encoded control signals, usually as several bit fields. The fields are decoded in a set microinstruction field decoders. Besides the encode control signal fields, the microinstruction contains the address of the next microinstruction of the given instruction microprogram and a control field used to control activities of the microinstruction address generator. The last mentioned field determines the addressing mode (addressing operation) to be applied to the address embedded in the current microinstruction. In microinstructions with the conditional addressing mode, this address is modified with the use of the processor condition flags that represent the status of computations in the current program. The last microinstruction in the microprogram of a given instruction is the microinstruction that fetches the next instruction from the main memory to the instruction register.



Microprogrammed control unit with a single level control store

In a control unit with a two-level control store, besides the control memory for microinstructions, a nanoinstruction memory is included (see the figure below). In such control unit, microinstructions do not contain encoded control signals. The operation part of microinstructions contains the address of the word in the nanoinstruction memory, which contains encoded control signals. The nanoinstruction memory contains all combinations of control signals that appear in microprograms that interpret the complete instruction set of a given computer, written once in the form of nanoinstructions. In this way, redundant storing of the same operation parts of microinstructions is avoided. The microinstruction word in this case can be much shorter than with the single level control store. It gives a much smaller volume in bits of the microinstruction memory and, as a result, a much smaller volume of the entire control memory. The microinstruction memory contains the control for selection of consecutive microinstructions, while that control signals are generated at the basis of nanoinstructions. In nanoinstructions, control signals are frequently encoded using 1 bit/ 1 signal method that eliminates decoding. However, signal encoding in multi-bit fields that requests decoding is also possible.



Microprogrammed control unit with a two-level control store

Microprogrammed control units are frequently applied in the design of contemporary microprocessors. Microprocessors of INTEL x86 series (USA), used in personal computers of the IBM PC type, have microprogrammed control units with a single level control store. Microprocessors Motorola 68xxx series (USA), used for the design of Mackintosh personal computers of the Apple company, have microprogrammed control units with two-level control stores. Microprocessors of the RISC type, designed by DEC-Alpha, Hewlett-Packard, Compaq, SUN companies, have hardwired control units.

***7)Input and Output Mechanism***

The central processing unit is the unseen part of a computer system, and users are only dimly aware of it. But users are very much aware of the input and output associated with the computer. They submit input data to the computer to get processed information, the output.

Sometimes the output is an instant reaction to the input. Consider these examples:

Zebra-striped bar codes on supermarket items provide input that permits instant retrieval of outputs - price and item name - right at the checkout counter.

A bank teller queries the computer through the small terminal at the window by giving a customer's account number as input. The same screen immediately provides the customer's account balance as output.

A forklift operator speaks directly to a computer through a microphone. Words like left, right, and lift are the actual input data. The output is the computer's instant response, which causes the forklift to operate as requested.

A medical student studies the human body on a computer screen, inputting changes to the program to show a close-up of the leg and then to remove layers of tissue to reveal the muscles and bone underneath. The screen outputs the changes, allowing the student (without donning a mask, sanitary gloves, or operating gown) to simulate surgery on the computer.

A sales representative uses an instrument that looks like a pen to enter an order on a special pad. The handwritten characters are displayed as "typed" text and are stored in the pad, which is actually a small computer.

Input and output may sometimes be separated by time or distance or both. Here are some examples:

Factory workers input data by punching in on a time clock as they go from task to task. The time clock is connected to a computer. The outputs are their weekly pay-checks and reports for management that summarize hours per project on a quarterly basis.

A college student writes checks. The data on the checks is used as input to the bank computer, which eventually processes the data to prepare a bank statement once a month.

Charge-card transactions in a retail store provide input data that is processed monthly to produce customer bills.

Water-sample data is collected at lake and river sites, keyed in at the environmental agency office, and used to produce reports that show patterns of water quality.

The examples in this section show the diversity of computer applications, but in all cases the process is the same: input-processing-output. We have already had an introduction to processing. Now, in this chapter we will examine input and output methods in detail.

***8)COMPARISON***

**HP PAVILION 14-N021TU VS HP PAVILION X360 13-S101TU**

**KEY FEATURES COMPARISION**

**OS**

HP Pavilion 14-CD0050tx : Windows 10

HP Pavilion x360 13-an0046tu : Windows 10

**DISPLAY**

HP Pavilion 14-CD0050tx : 14&quot; (1366 x 768)

HP Pavilion x360 13-an0046tu : 13.3&quot; (1920 x 1080)

**PROCESSOR**

HP Pavilion 14-CD0050tx : Intel Core i3 (3rd Generation) | 1.8 Ghz

HP Pavilion x360 13-an0046tu : Intel Core i5 (6th generation) | 2.3 Ghz upto 2.8 Ghz

**MEMORY**

HP Pavilion 14-CD0050tx : 500 GB SATA/8GB DDR3

HP Pavilion x360 13-an0046tu : 1 TB SATA/4GB DDR3

**BASIC INFORMATION**

**MODEL NAME**

HP Pavilion 14-CD0050tx

HP Pavilion x360 13-an0046tu

**OPERATING SYSTEM (WITH VERSION)**

HP Pavilion 14-CD0050tx : Windows 8 (64 bit)

HP Pavilion x360 13-an0046tu : Windows 10 Home 64 bit

**LAPTOP TYPE**

HP Pavilion 14-CD0050tx : Mainstream

HP Pavilion x360 13-an0046tu : Convertible

**DISPLAY**

**RESOLUTION**

HP Pavilion 14-CD0050tx : 1366 x 768

HP Pavilion x360 13-an0046tu : 1920 x 1080

**DISPLAY SIZE (IN INCHES)**

HP Pavilion 14-CD0050tx : 14

HP Pavilion x360 13-an0046tu : 13.3

**DISPLAY TECHNOLOGY**

HP Pavilion 14-CD0050tx : HD BrightView LED-backlit Display

HP Pavilion x360 13-an0046tu : Full HD IPS WLED-backlit touch screen

**CONNECTIVITY**

**WIRELESS CONNECTIVITY**

HP Pavilion 14-CD0050tx : WiFi, Bluetooth 4.0

HP Pavilion x360 13-an0046tu : WiFi, Bluetooth 4.0

**CONNECTIVITY**

HP Pavilion 14-CD0050tx : 2 x USB 3.0, 1 x USB 2.0, HDMI, VGA

HP Pavilion x360 13-an0046tu : 2 x USB 3.0, 1 x USB 2.0, HDMI

**MEMORY**

RAM INCLUDED (IN GB)

HP Pavilion 14-CD0050tx : 8

HP Pavilion x360 13-an0046tu : 4

**RAM TYPE**

HP Pavilion 14-CD0050tx : DDR3

HP Pavilion x360 13-an0046tu : DDR3

**RAM SPEED (IN MHZ)**

HP Pavilion 14-CD0050tx : 1600

HP Pavilion x360 13-an0046tu : 1600

**RAM EXPANDABILITY OPTIONS (NO. OF UNUSED SLOTS)**

HP Pavilion 14-CD0050tx : 2

HP Pavilion x360 13-an0046tu : 2 (Unused Slot - 1)

**PHYSICAL SPECIFICATIONS**

LAPTOP WEIGHT (IN KGS)

HP Pavilion 14-CD0050tx : 1.98

HP Pavilion x360 13-an0046tu : 1.71

**LAPTOP DIMENSION (IN MM)**

HP Pavilion 14-CD0050tx : 346.9 x 239 x 22.6

HP Pavilion x360 13-an0046tu : 346.9 x 239 x 22.6

**PROCESSOR MODEL NAME**

HP Pavilion 14-CD0050tx : Intel Core i3 (3rd Generation)

HP Pavilion x360 13-an0046tu : Intel Core i5 (6th generation)

**CLOCK SPEED**

HP Pavilion 14-CD0050tx : 1.8 Ghz

HP Pavilion x360 13-an0046tu : 2.3 Ghz upto 2.8 Ghz

**ULTRA-LOW VOLTAGE (YES OR NO)**

HP Pavilion 14-CD0050tx : -N021TU : Y

HP Pavilion x360 13-an0046tu : Y

**GRAPHICS PROCESSOR**

HP Pavilion 14-CD0050tx : Intel HD Graphics 4000

HP Pavilion x360 13-an0046tu : Intel HD Graphics 520

**STORAGE**

**HARD DRIVE TYPE**

HP Pavilion 14-CD0050tx : : SATA

HP Pavilion x360 13-an0046tu : SATA