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**MSPM’S**

**Deogiri Institute of Engineering and Management Studies, Aurangabad**

Report on

**Lenovo ideapad330**

Submitted By

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CERTIFICATE

This is to certify that Mrs. **Dipali Sudhakar Kharat** Seat No.26056 has completed a report writing on **Lenovo ideapad 330** in subject Computer Architecture and Organization.

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**Subject Teacher H.O.D. Director**

***Introduction:***

Description: https://upload.wikimedia.org/wikipedia/commons/thumb/d/d7/Lenovo_logo_%28English%29.svg/220px-Lenovo_logo_%28English%29.svg.png



***Lenovo ideapad 330***

* Lenovo Ideapad 330 core i58th Gen-(8GB/1TB HDD/ Windows 10 Home/2GB Graphics) 330-15IKB Laptop (15.6 inch, Onyx Black, 2.2kg)

Lenovo was founded in Beijing in November 1984 as **Legend** and was incorporated in Hong Kong in 1988. Lenovo acquired IBM's personal computer business in 2005 and agreed to acquire its Intel-based server business in 2014. Lenovo entered the Smartphone market in 2012 and as of 2014 was the largest vendor of smart phones in Mainland China. In 2014, Lenovo acquired the mobile phone handset maker Motorola Mobility from Google.

Lenovo is listed on the Hong Kong Stock Exchange and is a constituent of the Hang Seng China-Affiliated Corporations Index, often referred to as "Red Chips".

Lenovo laptops fit any budget while offering many designs and features — from basic family laptops, to high-performance gaming notebooks, to stylish multimode devices with smart designs that adapt to your needs. Match a laptop to your lifestyle.

India:

Lenovo has gained significant market share in India through bulk orders to large companies and government agencies. For example, the government of Tamil Nadu ordered a million laptops from Lenovo in 2012 and single-handedly made the firm a market leader. Lenovo distributes most of the personal computers it sells in India through five national distributors such as Ingram Micro and Redington.

Given that most Smartphone and tablets are sold to individuals Lenovo is pursuing a different strategy making use of many small state-centric distributors. Amar Babu, Lenovo's managing director for India, said, "To reach out to small towns and the hinterland, we have tied up with 40 regional distributors. We want our distributors to be exclusive to us. We will, in turn, ensure they have exclusive rights to distribute Lenovo products in their catchment area." As of 2013, Lenovo had about 6,000 retailers selling Smartphone and tablets in India. In February 2013, Lenovo established a relationship with Reliance Communications to sell Smartphone. The Smartphone carried by Reliance have dual-SIM capability and support both GSM and CDMA. Babu claims that the relative under penetration of Smartphone in India represents an opportunity for Lenovo.Lenovo has assembled a team of senior managers familiar with the Indian market, launched mobile phones at all price points there, and worked on branding to build market share. As of February 2014, Lenovo claims that its sales of Smartphone in India have been increasing 100% per quarter while the market is only growing 15-20% over the same period. Lenovo did marketing tests of its Smartphone in November 2012 in Gujarat and some southern cities, where Lenovo already had a strong presence. Lenovo's strategy has been to create awareness, maintain a broad selection of phones at all price points, and develop distribution networks. Lenovo partnered with two national distributors and over 100 local distributors. As of February 2014, more than 7,000 retail outlets in India sold Lenovo Smartphone. Lenovo has also partnered with HCL in order to set up 250 service centers in 110 cities.

In India, Lenovo grants distributors exclusive territories but allows them to sell computers from other companies. Lenovo uses its close relationships with distributors to gain market intelligence and speed up product development.

Lenovo reported a year-on-year increase of about 951% in tablet sales in India for the first quarter of 2014. Canals, a market research firm, said Lenovo took market share away from Apple and Samsung in the country.

***Features:***

Lenovo:



The LENOVO ideapad330 small-business laptop is perfectly portable, weighing in at just 4.46 pounds (2.2 kg)—yet it features powerful processing and a large 15.6-inch FHD display option, so it's a cinch to work with anywhere. What's more, with the 30 Whr battery option, rapid-charge technology helps to boost productivity levels—in just 30 minutes, the device charges 50%. Plus, it runs up to 6 hours on a single charge. This laptop is highly secure with Trusted Platform Module, which works in conjunction with Windows 10 Home Bitlocker to encrypt data and passwords. And the privacy camera shutter ensures the webcam is off when it's off—no chance of hackers inconspicuously spying.

With Windows 10 Home on your LENOVO ideapad330, you get your very own personal assistant, Cortana. Now, you'll never have to hunt for files, photos, or meetings again—simply let Cortana do the work for you! And when you integrate Cortana with your calendar, you can even search by when and who you worked with on a file, rather than having to remember files names.

***General Information***

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Brand |  | | Lenovo | |
| Model |  | | Ideapad 330s | |
| Dimensions(WxHxD) |  | | 375 x 253 x 22.3  mm | |
| Colors | |  | | Onyx Black | |
| Operating System | |  | | Windows Home 10 | |
| Operating System Type | |  | | 64-bit | |

***Display Details***

|  |  |  |
| --- | --- | --- |
| Display Size |  | 15.6 Inches (39.62 cm) |
| Display  Resolution |  | 1366 x 768 Pixels |
| Display Type |  | LED |
| Display Features |  | HD LED Backlit AntiGlare Display |
| Display Touchscreen |  | Description: no No |

***Performance***

|  |  |  |
| --- | --- | --- |
| Processor |  | Intel Core i5-8th Gen |
| Clock-speed |  | 2.3 Ghz |
| Graphic Processor |  | Intel HD 620 |

***Memory***

|  |  |  |
| --- | --- | --- |
| Capacity |  | 8 GB |
| RAM type |  | DDR4 |
| RAM speed |  | 2133 Mhz |
| Memory  Slot |  | 1 |
| Memory Layout |  | 1x4 Gigabyte |

***Storage***

|  |  |  |
| --- | --- | --- |
| HDD Capacity |  | 1 TB |
| HDD Speed(RPM) |  | 5400 RPM |
| HDD type |  | SATA |

***Battery***

|  |  |  |
| --- | --- | --- |
| Battery Cell |  | 2 Cell |
| Battery type |  | Li-Po |
| Power Supply |  | 45 W AC Adapter W |

***Networking***

|  |  |  |
| --- | --- | --- |
| Wireless LAN |  | 802.11 a/b/g/n/ac |
| Bluetooth |  | Description: yes |
| Bluetooth Version |  | 4.1 |

***Ports***

|  |  |  |
| --- | --- | --- |
| USB 3.0 slots |  | 2 |
| SD Card Reader |  | Description: yes |
| Headphone Jack |  | Description: yes |
| Microphone Jack |  | Description: yes |

***Multimedia***

|  |  |  |
| --- | --- | --- |
| Web-cam |  | Description: yes |
| Video Recording |  | 720p HD |
| Secondary cam(Rear-facing) |  | Description: no No |
| Speakers |  | Dual Speakers |
| In-built Microphone |  | Description: yes |
| Microphone Type |  | Internal Microphone |

***Peripherals***

|  |  |  |
| --- | --- | --- |
| Optical Drive |  | Description: yes |
| Drive Type |  | DVD Reader |
| Pointing Device |  | Touchpad with Multi-Touch Gestures Enabled |
| Keyboard |  | Standard Notebook Keyboard |

***Others***

|  |  |  |
| --- | --- | --- |
| Warranty |  | 1 Year |
| Lockport |  | Description: no No |
| Sales Package |  | Laptop, Battery, AC Adapter, User Guide |

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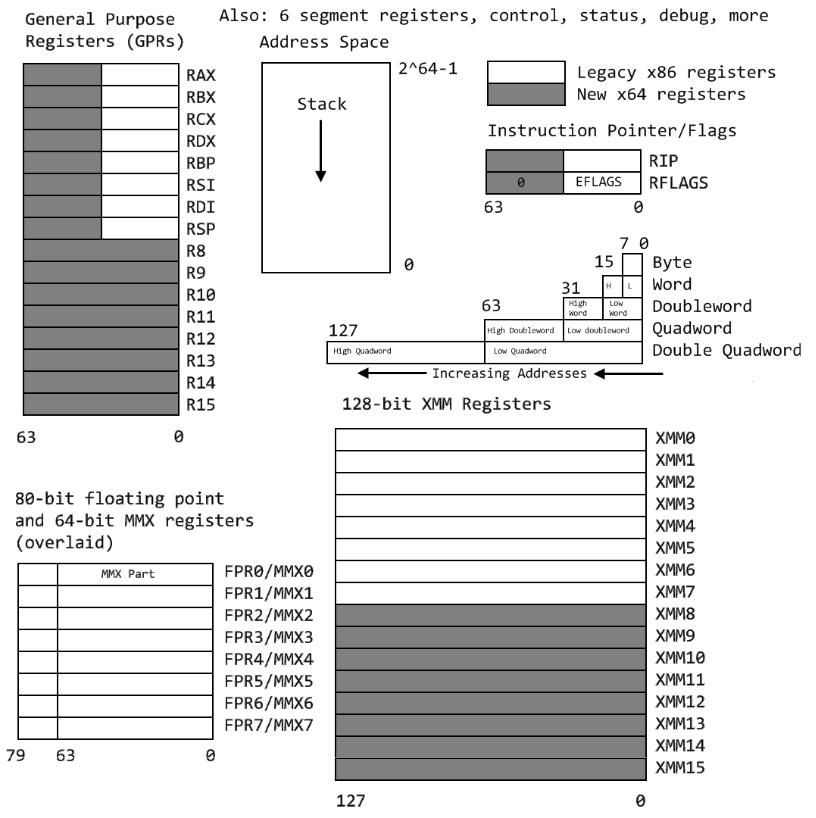
**Architecture**

When learning assembly for a given platform, the first place to start is to learn the register set.

**General Architecture**

Since the 64-bit registers allow access for many sizes and locations, we define a byte as 8 bits, a word as 16 bits, a double word as 32 bits, a quadword as 64 bits, and a double quadword as 128 bits. Intel stores bytes “little endian,” meaning lower significant bytes are stored in lower memory address.

[Figure 1](#page2) shows sixteen general purpose 64-bit registers, the first eight of which are labeled (for historical reasons) RAX, RBX, RCX, RDX, RBP, RSI, RDI, and RSP. The second eight are named R8-R15. By replacing the initial R with an E on the first eight registers, it is possible to access the lower 32 bits (EAX for RAX). Similarly, for RAX, RBX, RCX, and RDX, access to the lower 16 bits is possible by removing the initial R (AX for RAX), and the lower byte of the these by switching the X for L (AL for AX), and the higher byte of the low 16 bits using an H (AH for AX). The new registers R8 to R15 can be accessed in a similar manner like this: R8 (qword), R8D (lower dword), R8W (lowest word), R8B (lowest byte MASM style, Intel style R8L). Note there is no R8H.



**Figure 1 – General Architecture**

**SIMD Architecture**

Single Instruction Multiple Data (SIMD) instructions execute a single command on multiple pieces of data in parallel and are a common usage for assembly routines. MMX and SSE commands (using the MMX and XMM registers respectively) support SIMD operations, which perform an instruction on up to eight pieces of data in parallel. For example, eight bytes can be added to eight bytes in one instruction using MMX.

The eight 64-bit MMX registers MMX0-MMX7 are aliased on top of FPR0-7, which means any code mixing FP and MMX operations must be careful not to overwrite required values. The MMX instructions operate on integer types, allowing byte, word, and doubleword operations to be performed on values in the MMX registers in parallel. Most MMX instructions begin with „P‟ for “packed”. Arithmetic, shift/rotate, comparison, e.g.: PCMPGTB “Compare packed signed byte integers for greater than”.

The sixteen 128-bit XMM registers allow parallel operations on four single or two double precision values per instruction. Some instructions also work on packed byte, word, doubleword, and quadword integers. These instructions, called the Streaming SIMD Extensions (SSE), come in many flavors: SSE, SSE2, SSE3, SSSE3, SSE4, and perhaps more by the time this prints. Intel has announced more extensions along these lines called Intel® Advanced Vector Extensions (Intel® AVX), with a new 256-bit-wide datapath. SSE instructions contain move, arithmetic, comparison, shuffling and unpacking, and bitwise operations on both floating point and integer types. Instruction names include such beauties as PMULHUW and RSQRTPS. Finally, SSE introduced some instructions for memory pre-fetching (for performance) and memory fences (for multi-threaded safety).

[Table](#page5) lists some command sets, the register types operated on, the number of items manipulated in parallel, and the item type. For example, using SSE3 and the 128-bit XMM registers, you can operate on 2 (must be 64-bit) floating point values in parallel, or even 16 (must be byte sized) integer values in parallel.

To find which technologies a given chip supports, there is a CPUID instruction that returns processor-specific information.

**Table**

|  |  |  |  |
| --- | --- | --- | --- |
| Technology | Register size/type | Item type | Items in Parallel |
| MMX | 64 MMX | Integer | 8,4,2,1 |
| SSE | 64 MMX | Integer | 8,4,2,1 |
| SSE | 128 XMM | Float | 4 |
| SSE2/SSE3/SSSE3… | 64 MMX | Integer | 2,1 |
| SSE2/SSE3/SSSE3… | 128 XMM | Float | 2 |
| SSE2/SSE3/SSSE3… | 128 XMM | Integer | 16,8,4,2,1 |

***Instruction Basics***

***Addressing Modes***

Before covering some basic instructions, you need to understand addressing modes, which are ways an instruction can access registers or memory. The following are common addressing modes with examples:

* Immediate: the value is stored in the instruction.

**ADD EAX, 14 ; add 14 into 32-bit EAX**

* Register to register

**ADD R8L, AL** **; add 8 bit AL into R8L**

* Indirect: this allows using an 8, 16, or 32 bit displacement, any general purpose registers for base and index, and a scale of 1, 2, 4, or 8 to multiply the index. Technically, these

can also be prefixed with segment FS: or GS: but this is rarely required.

**MOV R8W, 1234[8\*RAX+RCX] ; move word at address 8\*RAX+RCX+1234 into R8W**

There are many legal ways to write this. The following are equivalent

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **MOV** | **ECX, dword ptr table[RBX][RDI]** | | | |
| **MOV** | **ECX, dword ptr table[RDI][RBX]** | | | |
| **MOV** | **ECX,** | **dword** | **ptr** | **table[RBX+RDI]** |
| **MOV** | **ECX,** | **dword** | **ptr** | **[table+RBX+RDI]** |

The **dword ptr** tells the assembler how to encode the **MOV** instruction.

* RIP-relative addressing: this is new for x64 and allows accessing data tables and such in the code relative to the current instruction pointer, making position independent code

easier to implement.

**MOV AL, [RIP] ; RIP points to the next instruction aka NOP NOP**

Unfortunately, MASM does not allow this form of opcode, but other assemblers like

FASM and YASM do. Instead, MASM embeds RIP-relative addressing implicitly.

**MOV EAX, TABLE ; uses RIP- relative addressing to get table address**

* Specialized cases: some opcodes use registers in unique ways based on the opcode. For example, signed integer division **IDIV** on a 64 bit operand value divides the 128-bit value in **RDX:RAX** by the value, storing the result in **RAX** and the remainder in **RDX.**

***INSTRUCTIONS SET***

[Table](#page7) lists some common instructions. \* denotes this entry is multiple opcodes where the \* denotes a suffix.

**Table – Common Opcodes**

|  |  |  |  |
| --- | --- | --- | --- |
| Opcode | Meaning | Opcode | Meaning |
| MOV | Move to/from/between | AND/OR/XOR/NOT | Bitwise operations |
|  | memory and registers |  |  |
| CMOV\* | Various conditional moves | SHR/SAR | Shift right logical/arithmetic |
| XCHG | Exchange | SHL/SAL | Shift left logical/arithmetic |
| BSWAP | Byte swap | ROR/ROL | Rotate right/left |
| PUSH/POP | Stack usage | RCR/RCL | Rotate right/left through carry |
|  |  |  | bit |
| ADD/ADC | Add/with carry | BT/BTS/BTR | Bit test/and set/and reset |
| SUB/SBC | Subtract/with carry | JMP | Unconditional jump |
| MUL/IMUL | Multiply/unsigned | JE/JNE/JC/JNC/J\* | Jump if equal/not |
|  |  |  | equal/carry/not carry/ many |
|  |  |  | others |
| DIV/IDIV | Divide/unsigned | LOOP/LOOPE/LOOPNE | Loop with ECX |
| INC/DEC | Increment/Decrement | CALL/RET | Call subroutine/return |
| NEG | Negate | NOP | No operation |
| CMP | Compare | CPUID | CPU information |

A common instruction is the LOOP instruction, which decrements RCX, ECX, or CX depending on usage, and then jumps if the result is not 0. For example,

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **XOR** | **EAX, EAX** | **; zero out eax** | | | | |
| **MOV** | **ECX, 10** | **; loop** | | **10** | **Times** | |
| **Label:** |  | **; this** | | **is** | **a** | **label in assembly** |
| **INX** | **EAX** | **;** | **increment** | | | **Eax** |
| **LOOP** | **Label** | **;** | **decrement** | | | **ECX, loop if not 0** |

Less common op codes implement string operations, repeat instruction prefixes, port I/O instructions, flag set/clear/test, floating point operations (begin usually with a F, and support move, to/from integer, arithmetic, comparison, transcendental, algebraic, and control functions), cache and memory opcodes for multithreading and performance issues, and more. The Intel 64 Volume 2, in two parts, covers each opcode in detail.

***Random-access memory (RAM)***

RAM is a form of computer memory that can be read and changed in any order, typically used to store working data and machine code. A random-access memory device allows data items to be read or written in almost the same amount of time irrespective of the physical location of data inside the memory. In contrast, with other direct-access data storage media such as [hard disks](https://en.wikipedia.org/wiki/Hard_disk), [CD-RWs](https://en.wikipedia.org/wiki/CD-RW), DVD-RWs and the older [magnetic tapes](https://en.wikipedia.org/wiki/Magnetic_tape_data_storage) and [drum memory](https://en.wikipedia.org/wiki/Drum_memory), the time required to read and write data items varies significantly depending on their physical locations on the recording medium, due to mechanical limitations such as media rotation speeds and arm movement.

RAM contains [multiplexing](https://en.wikipedia.org/wiki/Multiplexer) and [demultiplexing](https://en.wikipedia.org/wiki/Demultiplexing) circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Usually more than one bit of storage is accessed by the same address, and RAM devices often have multiple data lines and are said to be "8-bit" or "16-bit", etc. devices.

***Types***

The two widely used forms of modern RAM are [static RAM](https://en.wikipedia.org/wiki/Static_random_access_memory) (SRAM) and [dynamic RAM](https://en.wikipedia.org/wiki/Dynamic_random-access_memory) (DRAM). In SRAM, a [bit of data](https://en.wikipedia.org/wiki/Bit) is stored using the state of a six-transistor memory cell. This form of RAM is more expensive to produce, but is generally faster and requires less dynamic power than DRAM. In modern computers, SRAM is often used as cache memory for the CPU DRAM stores a bit of data using a transistor and capacitor pair, which together comprise a DRAM cell. The capacitor holds a high or low charge (1 or 0, respectively), and the transistor acts as a switch that lets the control circuitry on the chip read the capacitor's state of charge or change it. As this form of memory is less expensive to produce than static RAM, it is the predominant form of computer memory used in modern computers.



Both static and dynamic RAM are considered *volatile*, as their state is lost or reset when power is removed from the system. By contrast, read only memory (ROM) stores data by permanently enabling or disabling selected transistors, such that the cannot be altered. Writeable variants of ROM (such as EEPROM and flash memory) share properties of both ROM and RAM, enabling data to persist without power and to be updated without requiring special equipment. These persistent forms of semiconductor ROM include USB flash drives, memory cards for cameras and portable devices, and solid state drive. EEC memory (which can be either SRAM or DRAM) includes special circuitry to detect and/or correct random faults (memory errors) in the stored data, using partial bites or error correction codes.

In general, the term *RAM* refers solely to solid-state memory devices (either DRAM or SRAM), and more specifically the main memory in most computers.

***Read-only memory (ROM)***

ROM is a type of non-volatile memory used in computers and other electronic devices. Data stored in ROM cannot be electronically modified after the manufacture of the memory device. Read-only memory is useful for storing software that is rarely changed during the life of the system, sometimes known as [firmware](https://en.wikipedia.org/wiki/Firmware). Software applications for programmable devices can be distributed as [plug-in cartridges containing read-only memory](https://en.wikipedia.org/wiki/ROM_cartridge).

Erasable programmable read-only memory (EPROM) and electrically erasable programmable read-only memory (EEPROM) can be erased and re-programmed, but usually this can only be done at relatively slow speeds, may require special equipment to achieve, and is typically only possible a certain number of times.

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***Solid-State Drive (SSD)***

A solid-state drive (SSD) is a solid-state storage device that uses integrated circuit assemblies as memory to store data persistently, typically using flash memory. It is also sometimes called a solid-state device or a solid-state disk, although SSDs lack the physical spinning disks and movable read-write heads used by conventional electromechanical storage such as hard drives. ("HDD") or floppy disks.

SSDs based on volatile memory such as DRAM are characterized by very fast data access, generally less than 10 microseconds, and are used primarily to accelerate applications that would otherwise be held back by the latency of flash SSDs or traditional HDDs.

The key components of an SSD are the controller and the memory to store the data. The primary memory component in an SSD was traditionally DRAM volatile memory, but since 2009 it is more commonly NAND flash non-volatile memory.

A flash-based SSD typically uses a small amount of DRAM as a volatile cache, similar to the buffers in hard disk drives. A directory of block placement and wear leveling data is also kept in the cache while the drive is operating. One SSD controller manufacturer, Sand Force , does not use an external DRAM cache on their designs but still achieves high performance. Such an elimination of the external DRAM reduces the power consumption and enables further size reduction of SSDs.

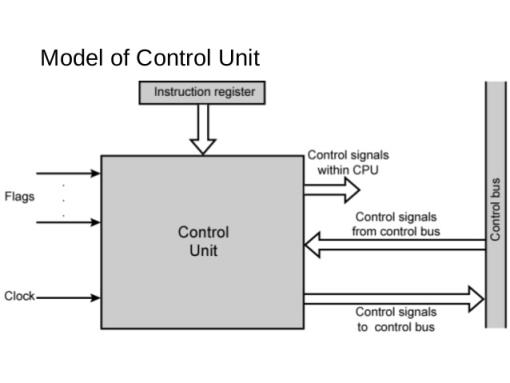
***Working of Control Unit***

The **control unit** (CU) is a component of a computer's central processing unit  (CPU) that directs the operation of the processor. It tells the computer's memory, arithmetic and logic unit and input and output devices how to respond to the instructions that have been sent to the processor.

The Control unit (CU) is digital circuitry contained within the processor that coordinates the sequence of data movements into, out of, and between a processor's many sub-units. The result of these routed data movements through various digital circuits (sub-units) within the processor produces the manipulated data expected by a software instruction (loaded earlier, likely from memory). It controls (conducts) data flow inside the processor and additionally provides several external control signals to the rest of the computer to further direct data and instructions to/from processor external destinations (i.e. memory).

The Control Unit (CU) is generally a sizable collection of complex digital circuitry interconnecting and directing the many execution units (i.e. ALU, data buffers, registers) contained within a CPU. The CU is normally the first CPU unit to accept from an externally stored computer program a single instruction (based on the CPU's instruction set). The CU then decodes this individual instruction into several sequential steps (fetching addresses/data from registers/memory, managing execution ([i.e. data sent to the ALU or I/O]), and storing the resulting data back into registers/memory) that controls and coordinates the CPU's inner works to properly manipulate the data. The design of these sequential steps is based on the needs of each instruction and can range in number of steps, the order of execution, and which units are enabled.

Thus by only using a program of set instructions in memory, the CU will configure all the CPU's data flows as needed to manipulate the data correctly between instructions. This result in a computer that could run a complete program and require no human intervention to make hardware changes between instructions (as had to be done when using only punch cards for computations before stored programmed computers with CUs were invented). These detailed steps from the CU dictate which of the CPU's interconnecting hardware control signals to enable/disable or which CPU units are selected/de-selected and the unit's proper order of execution as required by the instruction's operation to produce the desired manipulated data. Additionally, the CU's orderly hardware coordination properly sequences these control signals, then configures the many hardware units comprising the CPU, directing how data should also be moved, changed, and stored outside the CPU (i.e. memory) according to the instruction's objective.

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***Input and Output Mechanism***

The process of giving input to computer and giving output from computer is called input/ output. The mechanism almost same for input and output. The operating system is mainly responsible for input output operating interrupt and error handling is important terms related to input/outputs.

I/O devices are divided into two categories:-

1. **Block devices**: -

A block devices is one that store information in fixed-sized blocks, each one, with its own address common blocked size ranges from 512 bytes to 32768 bytes. The essential property of a block device is that it is possible to read or write each block independently of all the other ones. In other word, at any instant, the program can read or write any of the blocks. The common examples of block device are disk. A disk is block addressable device because no matter where the arm currently is, it is always possible to seek to another cylinder and then wait for another block to rotate the head.

1. **Character devices**: -

  A character device is one that delivers or accepts a stream of characters, without regards to any blocks structure. It is not accessible and does not have any such operation. The examples of character devices are printers, paper tapes, network interface card, mice and most other devices that are not disk like can be seen as.

***Device controller***

I/O units typically consist of mechanical part and the electronic part. The electronic part is also called the device controller or adapter. On pc, device controller takes the form of printed circuit card that can be inserted into an expansion slots. The controller card actually has a connected on it, into which a cable leading to the device itself can be plugged many controllers can handle more than one identical devices. The standard for interface between controller and device are ANSI, ICE, IDE, SCSI, ISO etc.

The interface between the controller and device is often a very low level interface. The controller job is to convert the serial bit stream into a block of bytes and perform any error. Correction if necessary the block of bytes is typically first assembled, bit by bit in a buffer inside the controller. After its checksum has been verified and block declared to be error free, it can then be copied to main memory.

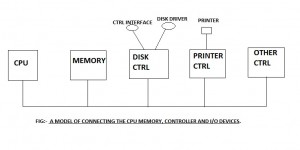
Each controller has some registers for communicating with CPU and many devices have data buffer, which the CPU can read and write data. The issues that arise of how the CPU communicates with the controller registers and the device data buffer has two alternatives.

**I/o mupped I/o:-**

  In this approach, each control register is assign an i/o port number and 8 bits or 16 bits integer. The scheme uses I/O instruction for I/O such as in OUT PORT, REG (CPU register).

**Memory mupped I/O:**-

In this approach, all the control register are mapped into the memory space. Each control register is assigned a unique memory address to which no memory is assigned. Usually, the assigned address is at the top of the address space. In this approach memory instruction like mov, stor, load are used.



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**FAST BATTERY CHARGE**

A ‘Fast Charge Battery’ feature because it is a world where you cannot be lagging behind. Powered by a long-lasting 3 cell 41WHr Li-ion fast charge battery. It recharges the battery up to 50% within 45 minutes (when the system is off) so that the entertainment doesn’t end.

#### NVIDIA GEFORCE MX110 DEDICATED GRAPHICS

Nvidia GeForce MX110 with 2GB Dedicated GDDR5 Graphic

Experience amazing dedicated GDDR5 graphics performance with NVIDIA GeForce MX110. Tap into the powerful NVIDIA Maxwell architecture for fast, smooth HD photo and video editing, plus better gaming.

#### SEAMLESS WIRELESS CONNECTIVITY

Enjoy improved connectivity with faster throughput thanks to Wi-Fi supporting gigabit speeds, with 1x1 antenna and Intel Wireless-AC 802.11 bgn Wi-Fi and Bluetooth 4.2 Combo.

#### THE SPEED YOU NEED

This laptop comes loaded 8th Gen Intel Core i5-8250U Processor, 8GB DDR4-2400 RAM and Nvidia GeForce MX110 2GB dedicated GDDR5 Graphics so that it doesn’t stop you from going forward.

***Additional Features of Lenovo IP 330***

#### Accidental Hinge Damage Prevention

An extra flexible 180-degree hinge allows greater maneuverability while reducing accidental excessive strain on the hinge, and thus prevents damage to display.

#### Faster Wi-Fi and Futuristic Ports

The 1x1 AC Wi-Fi helps you enjoy your data connection at 2 times the speed for better experience. The versatile USB Type-C is a reversible connecting port that helps connect to future-ready devices

#### Powerful Productivity

Idea pad 330 is equipped to meet your evolving needs. Cutting edge processing with Intel Core I5-8250U processor and AMD RADEON 530 (2GB GDDR5) graphics.

#### Stylish, Durable Design

A laptop isn’t just a piece of electronics - it’s also an investment. That’s why we designed the Ideapad 330 with a special protective PC ABS painting finish, to guard against wear and tear, as well as rubber detailing on the bottom to maximize ventilation and extend component life.

***Conclusion***

This has been a necessarily brief introduction to x64 assembly programming. The next step is to browse the [Intel® 64 and IA-32 Architectures Software Developer‟s Manuals.](http://developer.intel.com/products/processor/manuals/index.htm) Volume 1 contains the architecture details and is a good start if you know assembly. Other places are assembly books or online assembly tutorials. To get an understanding of how your code executes, it is instructive to step through code in debugger, looking at the disassembly, until you can read assembly code as well as your favorite language. For C/C++ compilers, debug builds are much easier to read than release builds so be sure to start there. Finally, read [the forums at](http://www.masm32.com/board/index.php) [masm32.com](http://www.masm32.com/board/index.php) for a lot of material.

***References***

“AMD64 Architecture Tech Docs,” available online at <http://www.amd.com/us-en/Processors/DevelopWithAMD/0,,30_2252_875_7044,00.html>

“Intel® 64 and IA-32 Architectures Software Developer's Manuals,” available online at <http://www.intel.com/products/processor/manuals/>