**MSPM’S**

**Deogiri Institute of Engineering and Management Studies, Aurangabad**

**Department of Computer Science and Engineering**

Report on

**lenovo G580 (59-323565) laptop**

Subject: **Computer Architecture and Organisation**

Submitted By

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# **SE-II (26135)**

Under the Guidance of

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**Device name: lenovo G580 (59-323565)**



## **SPECIFICATIONS:**

**BASIC INFORMATION**

Model name: Lenovo G580 (59-323565)

Launch date: 22 Nov 2012

Operating system: DOS

**Processor:**

Processor Brand: Intel

Processor Type: Core i3-3110

Processor Speed: 2.4 GHz

Graphics Coprocessor: Intel HD Graphics 4000

**Connectivity:**

Wireless LAN: 802.11 b/g/n

Bluetooth: Yes

**Memory:**

Ram Size: 2 GB

Memory Technology: SO-DIMM

Type and speed: DDR3-1333 or DDR3-1600

Maximum supported capacity: 16 GB

**Form Factor:**

weight: Appr. 2.5 kg

Dimension: 33.9 x 23 x 3.4 cm

Colour: Dark Brown Metal

**Storage:**

Hard Drive Size: 500 GB

Hard Disk Technology: Serial ATA

Optical Drive Type: DVD Writer

**Display:**

Maximum Display Resolution: 1366 x 768

**Battery Pack:**

Battery type: Lithium-ion

Cells/Capacity: 6 cell, 4400 mAh

**Warranty:**

Warranty time: 1 year

**Inputs:**

Web camera: Yes

Pointer device: Touchpad

Keyboard: Accu Type

Internal mic: Yes

Speakers: Yes

Touchscreen: No

**I/O Ports:**

USB ports: 2x USB 2.0,

1x USB 3.0

Video/Audio: HDMI x 1

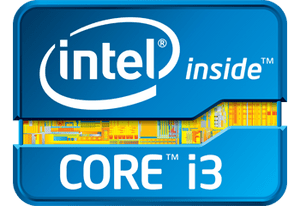
Ethernet: 10/100 Mbps or 10/100/1000 Mbps

Video: VGA x 1

Card reader: 2 in 1 slot x 1(SD/MMC)

Nobel lock security: Yes

**Processor Architecture:**



Intel Core i3-3110M is a low mid-range processor announced in Q1 of 2012. It is part of the “Ivy Bridge” generation and operates at a base frequency of 2.4GHz. Unlike its “bigger brethren” of the Core i5 and Core i7 families,  i3-3110M does not sport the TurboBoost functionality, prohibiting it from overclocking its cores during periods of higher loads.

The chip is equipped with 128KB of first level cache, 512KB of second level cache, and 3MB of third level cache. The Core i3-3110M has been developed using a 22nm process, allowing for the integration of the Intel HD Graphics 4000 controller. It operates at a base frequency of 650MHz, while Turbo Boost can increase that to 1000MHz. Power consumption of the whole system on a chip is 35 watts, with a maximum operating temperature of 90C. The processor also comes in a BGA variation, allowing it to be soldered onto motherboards. That version can withstand a temperature of 105C.

Intel Core i3-3110M supports HyperThreading (additional virtual core for every physical one), PCI Express 2.0, up to 32GB of DDR3L/-RS 1333/1600 memory and the SSE4 instruction set.

**Instruction set:**

SSE4 was formally announced on September 27th, 2006, and became available in hardware in early 2007 for both Intel and AMD processor. Earlier hints were available, but were incomplete(old version of this page were based on such reports). SSE4 now comes in 3 flavors: SSE4.1, SSE4.2, and SSE4a. All together, there are 54 instructions, 47 of which belong to SSE4.1, the remaining 7 belonging SSE4.2. SSE4a is from AMD(who didn’t support all the SSE4 instructions), and adds 6 instructions for bit manipulation.

**SSE4 – The Instructions:**

**SSE4** (**Streaming SIMD Extensions 4**) is a [SIMD](https://en.wikipedia.org/wiki/SIMD) CPU [instruction set](https://en.wikipedia.org/wiki/Instruction_set) used in the [Intel](https://en.wikipedia.org/wiki/Intel) [Core microarchitecture](https://en.wikipedia.org/wiki/Core_(microarchitecture)) and [AMD K10 (K8L)](https://en.wikipedia.org/wiki/AMD_K10). It was announced on September 27, 2006, at the Fall 2006 [Intel Developer Forum](https://en.wikipedia.org/wiki/Intel_Developer_Forum), with vague details in a [white paper](https://en.wikipedia.org/wiki/White_paper);[[1]](https://en.wikipedia.org/wiki/SSE4#cite_note-1) more precise details of 47 instructions became available at the Spring 2007 Intel Developer Forum in [Beijing](https://en.wikipedia.org/wiki/Beijing), in the presentation.[[2]](https://en.wikipedia.org/wiki/SSE4#cite_note-2) SSE4 is fully compatible with software written for previous generations of Intel 64 and IA-32 architecture microprocessors. All existing software continues to run correctly without modification on microprocessors that incorporate SSE4, as well as in the presence of existing and new applications that incorporate SSE4

**SSE4.1:**

|  |  |
| --- | --- |
| **Instruction** | **Description** |
| MPSADBW | Compute eight offset sums of absolute differences, four at a time (i.e., |x0−y0|+|x1−y1|+|x2−y2|+|x3−y3|, |x0−y1|+|x1−y2|+|x2−y3|+|x3−y4|, ..., |x0−y7|+|x1−y8|+|x2−y9|+|x3−y10|); this operation is important for some [HD](https://en.wikipedia.org/wiki/High-definition_video) [codecs](https://en.wikipedia.org/wiki/Codec), and allows an 8×8 block difference to be computed in fewer than seven cycles.[[9]](https://en.wikipedia.org/wiki/SSE4#cite_note-9) One bit of a three-bit immediate operand indicates whether y0 .. y10 or y4 .. y14 should be used from the destination operand, the other two whether x0..x3, x4..x7, x8..x11 or x12..x15 should be used from the source. |
| PHMINPOSUW | Sets the bottom unsigned 16-bit word of the destination to the smallest unsigned 16-bit word in the source, and the next-from-bottom to the index of that word in the source. |
| PMULDQ | Packed signed multiplication on two sets of two out of four packed integers, the 1st and 3rd per packed 4, giving two packed 64-bit results. |
| PMULLD | Packed signed multiplication, four packed sets of 32-bit integers multiplied to give 4 packed 32-bit results. |
| DPPS, DPPD | [Dot product](https://en.wikipedia.org/wiki/Dot_product_instruction) for AOS (Array of Structs) data. This takes an immediate operand consisting of four (or two for DPPD) bits to select which of the entries in the input to multiply and accumulate, and another four (or two for DPPD) to select whether to put 0 or the dot-product in the appropriate field of the output. |
| BLENDPS, BLENDPD, BLENDVPS,  BLENDVPD, PBLENDVB, PBLENDW | Conditional copying of elements in one location with another, based (for non-V form) on the bits in an immediate operand, and (for V form) on the bits in register XMM0. |
| PMINSB, PMAXSB, PMINUW, PMAXUW PMINUD, PMAXUD,  PMINSD, PMAXSD | Packed minimum/maximum for different integer operand types |
| ROUNDPS, ROUNDSS, ROUNDPD, ROUNDSD | Round values in a floating-point register to integers, using one of four rounding modes specified by an immediate operand |
| INSERTPS, PINSRB, PINSRD/PINSRQ,  EXTRACTPS, PEXTRB, PEXTRD/PEXTRQ | The INSERTPS and PINSR instructions read 8, 16 or 32 bits from an x86 register or memory location and inserts it into a field in the destination register given by an immediate operand. EXTRACTPS and PEXTR read a field from the source register and insert it into an x86 register or memory location. For example, PEXTRD eax, [xmm0], 1; EXTRACTPS [addr+4\*eax], xmm1, 1 stores the first field of xmm1 in the address given by the first field of xmm0. |
| PMOVSXBW, PMOVZXBW, PMOVSXBD,  PMOVZXBD, PMOVSXBQ, PMOVZXBQ,  PMOVSXWD, PMOVZXWD, PMOVSXWQ,  PMOVZXWQ, PMOVSXDQ, PMOVZXDQ | Packed sign/zero extension to wider types |
| PTEST | This is similar to the TEST instruction, in that it sets the [Z flag](https://en.wikipedia.org/wiki/Zero_flag) to the result of an AND between its operands: ZF is set, if DEST AND SRC is equal to 0. Additionally it sets the C flag if (NOT DEST) AND SRC equals zero.  This is equivalent to setting the Z flag if none of the bits masked by SRC are set, and the C flag if all of the bits masked by SRC are set. |
| PCMPEQQ | Quadword (64 bits) compare for equality |
| PACKUSDW | Convert signed DWORDs into unsigned WORDs with saturation. |
| MOVNTDQA | Efficient read from write-combining memory area into SSE register; this is useful for retrieving results from peripherals attached to the memory bus. |

### **SSE4.2:**

|  |  |
| --- | --- |
| **Instruction** | **Description** |
| CRC32 | Accumulate [CRC32](https://en.wikipedia.org/wiki/CRC32)C value using the polynomial 0x11EDC6F41 (or, without the high order bit, 0x1EDC6F41). |
| PCMPESTRI | Packed Compare Explicit Length Strings, Return Index |
| PCMPESTRM | Packed Compare Explicit Length Strings, Return Mask |

|  |  |
| --- | --- |
| PCMPISTRI | Packed Compare Implicit Length Strings, Return Index |
| PCMPISTRM | Packed Compare Implicit Length Strings, Return Mask |
| PCMPGTQ | Compare Packed Signed 64-bit data For Greater Than |

### POPCNT and LZCNT:

These instructions operate on integer rather than SSE registers, because they are not SIMD instructions, but appear at the same time and although introduced by AMD with the SSE4a instruction set, they are counted as separate extensions with their own dedicated CPUID bits to indicate support. Intel implements POPCNT beginning with the [Nehalem](https://en.wikipedia.org/wiki/Nehalem_%28microarchitecture%29) microarchitecture and LZCNT beginning with the [Haswell](https://en.wikipedia.org/wiki/Haswell_%28microarchitecture%29) microarchitecture. AMD implements both beginning with the [Barcelona microarchitecture](https://en.wikipedia.org/wiki/AMD_K10#Characteristics_of_the_microarchitecture).

|  |  |
| --- | --- |
| **Instruction** | **Description** |
| POPCNT | [Population count](https://en.wikipedia.org/wiki/Hamming_weight) (count number of bits set to 1). Support is indicated via the CPUID.01H:ECX.POPCNT[Bit 23] flag. |
| LZCNT | [Leading zero count](https://en.wikipedia.org/wiki/Leading_zero_count). Support is indicated via the CPUID.80000001H:ECX.ABM[Bit 5] flag. |

The encoding of *lzcnt* is similar enough to *bsr* (bit scan reverse) that if *lzcnt* is performed on a CPU not supporting it such as Intel CPU's prior to Haswell, it will perform the *bsr* operation instead of raising an invalid instruction error despite the different result values of *lzcnt* and *bsr*.

Trailing zeros can be counted using the *bsf* (bit scan forward) or *tzcnt* instructions.

### **SSE4a:**

The SSE4a instruction group was introduced in AMD's [Barcelona microarchitecture](https://en.wikipedia.org/wiki/AMD_K10#Characteristics_of_the_microarchitecture). These instructions are not available in Intel processors. Support is indicated via the CPUID.80000001H:ECX.SSE4A[Bit 6] flag.

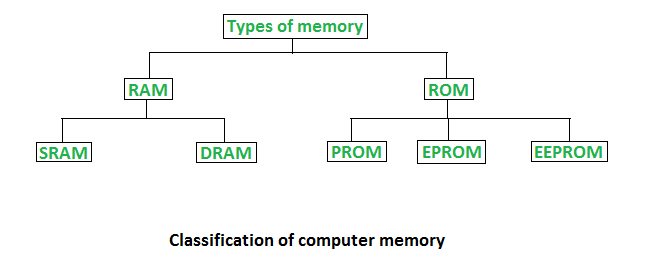
|  |  |
| --- | --- |
| **Instruction** | **Description** |
| EXTRQ/INSERTQ | Combined mask-shift instructions. |
| MOVNTSD/MOVNTSS | Scalar streaming store instructions. |

## Supporting CPUs:

* [Intel](https://en.wikipedia.org/wiki/Intel_Corporation)
  + [Silvermont](https://en.wikipedia.org/wiki/Silvermont_%28microarchitecture%29) processors (SSE4.1, SSE4.2 and POPCNT supported)
  + [Goldmont](https://en.wikipedia.org/wiki/Goldmont) processors (SSE4.1, SSE4.2 and POPCNT supported)
  + [Goldmont Plus](https://en.wikipedia.org/wiki/Goldmont_Plus) processors (SSE4.1, SSE4.2 and POPCNT supported)
  + [Tremont](https://en.wikipedia.org/w/index.php?title=Tremont_%28microarchitecture%29&action=edit&redlink=1) processors (SSE4.1, SSE4.2 and POPCNT supported)
  + [Penryn](https://en.wikipedia.org/wiki/Penryn_%28microarchitecture%29) processors (SSE4.1 supported)
  + [Nehalem](https://en.wikipedia.org/wiki/Nehalem_%28microarchitecture%29) processors and newer (SSE4.1, SSE4.2 and POPCNT supported)
  + [Haswell](https://en.wikipedia.org/wiki/Haswell_%28microarchitecture%29) processors and newer (SSE4.1, SSE4.2, POPCNT and LZCNT supported)

**Memory:**

Memory is the most essential element of a computing system because without it computer can’t perform simple tasks. Computer memory is of two basic type – Primary memory / Volatile memory and Secondary memory / non-volatile memory. Random Access Memory (RAM) is volatile memory and Read Only Memory (ROM) is non-volatile memory.



**1. Random Access Memory (RAM) –**

* It is also called as *read write memory* or the*main memory* or the *primary memory*.
* The programs and data that the CPU requires during execution of a program are stored in this memory.
* It is a volatile memory as the data loses when the power is turned off.
* RAM is further classified into two types- *SRAM (Static Random Access Memory)* and *DRAM (Dynamic Random Access Memory)*.

**2. Read Only Memory (ROM) –**

* Stores crucial information essential to operate the system, like the program essential to boot the computer.
* It is not volatile.
* Always retains its data.
* Used in embedded systems or where the programming needs no change.
* Used in calculators and peripheral devices.
* ROM is further classified into 4 types- *ROM*, *PROM*, *EPROM*, and *EEPROM*.

**Types of Read Only Memory (ROM) –**

1. **PROM (Programmable read-only memory)** – It can be programmed by user. Once programmed, the data and instructions in it cannot be changed.
2. **EPROM (Erasable Programmable read only memory)** – It can be reprogrammed. To erase data from it, expose it to ultra violet light. To reprogram it, erase all the previous data.
3. **EEPROM (Electrically erasable programmable read only memory)** – The data can be erased by applying electric field, no need of ultra violet light. We can erase only portions of the chip

**SSD (Solid-State Drive):** An SSD (solid-state drive) is a type of nonvolatile storage media that stores persistent data on solid-state flash memory. Two key components make up an SSD: a flash controller and NAND flash memory chips. The architectural configuration of the SSD controller is optimized to deliver high read and write performance for both sequential and random data requests. SSDs are sometimes referred to as flash drives or solid-state disks.

SSDs will use three main types of memory:

* 1. Single cell
  2. multi cell
  3. triple-level cells

1. Single-level cells can hold one bit of data at a time—a one or zero. Single-level cells (SLC) are the most expensive form of SSD, but it is also the fastest and most durable.
2. Multi-level cells (MLC) can hold two bits of data per cell and have a larger amount of storage space in the same amount of physical space as SLC. However, MLCs have slower write speeds.
3. Triple-level cells (TLC) can hold three bits of data in a cell. TLCs have a lower price, but slower write speeds and less durability. TLC-based SSDs deliver more flash capacity and are cheaper than an MLC or SLC.

**Control unit:** A control unit (CU) handles all processor control signals. It directs all input and output flow, fetches code for instructions from microprograms and directs other units and models by providing control and timing signals. A CU component is considered the processor brain because it issues orders to just about everything and ensures correct instruction execution.

**CU functions are as follows:**

* Controls sequential instruction execution
* Interprets instructions
* Guides data flow through different computer areas
* Regulates and controls processor timing
* Sends and receives control signals from other computer devices

**CUs are designed in two ways-**

* **Hardwired control:** Design is based on a fixed architecture. The CU is made up of flip-flops, logic gates, digital circuits and encoder and decoder circuits that are wired in a specific and fixed way. When instruction set changes are required, wiring and circuit changes must be made. This is preferred in a reduced instruction set computing (RISC) architecture, which only has a small number of instructions.
* **Microprogram control:** Microprograms are stored in a special control memory and are based on flowcharts. They are replaceable and ideal because of their simplicity.

**Input & output mechanism:**

**HDMI:** Stands for "High-Definition Multimedia Interface." HDMI is a trademark and brand name for a digital interface used to transmit audio and video data in a single cable. It is supported by modern audio/video equipment. HDMI outputs "feed" audio and video signals into the HDMI inputs of digital devices, which receive and process them. The cables are terminated with plug connectors, typically featuring 19 pins. Many A/V receivers contain digital processors that can take analog video signals, from a VHS or DVD player, and convert them to HMDI.

**USB:** USB" refers to Universal Serial Bus, which is a type of connection used to link computers to peripheral devices. USB ports are found on both the computers and the devices, and USB cables connect them to each other. USB ports function as both input and output ports. There are two types of USB ports, Type A and Type B, and information can go both directions on either one.

**USB Type A-**

The most popular type of USB standard is Type A. You will most likely to find Type-A ports in host devices like desktop computers, gaming consoles and media players.

**USB Type B-**

Type-B connectors are at the other end of a typical USB cable that plugs into a peripheral device, such as a smartphone, a printer or a hard drive.

**USB Type C-**

Type-C over other existing variants is that it allows for ‘reverse plug orientation’. It can be also be used to share data, charging device.

**Features:**

# LED-backlit LCD- A LED-backlit LCD is a [flat panel display](https://en.wikipedia.org/wiki/Flat_panel_display) that uses [LED](https://en.wikipedia.org/wiki/LED) [backlighting](https://en.wikipedia.org/wiki/Backlight) instead of the [cold cathode fluorescent](https://en.wikipedia.org/wiki/Cold_cathode#Lamps) (CCFL) backlighting. LED-backlit displays use the same [TFT LCD](https://en.wikipedia.org/wiki/TFT_LCD) ([thin-film-transistor liquid-crystal display](https://en.wikipedia.org/wiki/Thin-film-transistor_liquid-crystal_display)) technologies as CCFL-backlit displays, but offer reduced energy consumption, better contrast and brightness, greater color range (using more expensive RGB LEDs, blue LEDs with RG phosphors, or [quantum dot enhancement film](https://en.wikipedia.org/wiki/Quantum_dot_enhancement_film) (QDEF)), more rapid response to changes in scene (with dynamic backlight dimming), and [photorefractive effects](https://en.wikipedia.org/wiki/Photorefractive_effect).

Advantages:

 Wider color [gamut](https://en.wikipedia.org/wiki/Gamut) (with [RGB-LED](https://en.wikipedia.org/wiki/RGB_LED) or QDEF) and dimming range

 Very slim (some screens are less than 0.5 inches (13 mm) thin in edge-lit panels)

 Significantly lighter and cooler, as much as half the total chassis and system weight of a comparable CCFL

 Typically 20–30% lower power consumption and longer lifespan

 More reliable

Wireless interoperability:

Wireless LAN PCI Express Mini Card is designed to be interoperable with any wireless LAN product that is based on Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK), and/ or Orthogonal Frequency Division Multiplexing (OFDM) radio technology, and is compliant to:

* The IEEE 802.11a/b/g/n Standard on Wireless LANs, as defined and approved by the Institute of Electrical and Electronics Engineers.
* The Wireless Fidelity (WIFI) Certification as defined by the Wi-Fi Alliance.