Worksheet of Experiment

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Title of Experiment: Design and analysis of universal gate in switch level modelling using verilog in Cadence NCSIM.

Name of Language: Verilog.

Name of Software: Cadence NCSIM, simvision.

Theory of Experiment:

Switch level modelling:

Switch-level modeling is a technique used primarily in digital design and simulation to describe circuits at the transistor or switch level rather than at the more abstract behavioral or gate levels. In switch-level modeling, components are represented as switches, typically focusing on the behavior of MOSFETs (nMOS and pMOS transistors), which are the primary building blocks of CMOS technology.

Key Concepts of Switch-Level Modeling

1. Switch Representation: Switches can be modeled as either *open* or *closed*, depending on the control signals. In CMOS circuits, nMOS and pMOS transistors act as switches controlled by voltage levels at their gates.

2. nMOS and pMOS Transistors:

- nMOS Transistor: Conducts when the gate is at a high voltage and blocks when the gate is low.

- pMOS Transistor: Conducts when the gate is at a low voltage and blocks when the gate is high.

3. Node Voltages and Signal Flow: Switch-level models focus on node voltages and connectivity rather than currents, which makes them simpler for digital applications. Signal flow is determined by the state of the switches, allowing digital logic to be implemented by combinations of open and closed switches.

Advantages of Switch-Level Modeling

- Efficiency: Offers a low-level view of digital circuits without needing the full complexity of transistor-level modeling.

- Power Analysis: Enables simple power consumption analysis by examining the switching activities in transistors.

- Timing Simulation: Can provide approximate timing information, although it may not be as accurate as full SPICE simulations.

Applications of Switch-Level Modeling

- Digital Design Verification: Used to simulate and verify digital circuit designs by analyzing switch behavior.

- Power Estimation: Suitable for analyzing and estimating power dissipation in digital circuits.

- Design Debugging: Allows designers to observe how signals propagate through transistors in a circuit, making it useful for debugging transistor-level designs.

Program and Stimulus (Testbench) program:

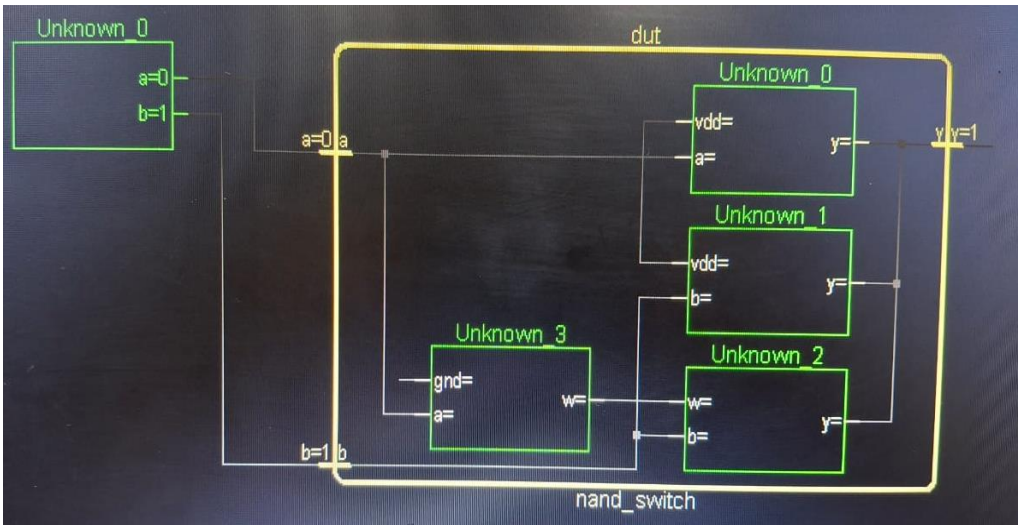
PROGRAM:

```
module nand_switch(a,b,
input a,b;
output y;
wire w;
supply1 vdd;
supply0 gnd;
pmos p1(y,vdd,a);
pmos p2(y,vdd,b);
nmos n1(y,w,b);
nmos n2(w,gnd,a);
endmodule

module nand_switchtb;
reg a,b;
wire y;
wire w;
nand_switch dut(a,b,y)
initial
begin
a=0;b=0;
#10 a=0;b=1;
#10 a=1;b=0;
#10 a=1;b=1;
#200 $stop;
end
endmodule
```

Simulation waveform:

RTL Schematic:



Learning Outcome:

1. Learn to write syntactically correct Verilog code for switch level modelling.

2. Create testbenches to simulate and verify the functionality of switch level modelling.

3. Apply techniques to optimize logic circuits for speed, area, and power efficiency.

4. Perform timing analysis to ensure circuits meet required timing constraints.

5. Analyze the performance of Counter and circuits in terms of timing, power, and area using simulation results.