

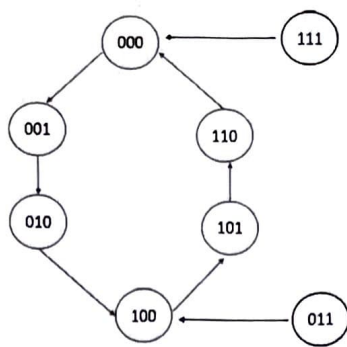
Shiv Nadar University Chennai

End Semester Examinations, 2023-2024 Odd

Question Paper

Name of the Program: Common to B.Tech. AI & DS and B.Tech. CSE (Cyber Security)			Semester: I
Course Code & Name: CS1703 Digital Design + Lab			
Regulation 2021			
Time: 3 Hours			Maximum: 100 Marks

Q.No	Questions	Marks	CO#	KL#
1	Calculate the binary equivalent of $(247.32)_{10}$.	2	CO1	KL3
2	Use the 2's complement method to subtract $(10111001)_2$ from $(11100110)_2$.	2	CO1	KL3
3	Determine the binary equivalent of the Gray code 101011.	2	CO1	KL3
4	Determine the signed 10's complement BCD representation of the decimal number -253.	2	CO1	KL3
5	Apply the properties of Boolean algebra and convert the following functions to the other canonical form: (a) $F(x, y, z) = \Sigma(1, 3, 7)$ (b) $F(a, b, c) = \Pi(0, 2, 5, 7)$	2	CO2	KL3
6	Determine the complement of the function, $F = x(y'z' + yz)$.	2	CO2	KL3
7	Discuss how a 2-bit parallel subtractor can be implemented using full adders with the logic diagram.	2	CO3	KL2
8	Explain how a priority encoder is different from a regular encoder.	2	CO3	KL2
9	Differentiate a latch from a flip-flop.	2	CO4	KL2
10	Draw the logic diagram of a JK flip-flop and state how it can be converted into a T flip-flop.	2	CO4	KL1
11	Determine the simplified form of the Boolean function, $F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10)$ along with the don't care conditions, $d(w, x, y, z) = \Sigma(5, 6, 11, 15)$ in the sum of products and the product of sum form using a K-map.	10	CO2	KL3
12	Use the Quine McCluskey method to minimize the Boolean function, $F = A'B'C'D' + AC'D' + B'CD' + A'BCD + BC'D$.	10	CO2	KL3
13	Illustrate the design of a full adder using the following: (a) only basic logic gates (b) a decoder and OR gates	10	CO3	KL4
14	Design a combinational circuit with three inputs, x, y , and z , and three outputs, A, B , and C . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.	10	CO3	KL6
15	a Show the functional table and the logic diagram of a 1x4 demultiplexer.	5	CO3	KL3

	b	Use a multiplexer to implement the function $F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$.	5	CO3	KL3																																																	
16		Illustrate the logic diagram of a mod-5 asynchronous counter. Explain its working and pictorially represent its operation with a timing diagram.	8	CO4	KL3																																																	
17		Design a Synchronous counter using JK flip-flops to count the sequence given below: 	12	CO4	KL6																																																	
18	a	Draw the logic diagram of a 4-bit parallel-in serial-out shift register and explain the working of the circuit assuming an input of 1011 is to be given to the circuit.	5	CO4	KL2																																																	
	b	Determine the reduced state table and the corresponding state diagram for the following state table: <table border="1" data-bbox="228 1010 1053 1487"><thead><tr><th rowspan="2">Present State</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr><tr><th>$x = 0$</th><th>$x = 1$</th><th>$x = 0$</th><th>$x = 1$</th></tr></thead><tbody><tr><td>a</td><td>f</td><td>b</td><td>0</td><td>0</td></tr><tr><td>b</td><td>d</td><td>c</td><td>0</td><td>0</td></tr><tr><td>c</td><td>f</td><td>e</td><td>0</td><td>0</td></tr><tr><td>d</td><td>g</td><td>a</td><td>1</td><td>0</td></tr><tr><td>e</td><td>d</td><td>c</td><td>0</td><td>0</td></tr><tr><td>f</td><td>f</td><td>b</td><td>1</td><td>1</td></tr><tr><td>g</td><td>g</td><td>h</td><td>0</td><td>1</td></tr><tr><td>h</td><td>g</td><td>a</td><td>1</td><td>0</td></tr></tbody></table>	Present State	Next State		Output		$x = 0$	$x = 1$	$x = 0$	$x = 1$	a	f	b	0	0	b	d	c	0	0	c	f	e	0	0	d	g	a	1	0	e	d	c	0	0	f	f	b	1	1	g	g	h	0	1	h	g	a	1	0	5	CO4	KL3
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