Shiv Nadar University Chennai

Mid Semester Examinations 2023-2024 Even

Question Paper

Name of the Program: Common to B.Tech. AI & DS., B.Tech. CSE (IoT) and B.Tech. CSE (CS)		Semester: II
Course Code & Name: CS1004 COMPUTER ORGANIZATION AND ARCHITECTURE		
Regulation 2021		
Time: 2 Hours	Answer All Questions	Maximum: 50 Marks

Questions		Marks	CO	KL
1	Write an assembly language program using one address instruction which can perform the operation Y= M * X + C	2	CO1	KL3
2	Find the sum of following using 2's complement: (a) 10101-00111 and (b) 0100-0111	2	CO2	KL3.
3	Let us assume 'p' bits are used for the exponent. What could be the value of bias to be added to the actual exponent in IEEE754 single precision representation. Justify the need for biasing.	2	CO2	KL2
4	What are addressing modes? Explain register indirect and indexed addressing mode.	2	CO1	KL2
5	Give any two differences between RISC and CISC ISAs.	2	CO1	KL2
6	Present the equation used by SPEC for measuring the performance of a computer. Assuming that the reference computer is ultra SPARCIO workstation with 300 MHz ultra-SPARC processor. The company has to purchase 1000 new computers and hence ordered testing of the new computer with SPEC. Following observations were made: The company system manager will place the order for purchasing new computers only if the overall SPEC rating is at least 12. After the said test, will the system manager place order for purchase of new computers?	5	CO1	KL3
7	Write the procedure for multiplying two numbers in IEE 754 format. Given two numbers 1.01101×2^3 and 1.110001×2^1. Subtract the two numbers and represent the result in IEEE754 single precision format.	5	CO2	KL3
8	Draw the basic functional diagram of a processor having memory and I/O units as peripherals connected via a system BUS. Explain in detail the step-by-step procedure followed by the processor during the execution of the following instruction: ADD R2, R1, [2000H]. Note, R1 is the general-purpose register having the first operand and 2000H is the memory address where the second operand is stored. Result should be stored in R2. Explanation should include the details about the interactions of various units inside the processor.	10	CO1	KL4

Programs	Runtime on reference computer	Runtime on new computer
1	50 minutes	5 minutes
2	75 minutes	4 minutes
3	60 minutes	6 minutes
4	30 minutes	3 minutes

9	A computer is executing a program P1. During the execution of program P1 an interrupt I1 occurred. By providing all the necessary details about the concerned processor registers and memory, explain how the computer handles the interrupt I1 without affecting the consistency of the program P1.	10	CO1	KL4
10	Explain the following terms with their relevant binary expressions in the context of an *n-bit* binary carry look-ahead adder: 1) Kill, 2) Generate, and 3) Propagate. Write the expressions for calculating C_1, C_2, C_3, and C_4 using C_{in}. Note, C_{in} is the input carry.	10	CO2	KL3

KL – Bloom's Taxonomy Levels
(KL1: Remembering, KL2: Understanding, KL3: Applying, KL4: Analyzing, KL5: Evaluating, KL6: Creating)
CO – Course Outcomes
