Title: EmPowerSoc flow for Active Power Estimation of SOC

EmPowerSoC is an open-source EDA tool for power estimation of SoC. It has been developed alongside the existing Qflow open-source tool chain which is currently being used for implementation of RTL to GDSII flow.

The development work was carried out by Mr. Akshat Jain, Mr. Nimesh Shahdadpuri and Mr. Naveen Dugar, bonafide students of B.E. (ECE) at NSUT under the guidance of Dr. Kunwar Singh, Assistant Professor, Department of ECE, Netaji Subhas University of Technology.

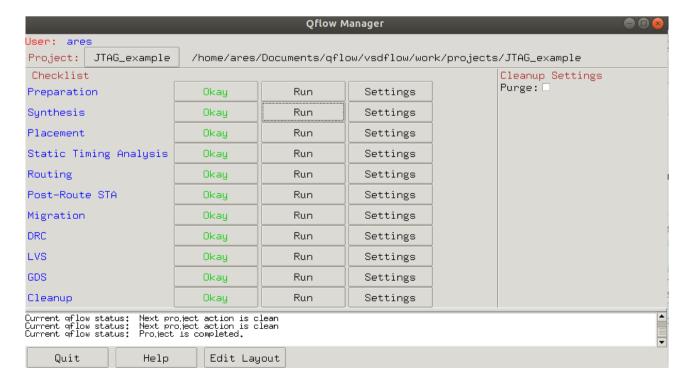
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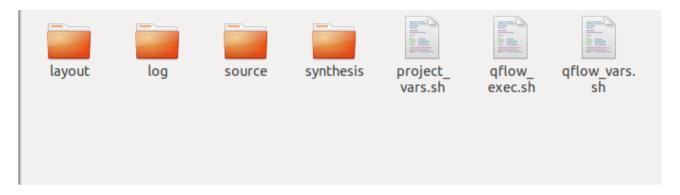
- → Download the provided example source code verilog files for Jtag.
- → Make project directory "JTAG\_Example" and "source" directory inside JTAG\_Example. Paste the JTAG verilog files inside source folder.

Use the following commands-

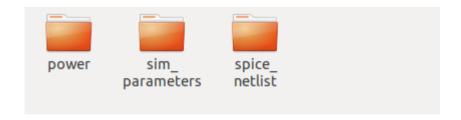
- mkdir JTAG\_Example
- cd JTAG Example
- mkdir source
- mv <source\_location> ./source/tap\_top.v
- mv <source\_location> ./source/tap\_defines.v
- → In the **JTAG\_Example** directory, open the qflow gui using terminal window and run the RTL2GDS flow by selecting required parameters.



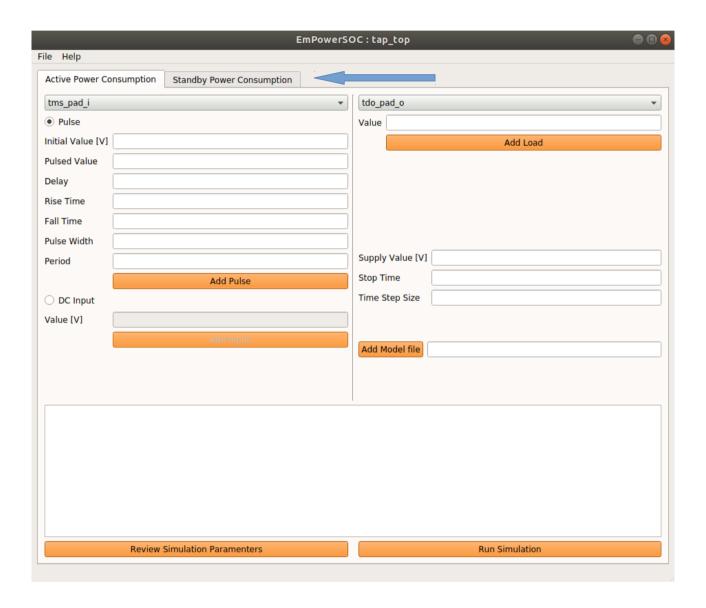
→ After completion of RTL2GDS, these below mentioned folders should be created in the project directory.



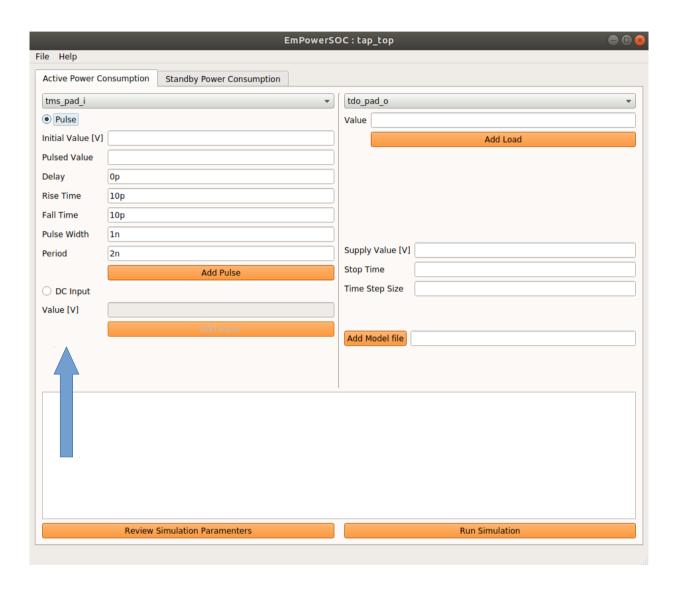
- → Now, inside the project directory Jtag\_example, right click and select open in terminal. Run the command "empower" in terminal to start EmPowerSoc.
- → EmPowerSoc directory will be created in your project directory. It will contain 3 sub directories-
  - → Power Conatins the calculated power values.
  - → Spice Netlist Contains the spice netlists for all the standard cells
  - → Sim\_Parameters Conatins the saved project simulation parameters which can be loaded directly in the future.



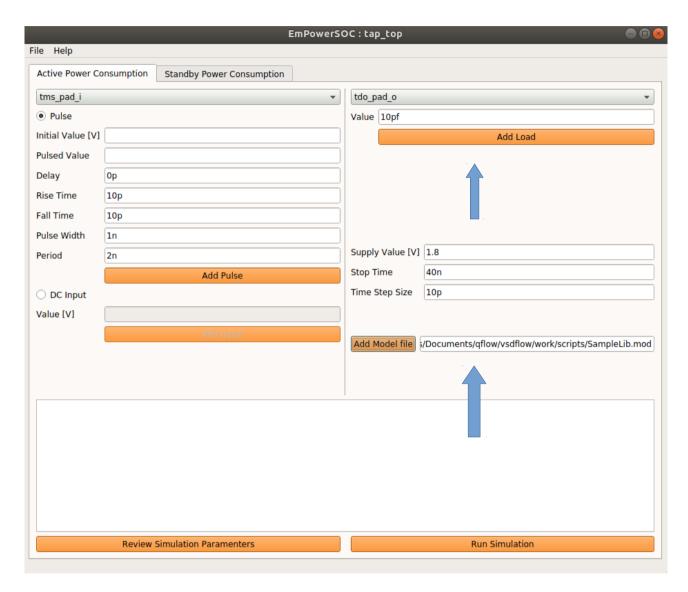
→ In the GUI, by changing tabs you can switch between Standby Power estimation and Active Power estimation.



→ Apply input pulses to all the required ports and add DC inputs wherever required.



→ Specify the load capacitances for the output nodes. And add the Supply Value, simulation time and time step for simulation.



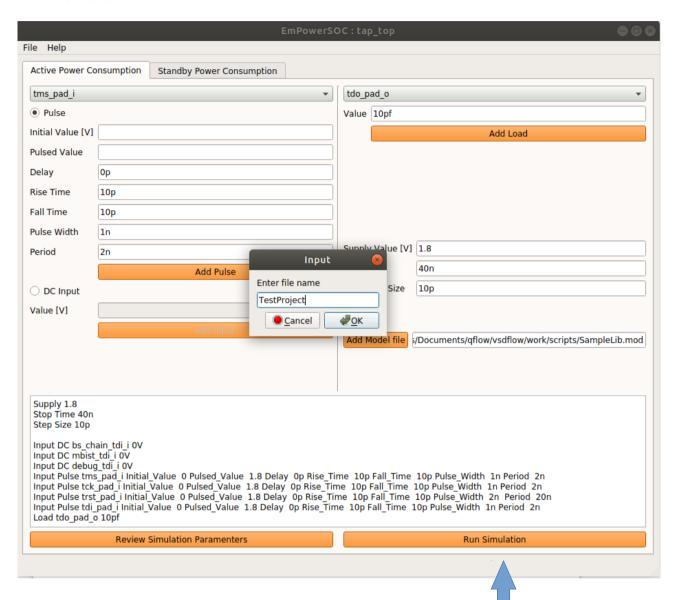
→ Add the model file for NMOS and PMOS. We have provided a sample model file for reference.

Note: If you want to use your own model parameters, kindly ensure the library name and model name are same as the one in sample model file provided.

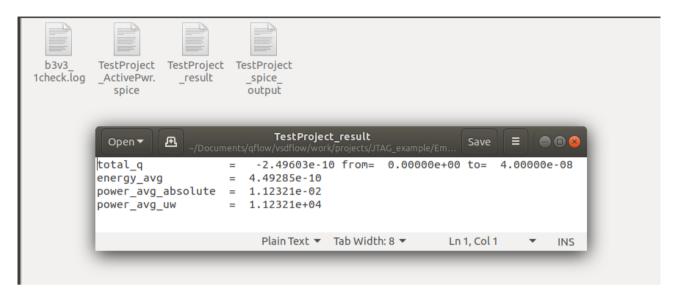
→ Review the simulation parameters. Make any changes if necessary.

	EmPowerSo	OC : tap_top	<b>⊜</b> ⊕ <b>(</b>
File Help			
Active Power Co	nsumption Standby Power Consumption		
tms_pad_i	<b>v</b>	tdo_pad_o	•
Pulse		Value 10pf	
Initial Value [V]			Add Load
Pulsed Value			
Delay	0p		
Rise Time	10p		
Fall Time	10p		
Pulse Width	1n		
Period	2n	Supply Value [V]	1.8
	Add Pulse	Stop Time	40n
O DC Input		Time Step Size	10p
Value [V]			
	Add Input	A -  -  -  -  -  -  -  -  -  -  -  -  -	(Danish of an interest of a second of a second of a second of the second
		Add Model file	s/Documents/qflow/vsdflow/work/scripts/SampleLib.mod
Supply 1.8 Stop Time 40n			
Step Size 10p			
Input DC bs_chain_tdi_i 0V			
Input DC mbist_tdi_i 0V Input DC debug_tdi_i 0V			
Input Pulse tms_pad_i Initial_Value 0 Pulsed_Value 1.8 Delay 0p Rise_Time 10p Fall_Time 10p Pulse_Width 1n Period 2n Input Pulse tck_pad_i Initial_Value 0 Pulsed_Value 1.8 Delay 0p Rise_Time 10p Fall_Time 10p Pulse_Width 1n Period 2n			
Input Pulse trst_pad_i Initial_Value_0 Pulsed_Value_1.8 Delay_0p Rise_Time_10p Fall_Time_10p Pulse_Width_2n_Period_20n Input Pulse tdi_pad_i Initial_Value_0 Pulsed_Value_1.8 Delay_0p Rise_Time_10p Fall_Time_10p Pulse_Width_1n Period_2n			
Load tdo_pad_o 10pf			
	Review Simulation Paramenters		Run Simulation

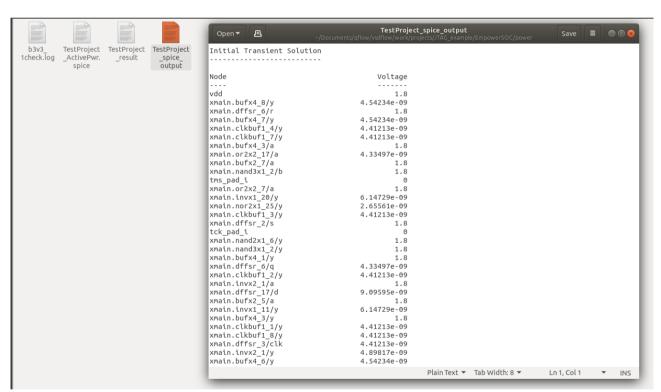
→ Finally, run the simulaton. You will be asked to provide a name for your project in order to save it.



→ The Estimated Power will be saved as a text file TestProject\_result in the EmpowerSoc>Power directory.



→ The complete ngspice output will also be saved.



→ In future, you can load these parameters directly into the tool by going into File>Open, and then selecting the simulation parameters file for that project.

