Title: EmPowerSoc flow for Active Power Estimation of SOC

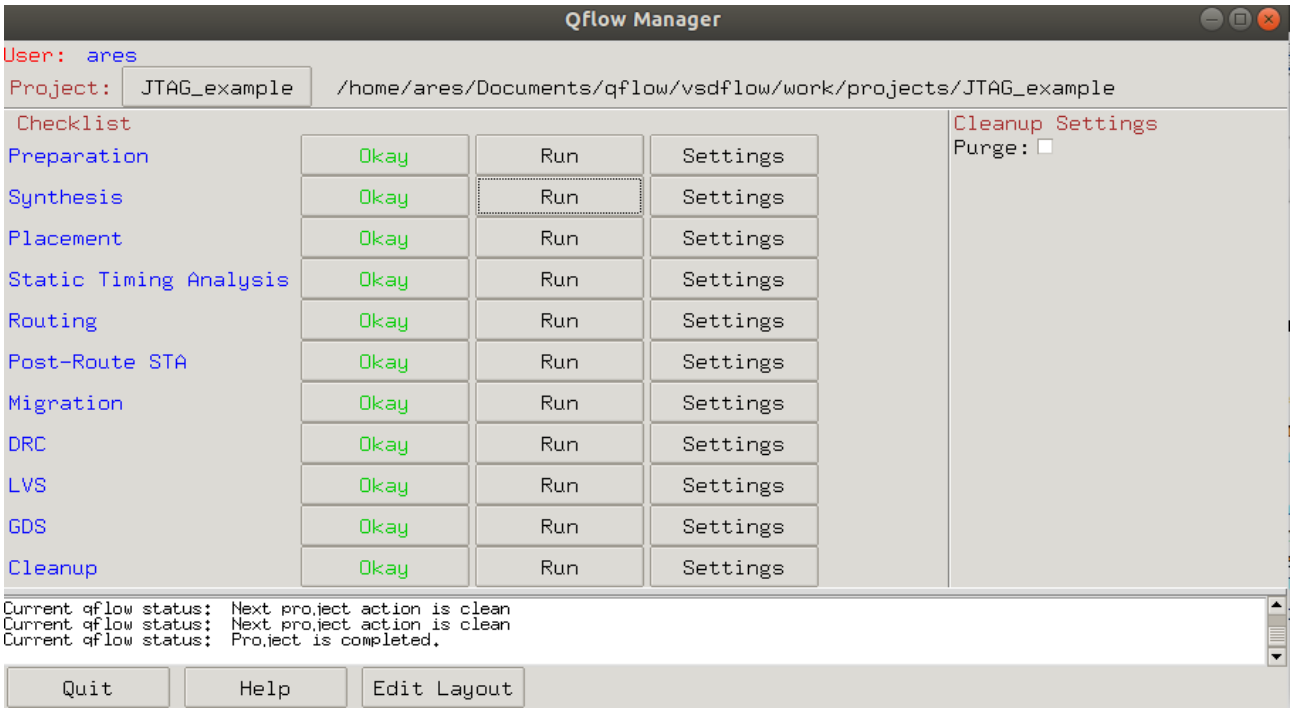
****

EmPowerSoC is an open-source EDA tool for power estimation of SoC. It has been developed alongside the existing Qflow open-source tool chain which is currently being used for implementation of RTL to GDSII flow.

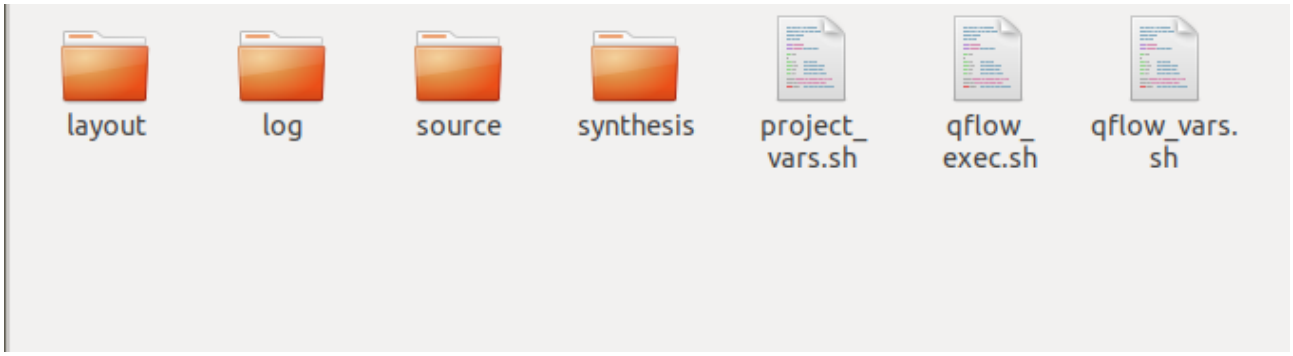
The development work was carried out by Mr. Akshat Jain, Mr. Nimesh Shahdadpuri , Mr. Sagar Yadav and Mr. Naveen Dugar, bonafide students at NSUT under the guidance of Dr. Kunwar Singh, Assistant Professor, Department of ECE, Netaji Subhas University of Technology.

****

- ➔ Download the provided example source code verilog files for Jtag.
- ➔ Make project directory **"JTAG_Example"** and **"source"** directory inside JTAG_Example. Paste the JTAG verilog files inside source folder.
  Use the following commands-
  - mkdir JTAG_Example
  - cd JTAG_Example
  - mkdir source
  - mv <source_location> ./source/tap_top.v
  - mv <source_location> ./source/tap_defines.v
- ➔ In the **JTAG_Example** directory, open the qflow gui using terminal window and run the RTL2GDS flow by selecting required parameters.



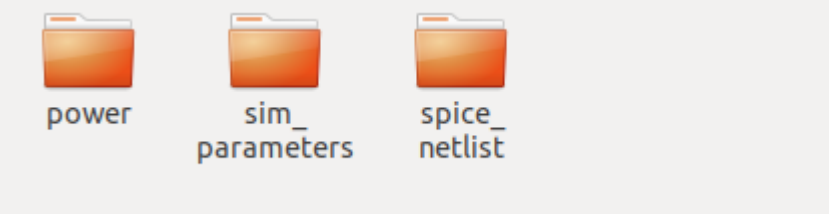
➔ After completion of RTL2GDS, these below mentioned folders should be created in the project directory.



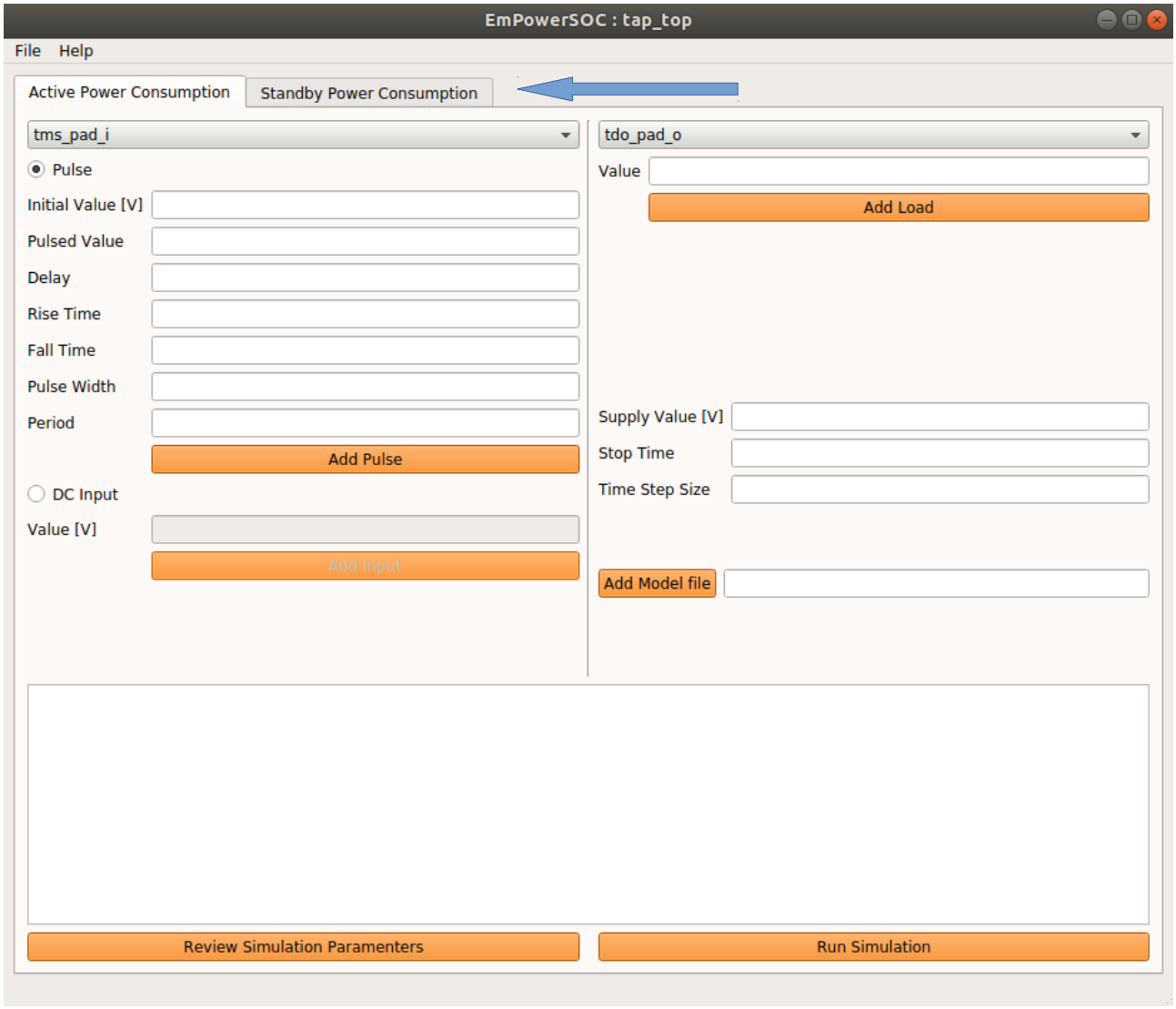
➔ Now, inside the project directory Jtag_example, right click and select open in terminal. Run the command “empower” in terminal to start EmPowerSoc.

➔ EmPowerSoc directory will be created in your project directory. It will contain 3 sub directories-

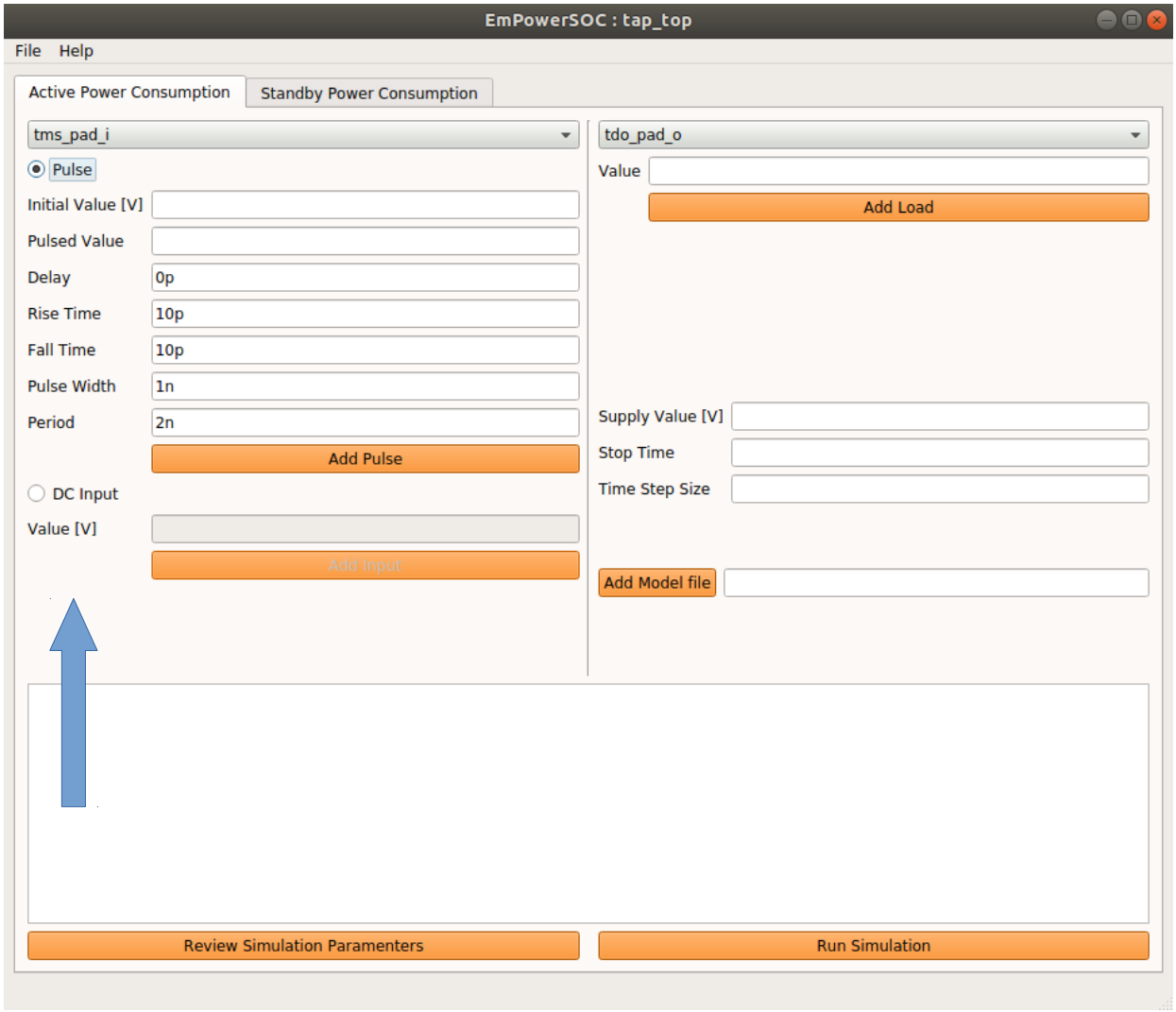
- ➔ Power – Conatins the calculated power values.
- ➔ Spice Netlist - Contains the spice netlists for all the standard cells
- ➔ Sim_Parameters – Conatins the saved project simulation parameters which can be loaded directly in the future.



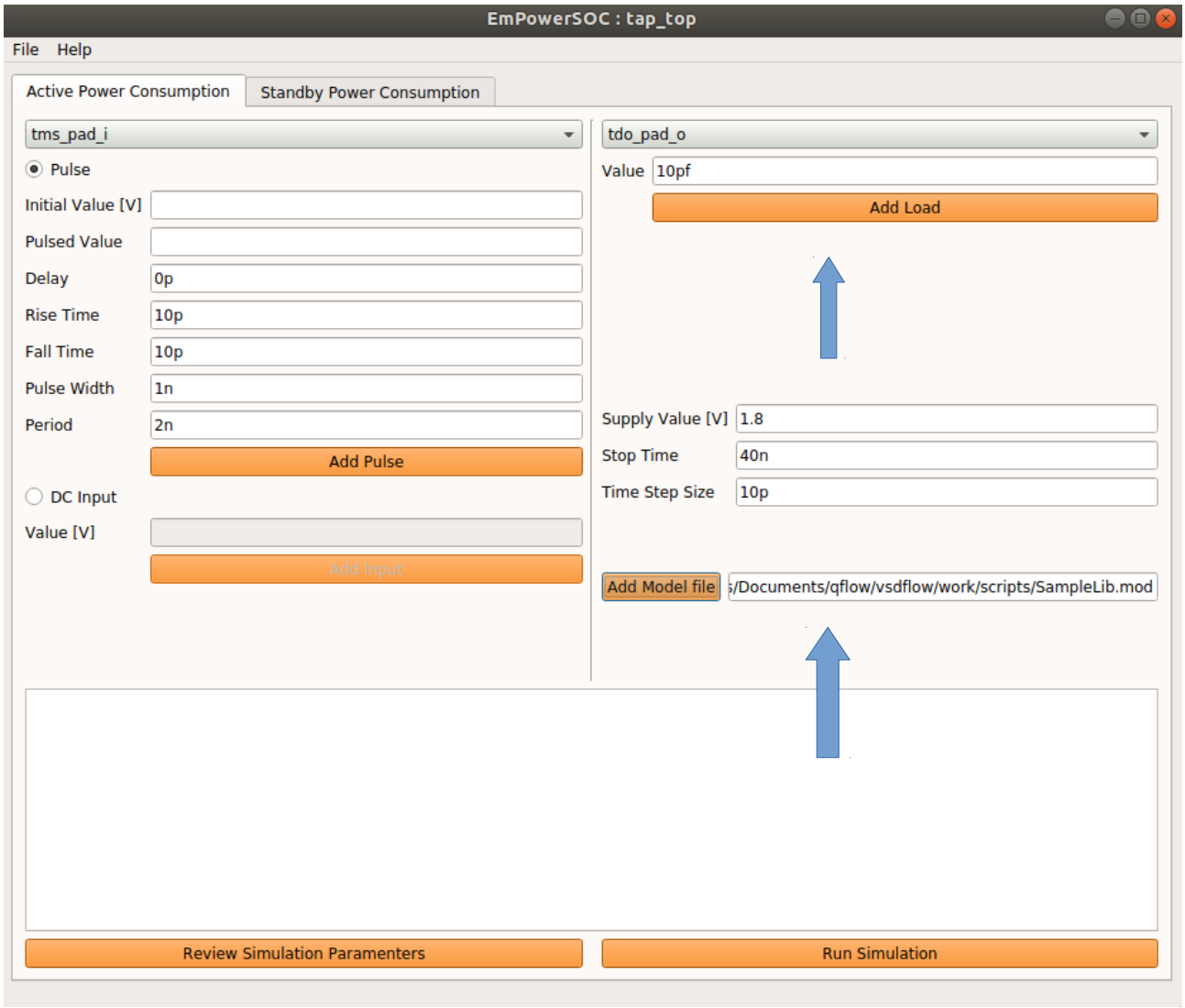
➔ In the GUI, by changing tabs you can switch between Standby Power estimation and Active Power estimation.



➔ Apply input pulses to all the required ports and add DC inputs wherever required.



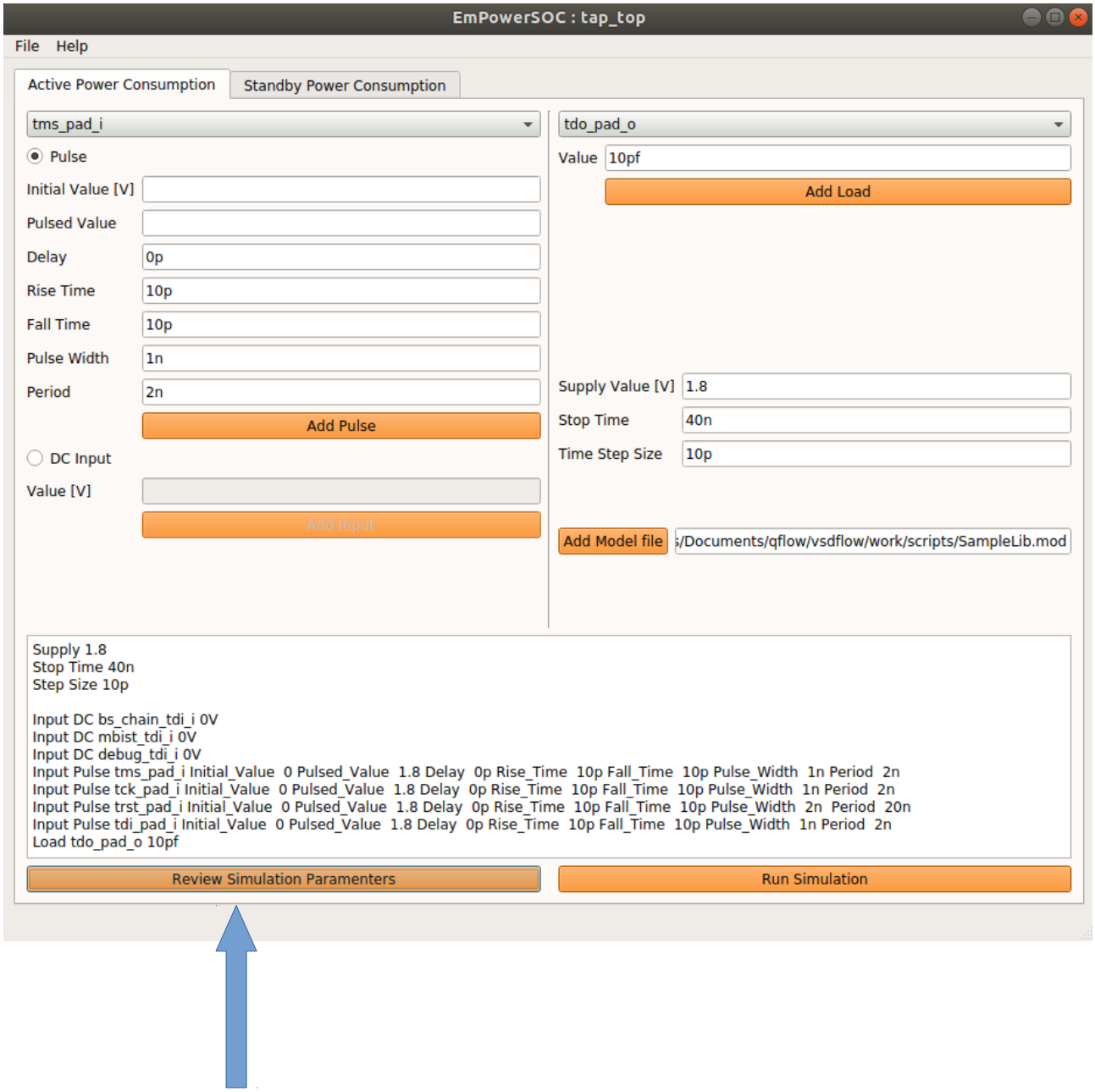
➔ Specify the load capacitances for the output nodes. And add the Supply Value, simulation time and time step for simulation.



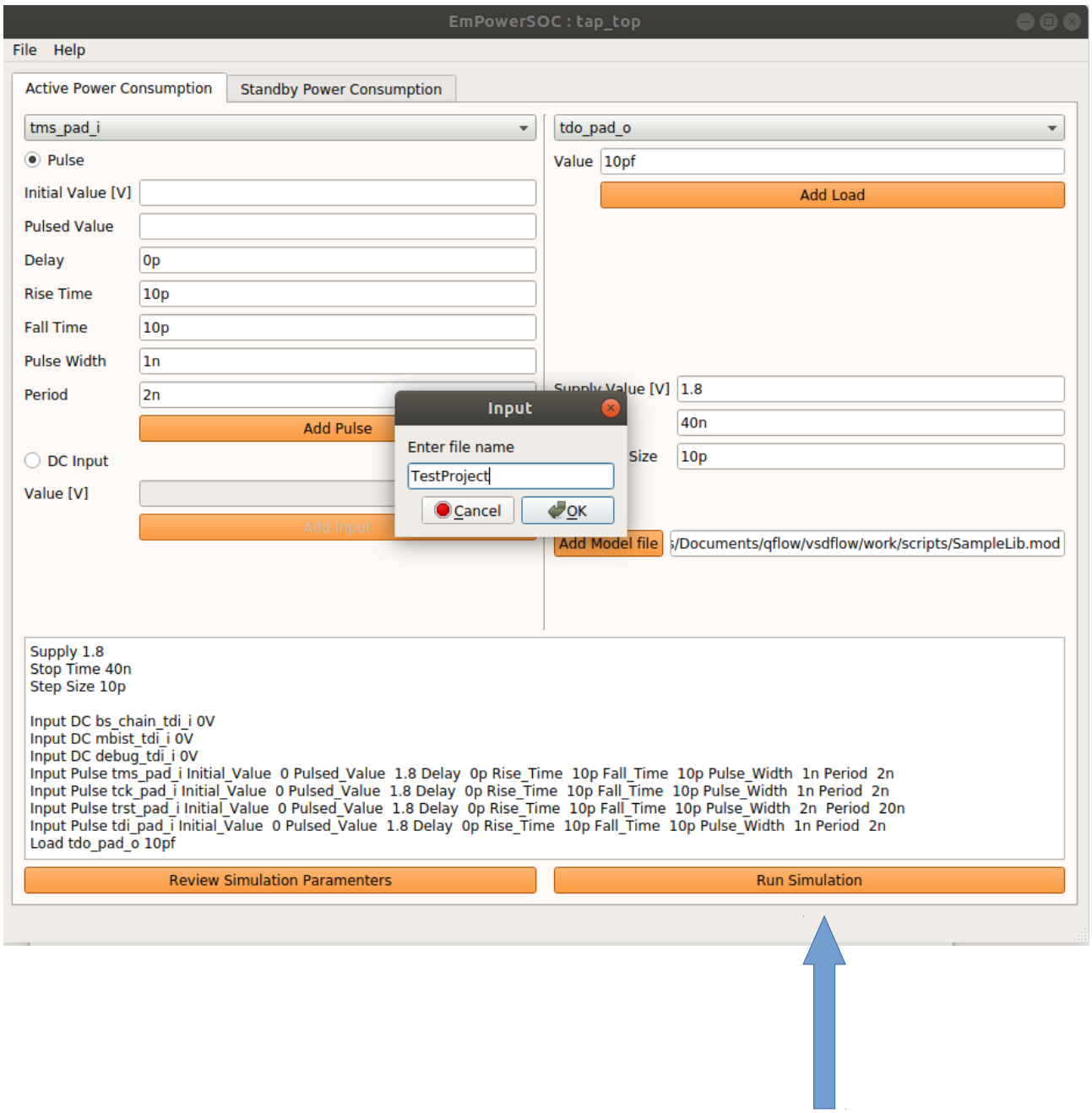
➔ Add the model file for NMOS and PMOS. We have provided a sample model file for reference.

Note: If you want to use your own model parameters, kindly ensure the library name and model name are same as the one in sample model file provided.

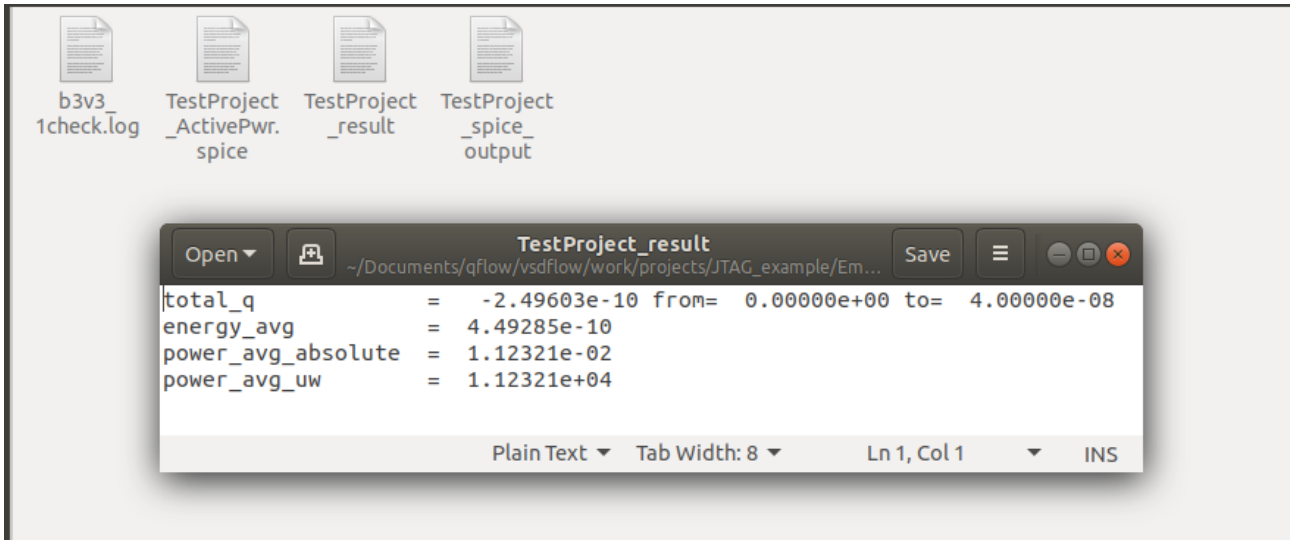
➔ Review the simulation parameters. Make any changes if necessary.



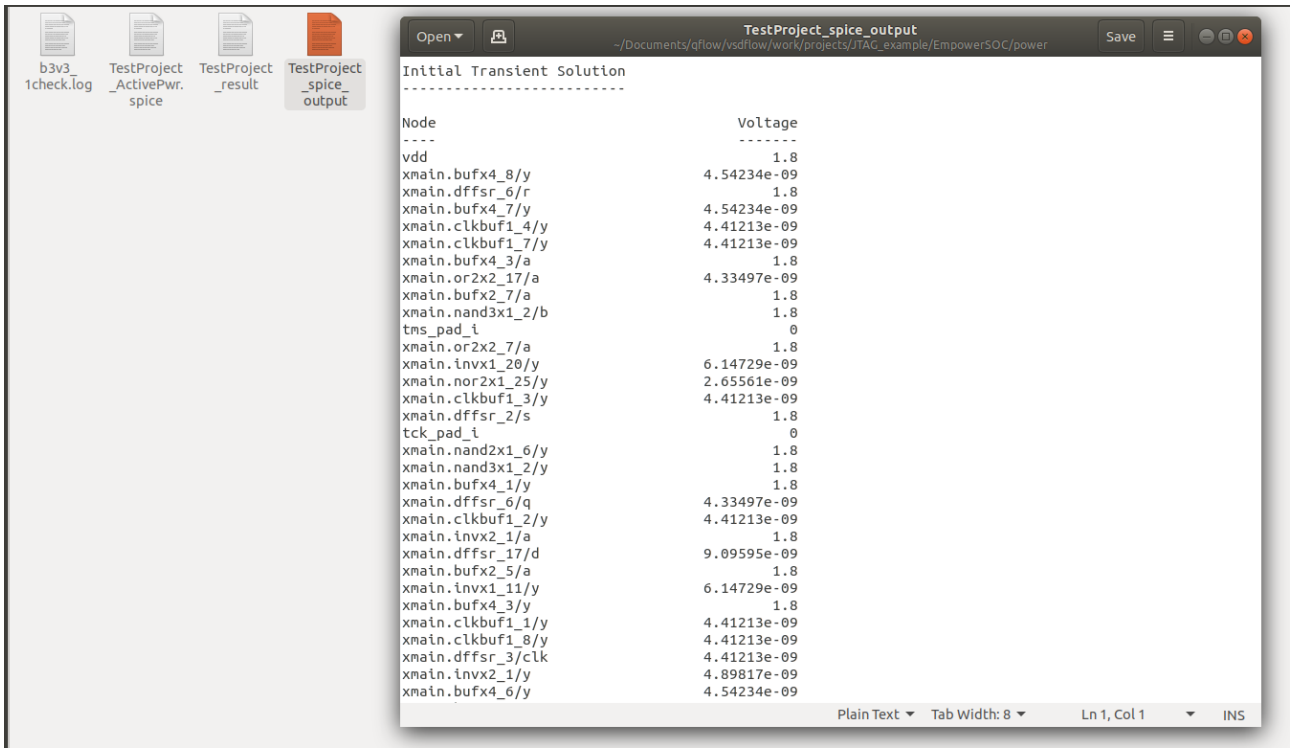
➔ Finally, run the simulaton. You will be asked to provide a name for your project in order to save it.



➔ The Estimated Power will be saved as a text file TestProject_result in the EmpowerSoc>Power directory.



➔ The complete ngspice output will also be saved.



➔ In future, you can load these parameters directly into the tool by going into File>Open, and then selecting the simulation parameters file for that project.