**Demultiplexer**

**Aim :**

**To write a program for demultiplexer using Verilog HDL and simulate the same**

**Demultiplexer**

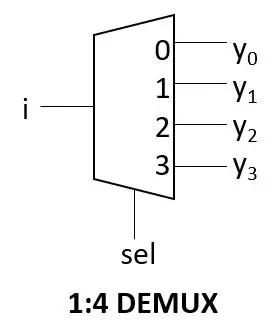
A demultiplexer (DEMUX) is a combinational circuit that works exactly opposite to a multiplexer. A DEMUX has a single input line that connects to any one of the output lines based on its control input signal (or selection lines)

Usually, for ‘n’ selection lines, there are N = 2^n output lines.

Nomenclature: 1:N denotes one input line and ‘N’ output lines.

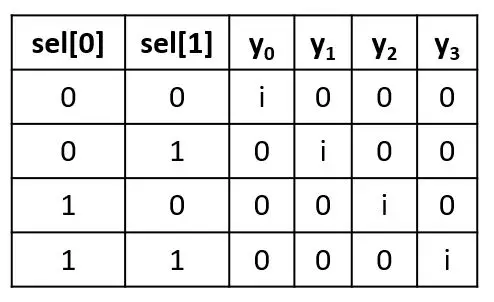
**1:4 Demultiplexer**

**1:4 DEMUX has one select line and 4 output lines**

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**Truth Table**

**1:4 demux truth table**

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**1:4 De-Mux Program**

module onetofourdmux(i,y,s);

input i;

input [1:0] s;

output reg [3:0] y;

always @(i,s)

case (s)

2'b00:

begin

y[0]=i;

y[3:1]=0;

end

2'b 01:

begin

y[0]=0;

y[1]=i;

y[3:2]=0;

end

2'b 10:

begin

y[1:0]=0;

y[2]=i;

y[3]=0;

end

2'b 11:

begin

y[2:0]=0;

y[3]=i;

end

endcase

endmodule

**Test Bench**

initial begin

i=1;

s=2'b 00;

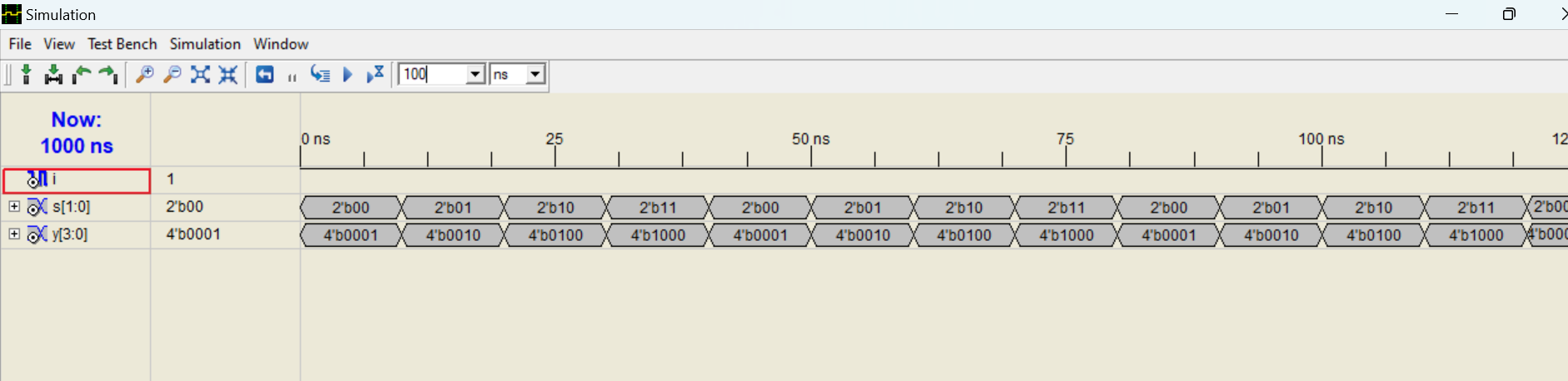
end

always # 10 s[0]= ~s[0];

always # 20 s[1]=~s[1];

endmodule

**Output**

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**Result**

Hence 1:4 Demultiplexer program is verified successfully .