# Ashish Bhaskar

ashishbhaskar<br/>11@gmail.com | 9468880077 |  $\underline{\text{LinkedIn}}$  |  $\underline{\text{Github}}$ 

# EDUCATION

# Indian Institute of Technology, Delhi

7.78/10

Bachelor of Technology in Electrical Engineering

July 2019 - 2023

#### Work Experience

#### **Software Engineer** | Samsung Research Institute, Bangalore

Aug 2023 - Present

- Took ownership of key tasks related to low-light video solution development (A55), including QC model porting, development of interface for S24 Ultra Qualcomm, and collaboration with the solutions and HAL teams
- Led end-to-end design, development, and implementation of backend solutions, ensuring seamless integration and deployment pipelines, Contributed towards ideation and A1 documentation preparation for patent filing
- Optimized low-light video enhancement for low and mid-tier phones, leveraging heterogeneous computing (GPU & CPU task offloading) and multithreading, resulting in significant performance improvements
- Collaborated with cross-functional teams to architect scalable solutions, optimize backend performance, achieving 9X reduction in frame processing time, streamlined the deployment pipeline for cutting-edge camera systems
- Created custom APIs using Android NDK tailored to various architectures, seamlessly integrating them into the camera pipeline to enhance video processing capabilities

## Internships

#### **Developer Intern** | Samsung Research Institute, Bangalore

June 2022 - Aug 2022

- Automated the debugging process by implementing a C++ program to collect and analyze the data in a single call
- Reduced overall debugging time and documented the program with comprehensive technical descriptions

#### Performance Modeling of Integrated Architecture | SNU, South Korea

May 2021 - July 2021

- Conducted performance profiling of Intel integrated CPU-GPU architecture using custom-designed OpenCL microkernels, and meticulously documented Register Allocation for Intel Processor Graphics
- Dumped and Disassembled OpenCL kernels of Intel Architecture to generate the corresponding Assembly code

#### COASTER PROJECT | Economics Department, Trinity College Dublin

March 2021 - May 2021

- Digitized and analyzed historical coastal trade data to assess Britain-Ireland macroeconomic trade relations
- Performed detailed data analysis to estimate trade volumes and trends during their economic union

# Projects

## Dynamic Memory Allocator | Prof. Rahul Garg (IIT-D)

- Developed an efficient, Java based system to allocate/free memory as per requirement using linked lists and trees
- Implemented Doubly Linked List data structure using First Split Fit algorithm to track free and allocated memory
- Implemented Best Split Fit algorithm to optimally perform allocate and free operations while minimizing memory fragmentation

## Red Lesion Segmentation for Early DR Screening | Prof. Monika Agarwal

- Developed a solution for early-stage Diabetic Retinopathy screening by detecting red lesions in 2D retinal fundus images
- Utilized machine learning and image processing techniques, incorporating handcrafted intensity-based features to minimize false negatives and improve model accuracy

#### Graph Topology Analysis | Prof. Rahul Garg | Course Project

- Implemented bi-directed graph using two csv files having data regarding storylines of characters in Marvel comics.
- Implemented DFS on the graph to generate independent storylines by utilizing Hash-Map and Array-List data structures

#### TECHNICAL EXPERTISE

Languages: C++/C, Python, Java, SQL, JavaScript, HTML, CSS, Matlab

Software, Libraries, Tools, and Frameworks: Arm Neon, OpenCL, OpenCV, Git/GitHub, VS Code, Visual Studio, MATLAB, Octave, Microsoft Office

Performance Optimization Technologies: Multithreading, Heterogenous computing