Date:16-09-2022

Assignment-6

Question 1: Write a Verilog code to design a 4:1 Multiplexer and verify the same.

Code:

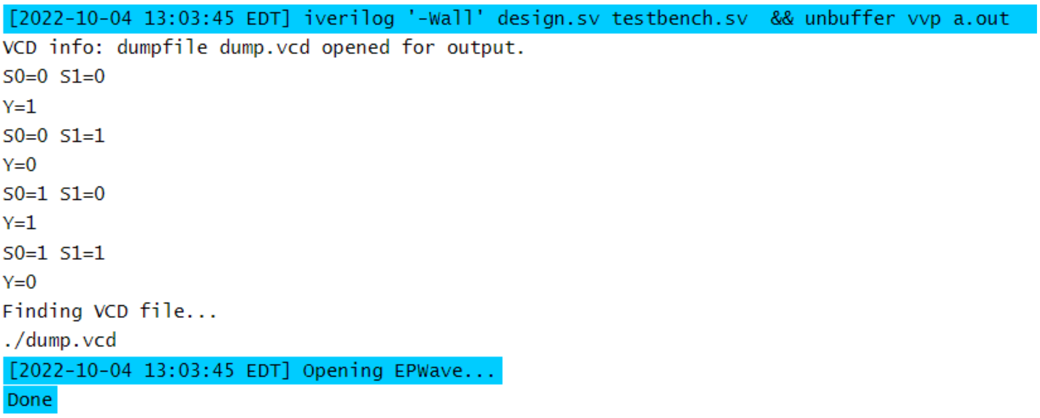
Testbench Code:

```
//21BCP322
//Akshat shah
module tb_MUX;

  reg S0,S1,I0,I1,I2,I3;
  wire Y;

  MUX M4x1(S0,S1,I0,I1,I2,I3,Y);

  initi
    al
    be
    gin
     S0=0; S1=0; I0=0 ;I1=0;I2=0;I3=1;  #1
     $display("S0=%b S1=%b",S0,S1);
     $display("Y=%b",Y);

     S0=0; S1=1; I0=1 ;I1=0;I2=1;I3=1;  #1
     $display("S0=%b S1=%b",S0,S1);
     $display("Y=%b",Y);

     S0=1; S1=0; I0=0 ;I1=0;I2=1;I3=0;  #1
     $display("S0=%b S1=%b",S0,S1);
     $display("Y=%b",Y);

     S0=1; S1=1; I0=0 ;I1=1;I2=0;I3=1;  #1
     $display("S0=%b S1=%b",S0,S1);
     $display("Y=%b",Y);
end
  init
 ial
 beg
 in
 $dumpfile("dump.vcd");
 $dumpvars(
1); end
endmodule
```

Design Code:

```
//21BCP322
module MUX(input s0,s1,I0,I1,I2,I3, output y);
  wire s0_not,s1_not,a,b,c,d;
  not(s0_not,s0);
  not(s1_not,s1);
  assign a = s0 & s1 & I0;
  assign b = s0_not & s1 &
  I1; assign c = s0 & s1_not
  & I2;
  assign d = s0_not & s1_not & I3;
  assign y = a | b | c | d;
endmodule
```

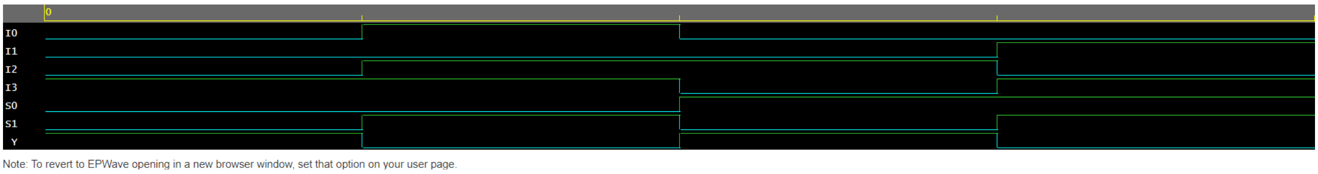
Output:



```
[2022-10-04 13:03:45 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
S0=0 S1=0
Y=1
S0=0 S1=1
Y=0
S0=1 S1=0
Y=1
S0=1 S1=1
Y=0
Finding VCD file...
./dump.vcd
[2022-10-04 13:03:45 EDT] Opening EPWave...
Done
```

Figure 1: Output of 4:1 Multiplexer

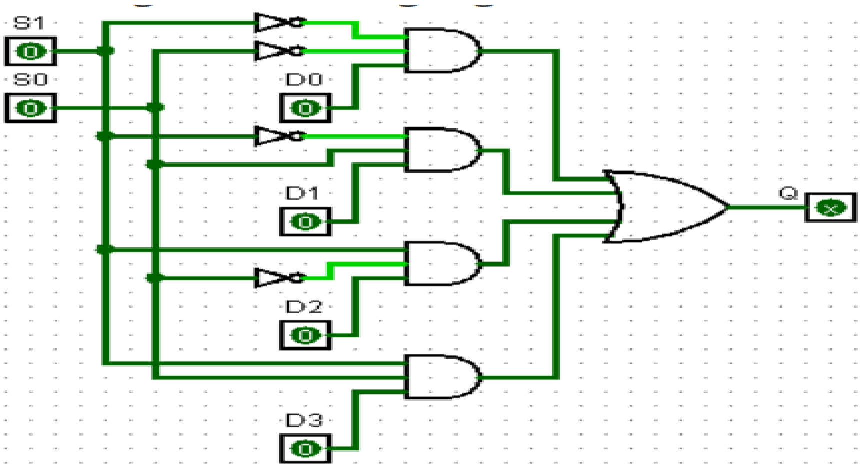
Waveform:



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Figure 2: Waveform of 4:1 Multiplexer

Circuit diagram:



Question 2: Write a Verilog code to design an 8:1 Multiplexer and verify the same.

Testbench Code:

```
//21BCP322
//Akshat shah
module tb_MUX;

  reg S0,S1,S2;
  reg I0,I1,I2,I3,I4,I5,I6,I7;
  wire Y;

  MUX M8x1(S0,S1,S2,I0,I1,I2,I3,I4,I5,I6,I7,Y);

  initial
    begin

S0=0;S1=0;S2=0;I0=0;I1=0;I2=0;I3=0;I4=0;I5=0;I6=0;I7=1; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);
S0=0;S1=0;S2=1;I0=1;I1=0;I2=0;I3=0;I4=0;I5=0;I6=1;I7=0; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);


S0=0;S1=1;S2=0;I0=0;I1=0;I2=0;I3=0;I4=0;I5=1;I6=0;I7=0; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);


S0=0;S1=1;S2=1;I0=0;I1=0;I2=0;I3=0;I4=1;I5=0;I6=0;I7=0; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);


S0=1;S1=0;S2=0;I0=0;I1=0;I2=0;I3=1;I4=0;I5=0;I6=0;I7=0; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);


S0=1;S1=0;S2=1;I0=0;I1=0;I2=1;I3=0;I4=0;I5=0;I6=0;I7=0; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);


S0=1;S1=1;S2=0;I0=0;I1=1;I2=0;I3=0;I4=0;I5=0;I6=0;I7=0; #1
      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);
```

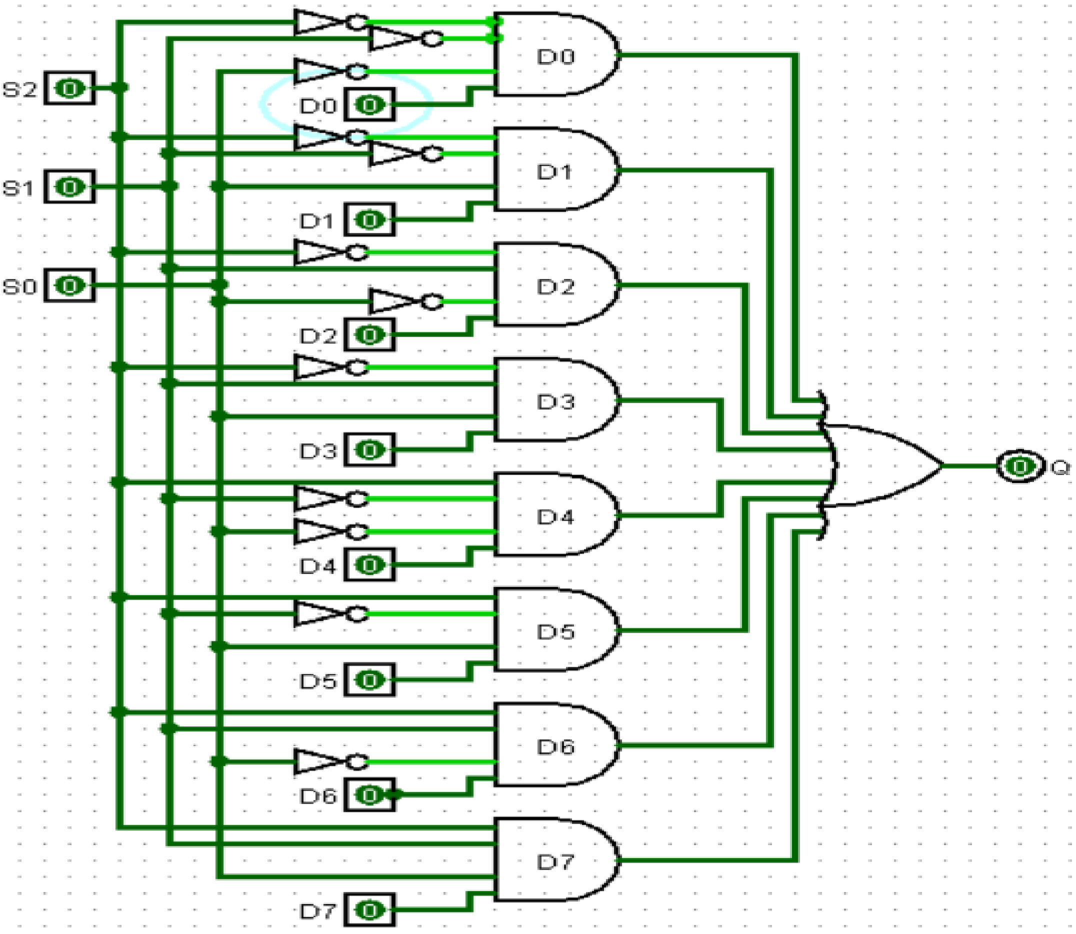
Design Code:

```
//21BCP291
Module MUX(s0,s1,s2,A0,A1,A2,A3,A4,A5,A6,A7,y);
  input s0,s1,s2;
  input A0,A1,A2,A3,A4,A5,A6,A7;
  output y;
  wire s0_not,s1_not,s2_not;
  wire B0,B1,B2,B3,B4,B5,B6;
  not(s0_not,s0);
  not(s1_not,s1);
  not(s2_not,s2);
  assign B0 = s0 & s1 & s2 & A0;
assign B1 = s0 & s1 & s2_not & A1;
assign B2 = s0 & s1_not & s2 & A2;
assign B3 = s0 & s1_not & s2_not & A3;
  assign B4 = s0_not & s1 & s2 & A4;
  assign B5 = s0_not & s1 & s2_not & A5;

Assign B6= s0_not &s1_not &s2 &A6;
Assign B7=s0_not &s1_not &s2 &A7;

Assign y=B0|B1|B2|B3|B4|B5|B6|B7;

endmodule
```

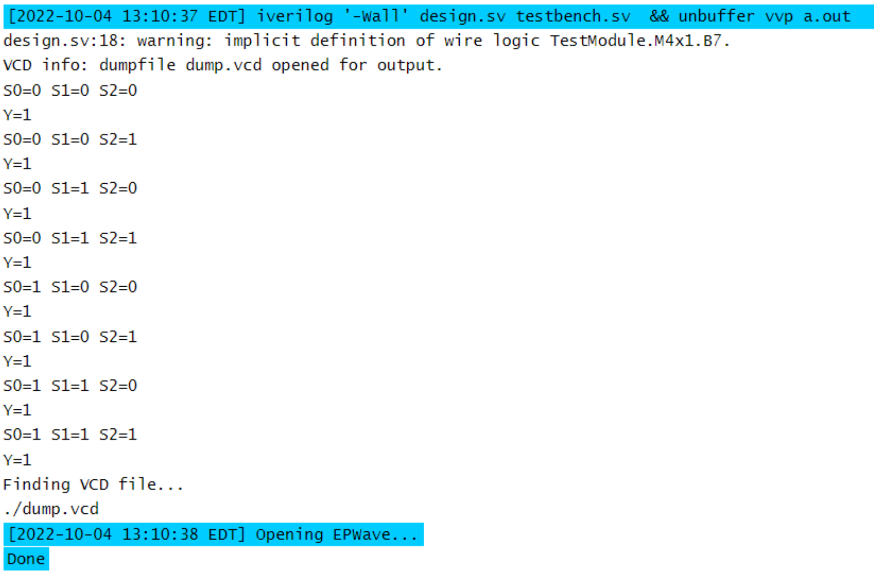
```
      S0=1;S1=1;S2=1;I0=1;I1=0;I2=0;I3=0;I4=0;I5=0;I6
      =0;I7=0;#1

      $display("S0=%b S1=%b S2=%b",S0,S1,S2);
      $display("Y=%b",Y);

 end
   initial
  begin
  $dumpfile("dump.vcd");
  $dumpvars(1);
  end
      endmodule
```

Table 2:Code of 8:1 Multiplexer

Circuit diagram(8:1 MUX):



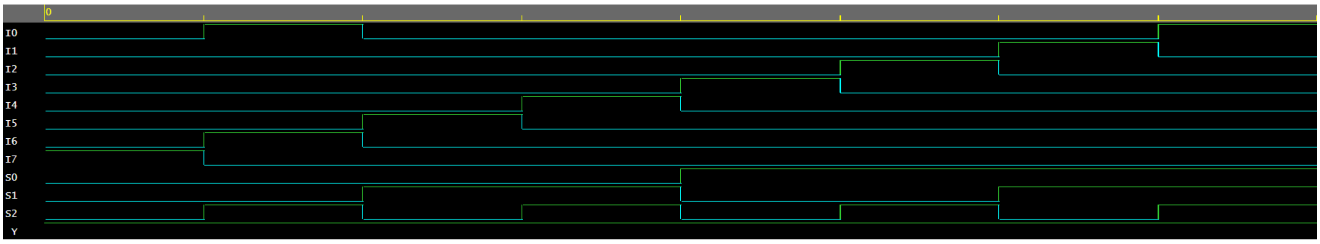
Output:



```
[2022-10-04 13:10:37 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
design.sv:18: warning: implicit definition of wire logic TestModule.M4x1.B7.
VCD info: dumpfile dump.vcd opened for output.
S0=0 S1=0 S2=0
Y=1
S0=0 S1=0 S2=1
Y=1
S0=0 S1=1 S2=0
Y=1
S0=0 S1=1 S2=1
Y=1
S0=1 S1=0 S2=0
Y=1
S0=1 S1=0 S2=1
Y=1
S0=1 S1=1 S2=0
Y=1
S0=1 S1=1 S2=1
Y=1
Finding VCD file...
./dump.vcd
[2022-10-04 13:10:38 EDT] Opening EPWave...
Done
```

Figure 3: Output of 8:1 Multiplexer

Waveform:



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Figure 4: Waveform of 8:1 Multiplexer

Question 3: Write a Verilog code to design a 1:4 Demultiplexer and verify the same.

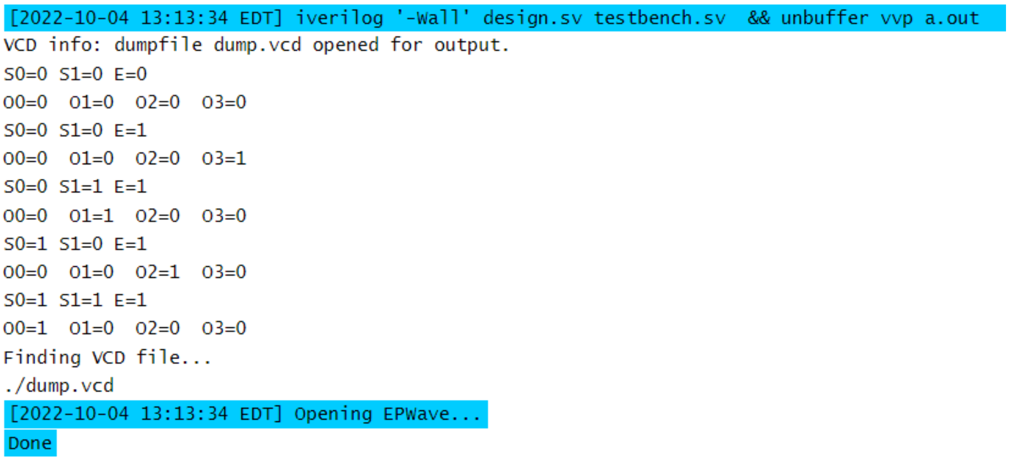
Testbench Code:

```
//21BCP322
//Akshat Shah
module
tb_DEMUX;

  reg S0,S1,E;
  wire O0,O1,O2,O3;

  DEMUX DM4x1(S0,S1,E,O0,O1,O2,O3);

  initial
    begin
     S0=0; S1=0; E=0; #1
      $display("S0=%b S1=%b E=%b",S0,S1,E);

      $display("O0=%b  O1=%b  O2=%b
O3=%b",O0,O1,O2,O3);

      S0=0; S1=0; E=1;#1
      $display("S0=%b S1=%b E=%b",S0,S1,E);
      $display("O0=%b  O1=%b  O2=%b
O3=%b",O0,O1,O2,O3);

      S0=0; S1=1; E=1;#1
      $display("S0=%b S1=%b E=%b",S0,S1,E);
      $display("O0=%b  O1=%b  O2=%b
O3=%b",O0,O1,O2,O3);

      S0=1; S1=0; E=1;#1
      $display("S0=%b S1=%b E=%b",S0,S1,E);
      $display("O0=%b  O1=%b  O2=%b
O3=%b",O0,O1,O2,O3);

      S0=1; S1=1; E=1;#1
      $display("S0=%b S1=%b E=%b",S0,S1,E);
      $display("O0=%b  O1=%b  O2=%b
O3=%b",O0,O1,O2,O3);
end
  initial
 begin
 $dumpfile("dump.vcd");
 $dumpvars(1);
end
endmodule
```

Design Code:

```
//21BCP322
module DEMUX(input  s0,s1,E, output
o0,o1,o2,o3);
  wire s0_not,s1_not,x,y,z,w;
  not(s0_not,s0);
  not(s1_not,s1);
  assign o0 = s0 & s1 & E;
  assign o1 = s0_not & s1 & E;
  assign o2 = s0 & s1_not & E;
  assign o3 = s0_not & s1_not & E;

endmodule
```

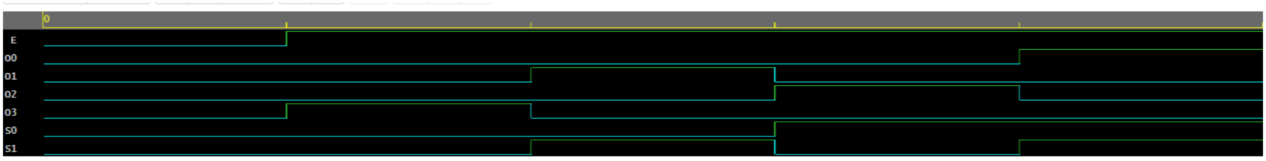
Output:



```
[2022-10-04 13:13:34 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
S0=0 S1=0 E=0
O0=0  O1=0  O2=0  O3=0
S0=0 S1=0 E=1
O0=0  O1=0  O2=0  O3=1
S0=0 S1=1 E=1
O0=0  O1=1  O2=0  O3=0
S0=1 S1=0 E=1
O0=0  O1=0  O2=1  O3=0
S0=1 S1=1 E=1
O0=1  O1=0  O2=0  O3=0
Finding VCD file...
./dump.vcd
[2022-10-04 13:13:34 EDT] Opening EPWave...
Done
```

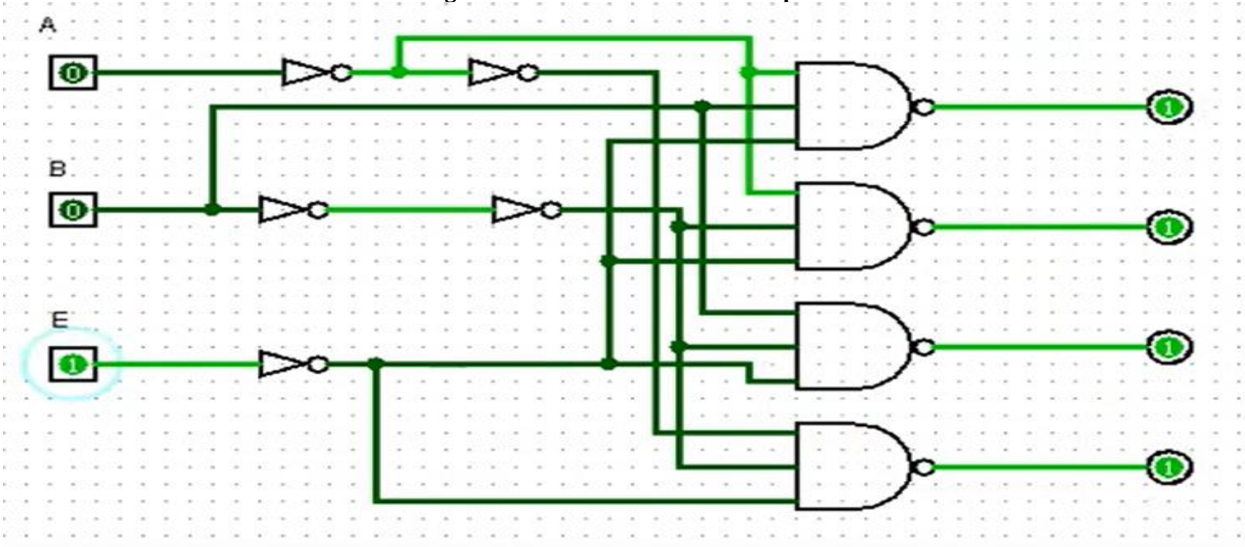
Figure 5: Output of 1:4 Demultiplexer

Waveform:



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Figure 6: Waveform of 1:4 Demultiplexer



Circuit diagram of 1:4 demultiplexer

Question 4: Write a Verilog code to design a 1:8 Demultiplexer and verify the same.

Testbench code:

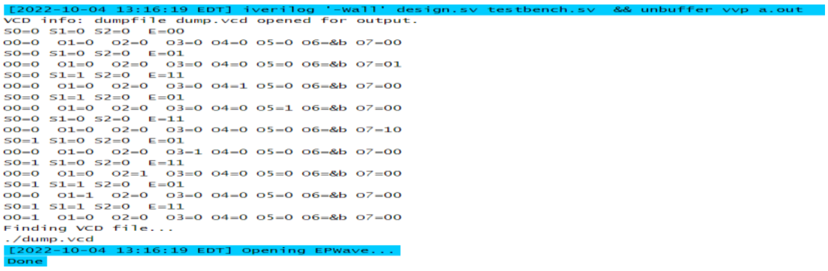
```
//21BCP322
//Akshat shah
module
tb_DEMUX;

  reg S0,S1,S2,E;
  wire O0,O1,O2,O3,O4,O5,O6,O7;

  DEMUX
DM8x1(S0,S1,S2,E,O0,O1,O2,O3,O4,O5,O6,O
7);

  initial
    begin
     S0=0; S1=0; S2=0; E=0; #1
     $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
     $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

      S0=0; S1=0; S2=0; E=1; #1
     $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
     $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

      S0=0; S1=1; S2=1; E=1; #1
     $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
     $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

      S0=0; S1=1; S2=0; E=1; #1
     $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);

     $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);
```

Design code:

```
//21BCP322
module
DEMUX(s0,s1,s2,E,A0,A1,A2,A3,A4,A5,A6,A
7);
  input s0,s1,s2,E;
  output A0,A1,A2,A3,A4,A5,A6,A7;
  wire s0_not,s1_not,s2_not;
  not(s0_not,s0);
  not(s1_not,s1);
  not(s2_not,s2);
  assign A0 = s0 & s1 & s2 & E;
  assign A1 = s0 & s1 & s2_not & E;
  assign A2 = s0 & s1_not & s2 & E;
  assign A3 = s0 & s1_not & s2_not & E;
  assign A4 = s0_not & s1 & s2 & E;
  assign A5 = s0_not & s1 & s2_not & E;
  assign A6 = s0_not & s1_not & s2 & E;
  assign A7 = s0_not & s1_not & s2_not & E;

endmodule
```

```
 $display("S0 S0=0; S1=0; S2=1; E=1; #1
    =%b S1=%b S2=0 E=%b",S0,S1,S2,E);
    $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

     S0=1; S1=0; S2=0; E=1; #1
    $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
    $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

     S0=1; S1=0; S2=1; E=1; #1
    $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
    $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

     S0=1; S1=1; S2=0; E=1; #1
    $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
    $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

     S0=1; S1=1; S2=1; E=1; #1
    $display("S0=%b S1=%b S2=0
E=%b",S0,S1,S2,E);
    $display("O0=%b  O1=%b  O2=%b  O3=%b
O4=%b O5=%b O6=&b
O7=%b",O0,O1,O2,O3,O4,O5,O6,O7);

end
  initial
 begin
 $dumpfile("dump.vcd");
 $dumpvars(1);
end
endmodule
```

Output:



```
[2022-10-04 13:16:19 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
S0=0 S1=0 S2=0  E=00
O0=0  O1=0  O2=0  O3=0 O4=0 O5=0 O6=&b O7=00
S0=0 S1=0 S2=0  E=01
O0=0  O1=0  O2=0  O3=0 O4=0 O5=0 O6=&b O7=01
S0=0 S1=1 S2=0  E=11
O0=0  O1=0  O2=0  O3=0 O4=1 O5=0 O6=&b O7=00
S0=0 S1=1 S2=0  E=01
O0=0  O1=0  O2=0  O3=0 O4=0 O5=1 O6=&b O7=00
S0=0 S1=0 S2=0  E=11
O0=0  O1=0  O2=0  O3=0 O4=0 O5=0 O6=&b O7=10
S0=1 S1=0 S2=0  E=01
O0=0  O1=0  O2=0  O3=1 O4=0 O5=0 O6=&b O7=00
S0=1 S1=0 S2=0  E=11
O0=0  O1=0  O2=1  O3=0 O4=0 O5=0 O6=&b O7=00
S0=1 S1=1 S2=0  E=01
O0=0  O1=1  O2=0  O3=0 O4=0 O5=0 O6=&b O7=00
S0=1 S1=1 S2=0  E=11
O0=1  O1=0  O2=0  O3=0 O4=0 O5=0 O6=&b O7=00
Finding VCD file...
./dump.vcd
[2022-10-04 13:16:19 EDT] Opening EPWave...
Done
```

Waveform:

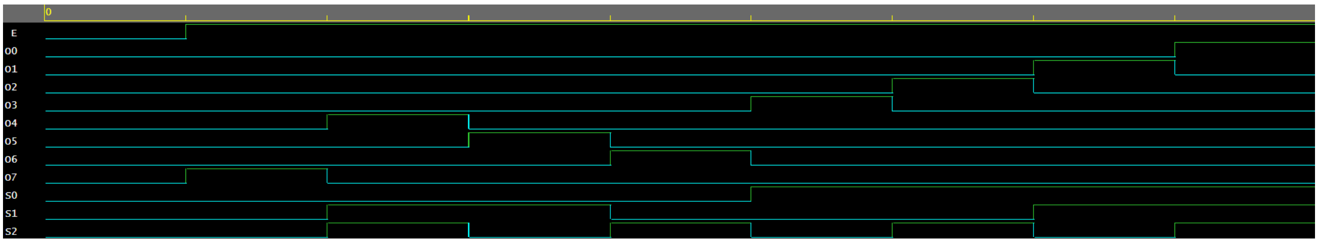
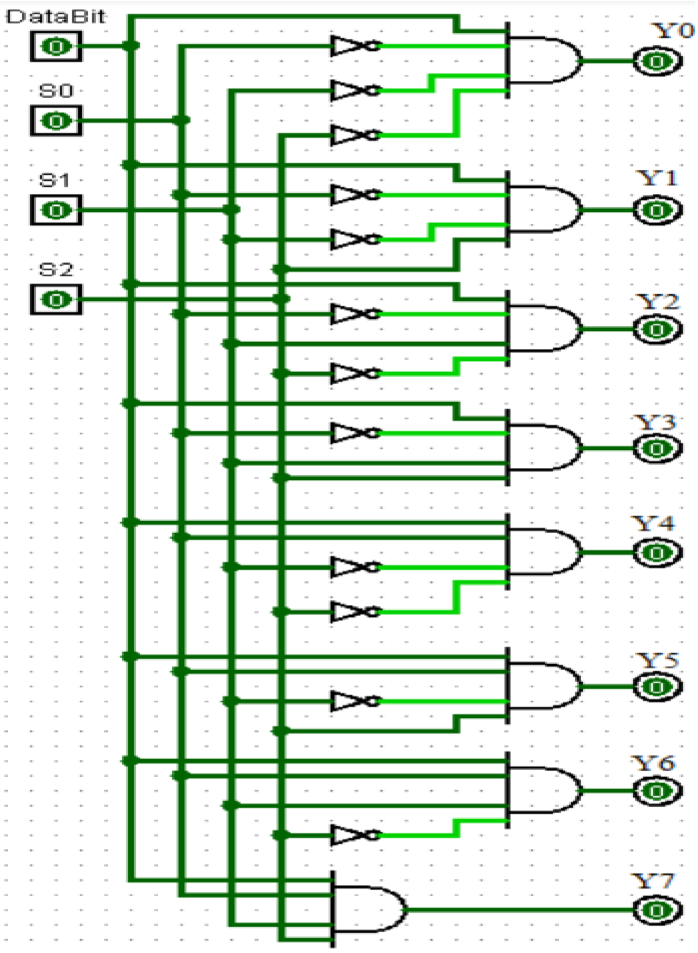


Figure 8: Waveform of 1:8 Demultiplexer

Circuit diagram:



Question 5: Write a Verilog code to design a 3:8 Decoder and verify the same.

Code:

Testbench:

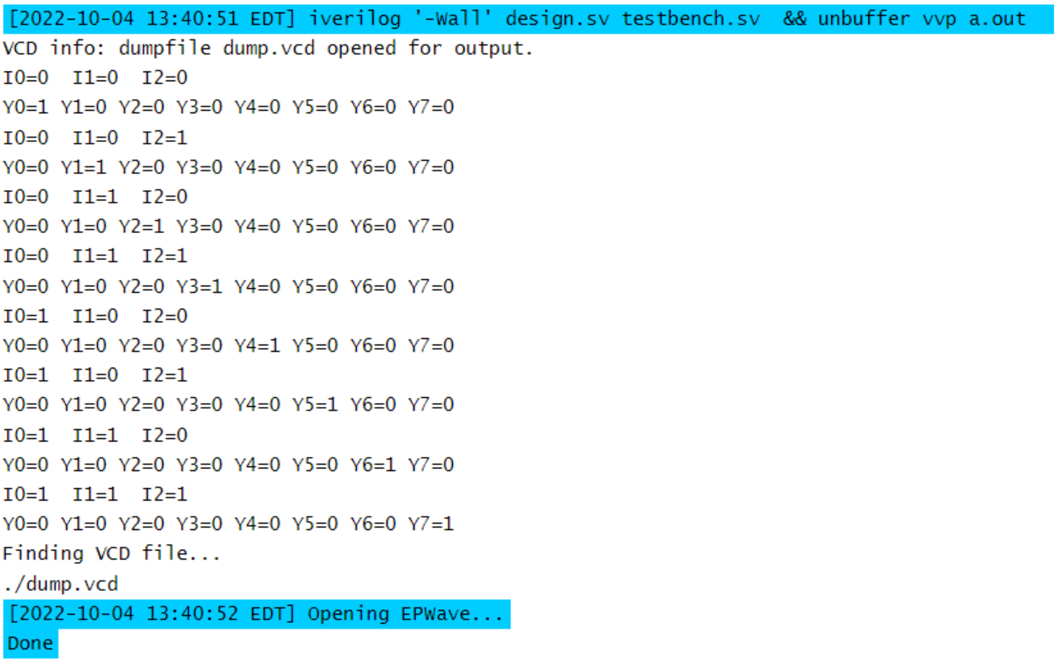
```
//21BCP322
// Akshat shah
module tb_Dec;

  reg I0,I1,I2;
  wire Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7;

  Decoder D1(I0,I1,I2,Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);
  initial
    begin
            I0=0;I1=0;I2=0;  #1
      $display("I0=%b I1=%b I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b Y4=%b Y5=%b Y6=%b Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=0;I1=0;I2=1;  #1
      $display("I0=%b I1=%b I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b Y4=%b Y5=%b Y6=%b Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=0;I1=1;I2=0;  #1
      $display("I0=%b I1=%b I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b Y4=%b Y5=%b Y6=%b Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=0;I1=1;I2=1;  #1
      $display("I0=%b I1=%b I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b Y4=%b Y5=%b Y6=%b Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=1;I1=0;I2=0;  #1
      $display("I0=%b I1=%b I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b Y4=%b Y5=%b Y6=%b Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=1;I1=0;I2=1;  #1
      $display("I0=%b I1=%b I2=%b",I0,I1,I2);
```

Design:

```
//21BCP322
module Decoder(B0,B1,B2,A0,A1,A2,A3,A4,A5,A6,A7);
  input B0,B1,B2;
  output A0,A1,A2,A3,A4,A5,A6,A7;
  assign A0 = ~B0 & ~B1 & ~B2;
  assign A1 = ~B0 & ~B1 &  B2;
  assign A2 = ~B0 &  B1 & ~B2;
  assign A3 = ~B0 &  B1 &  B2;
  assign A4 =  B0 & ~B1 & ~B2;
  assign A5 =  B0 & ~B1 &  B2;
  assign A6 =  B0 &  B1 & ~B2;
  assign A7 =  B0 &  B1 &  B2;

endmodule
```

```
      $display("Y0=%b Y1=%b Y2=%b Y3=%b
Y4=%b Y5=%b Y6=%b
Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=1;I1=1;I2=0;  #1
      $display("I0=%b I1=%b
I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b
Y4=%b Y5=%b Y6=%b
Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

     I0=1;I1=1;I2=1;  #1
      $display("I0=%b I1=%b
I2=%b",I0,I1,I2);
      $display("Y0=%b Y1=%b Y2=%b Y3=%b
Y4=%b Y5=%b Y6=%b
Y7=%b",Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7);

end
  initial
 begin
 $dumpfile("dump.vcd");
 $dumpvars(1);
end
endmodule
```

Output:



```
[2022-10-04 13:40:51 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
I0=0  I1=0  I2=0
Y0=1 Y1=0 Y2=0 Y3=0 Y4=0 Y5=0 Y6=0 Y7=0
I0=0  I1=0  I2=1
Y0=0 Y1=1 Y2=0 Y3=0 Y4=0 Y5=0 Y6=0 Y7=0
I0=0  I1=1  I2=0
Y0=0 Y1=0 Y2=1 Y3=0 Y4=0 Y5=0 Y6=0 Y7=0
I0=0  I1=1  I2=1
Y0=0 Y1=0 Y2=0 Y3=1 Y4=0 Y5=0 Y6=0 Y7=0
I0=1  I1=0  I2=0
Y0=0 Y1=0 Y2=0 Y3=0 Y4=1 Y5=0 Y6=0 Y7=0
I0=1  I1=0  I2=1
Y0=0 Y1=0 Y2=0 Y3=0 Y4=0 Y5=1 Y6=0 Y7=0
I0=1  I1=1  I2=0
Y0=0 Y1=0 Y2=0 Y3=0 Y4=0 Y5=0 Y6=1 Y7=0
I0=1  I1=1  I2=1
Y0=0 Y1=0 Y2=0 Y3=0 Y4=0 Y5=0 Y6=0 Y7=1
Finding VCD file...
./dump.vcd
[2022-10-04 13:40:52 EDT] Opening EPWave...
Done
```

Figure 9: Output of 3:8 Decoder

Waveform:

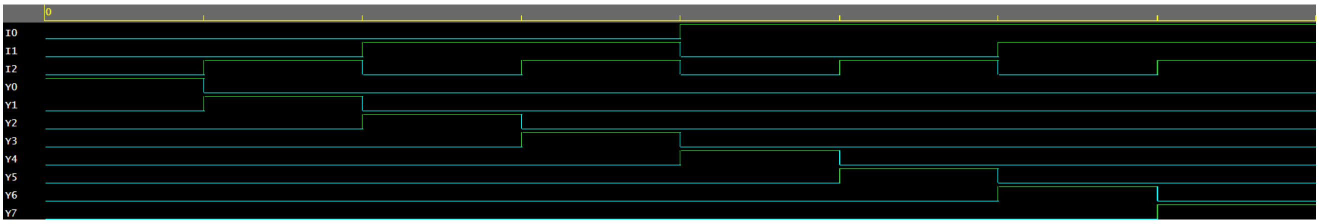
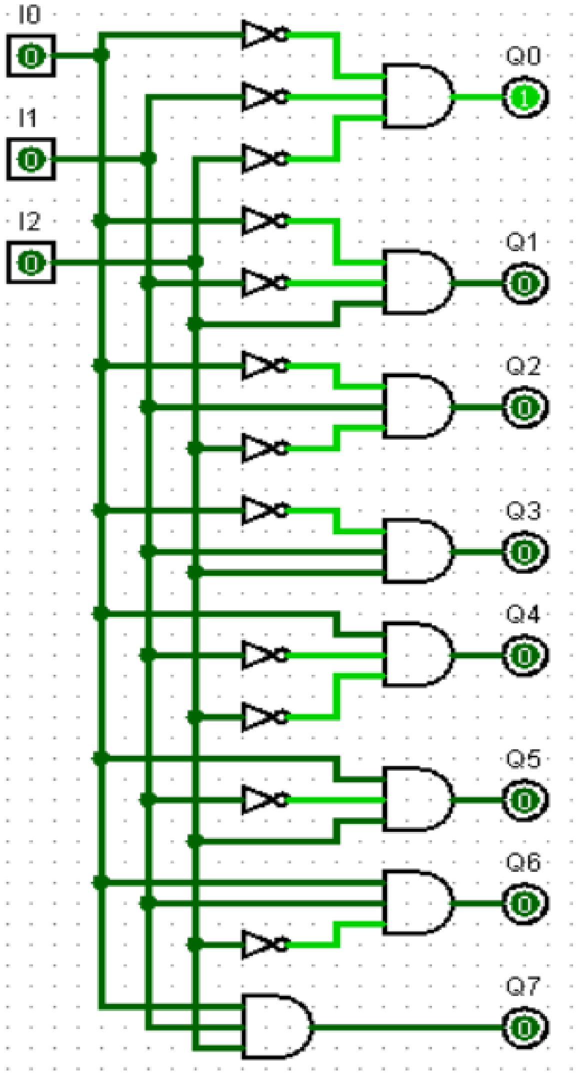


Figure 10: Waveform of 3:8 Decoder

Circuit diagram:



Question 6: Write a Verilog code to design a 8:3 Encoder and verify the same.

Testbench:

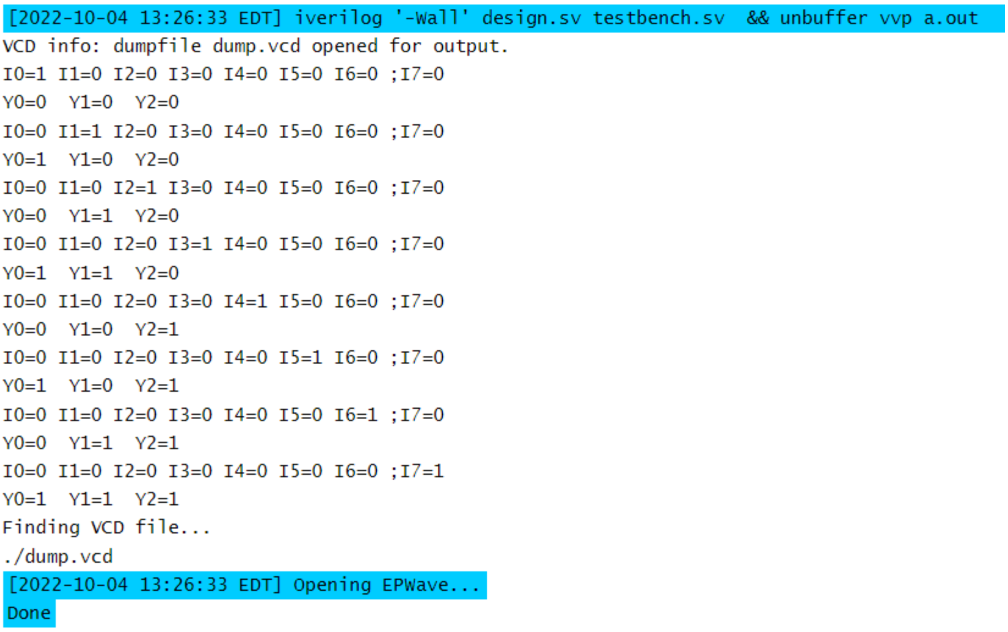
```
//21BCP322
//Akshat shah
module tb_Enc;

  reg I0,I1,I2,I3,I4,I5,I6,I7;
  wire Y0,Y1,Y2;

  Encoder
E1(I0,I1,I2,I3,I4,I5,I6,I7,Y0,Y1,Y2);
  initial
    begin

I0=1;I1=0;I2=0;I3=0;I4=0;I5=0;I6=0;I7=0;  #1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=1;I2=0;I3=0;I4=0;I5=0;I6=0;I7=0;
#1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=0;I2=1;I3=0;I4=0;I5=0;I6=0;I7=0;
#1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=0;I2=0;I3=1;I4=0;I5=0;I6=0;I7=0;
      #1


      $display("I0=%b I1=%b I2=%b I3=%b
      I4=%b I5=%b
      I6=%b;I7=%b”,I0,I1,I2,I3,I4,I5,I6,I7);
```

Design:

```
//21BCP291
module
Encoder(A0,A1,A2,A3,A4,A5,A6,A7,B0,B1,B2);
input A0,A1,A2,A3,A4,A5,A6,A7;
  output B0,B1,B2;
  assign B0 = A1 | A3 | A5 | A7;
  assign B1 = A2 | A3 | A6 | A7;
  assign B2 = A4 | A5 | A6 | A7;

endmodule
```

```
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=0;I2=0;I3=0;I4=1;I5=0;I6=0;I7=0;
#1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=0;I2=0;I3=0;I4=0;I5=1;I6=0;I7=0;
#1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=0;I2=0;I3=0;I4=0;I5=0;I6=1;I7=0;
#1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);

      I0=0;I1=0;I2=0;I3=0;I4=0;I5=0;I6=0;I7=1;
#1
      $display("I0=%b I1=%b I2=%b I3=%b
I4=%b I5=%b I6=%b
;I7=%b",I0,I1,I2,I3,I4,I5,I6,I7);
      $display("Y0=%b  Y1=%b
Y2=%b",Y0,Y1,Y2);
end
  initial
 begin
 $dumpfile("dump.vcd");
 $dumpvars(1);
end
endmodule
```

Output:



```
[2022-10-04 13:26:33 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
I0=1 I1=0 I2=0 I3=0 I4=0 I5=0 I6=0 ;I7=0
Y0=0  Y1=0  Y2=0
I0=0 I1=1 I2=0 I3=0 I4=0 I5=0 I6=0 ;I7=0
Y0=1  Y1=0  Y2=0
I0=0 I1=0 I2=1 I3=0 I4=0 I5=0 I6=0 ;I7=0
Y0=0  Y1=1  Y2=0
I0=0 I1=0 I2=0 I3=1 I4=0 I5=0 I6=0 ;I7=0
Y0=1  Y1=1  Y2=0
I0=0 I1=0 I2=0 I3=0 I4=1 I5=0 I6=0 ;I7=0
Y0=0  Y1=0  Y2=1
I0=0 I1=0 I2=0 I3=0 I4=0 I5=1 I6=0 ;I7=0
Y0=1  Y1=0  Y2=1
I0=0 I1=0 I2=0 I3=0 I4=0 I5=0 I6=1 ;I7=0
Y0=0  Y1=1  Y2=1
I0=0 I1=0 I2=0 I3=0 I4=0 I5=0 I6=0 ;I7=1
Y0=1  Y1=1  Y2=1
Finding VCD file...
./dump.vcd
[2022-10-04 13:26:33 EDT] Opening EPWave...
Done
```

Figure 11: Output of 8:3 Encoder

Waveform:

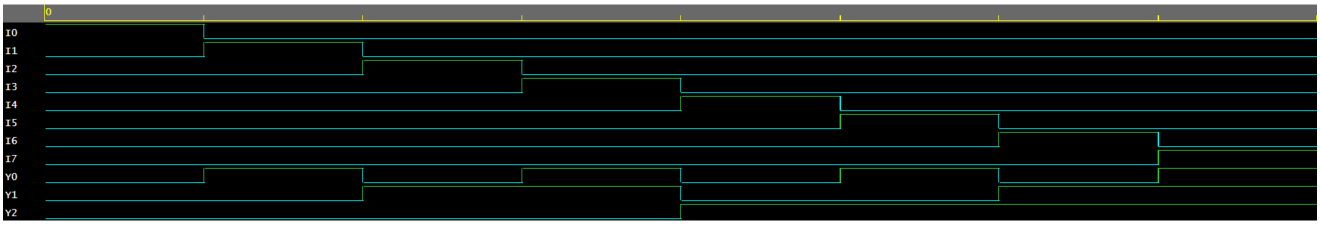
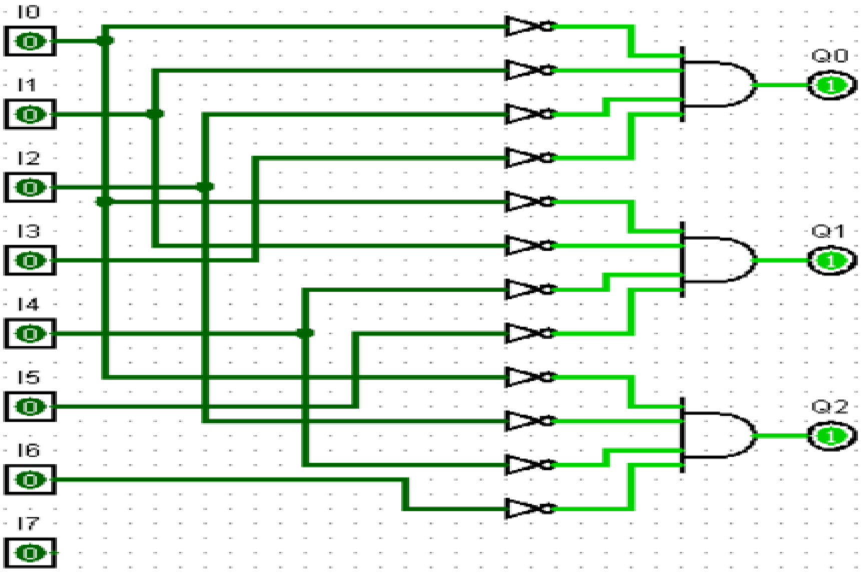


Figure 12: Waveform of 8:3 Encoder

Circuit diagram:


I0
0
I1
0
I2
0
I3
0
I4
0
I5
0
I6
0
I7
0
Q0
1
Q1
1
Q2
1