

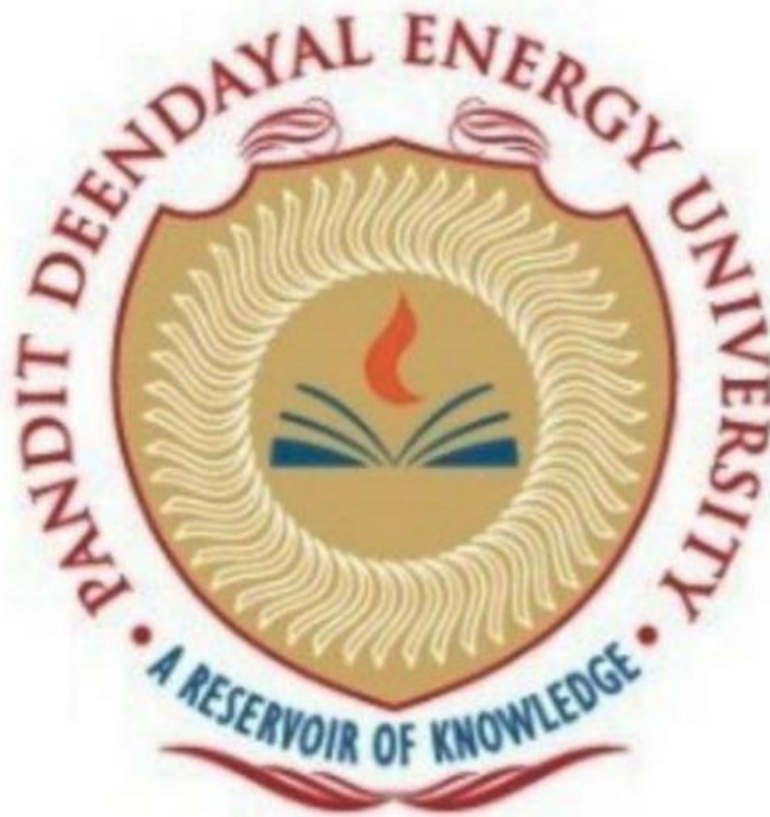
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Sem – III

Digital Electronics and Computer Organization Lab

Course Code – 20CP203P



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School of Technology,  
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### Assignment-3

**Aim:** To learn module instantiation using structural and behavioral methods.

#### Table of Contents

#### 1. Behavioral Code for expressions:..... **Error! Bookmark not defined.**

1.1.  $F(A, B, C) = A'BC + AB'C + ABC$

1.2  $F(A, B, C, D) = ABCD' + A'BCD + AB'CD' + ABC$

1.3  $F(A, B, C, D, E, F) = ABC + DE + F$

1.4  $F(A, B) = (A' + B')(A + B')(A' + B)(A + B)$

1.5  $F(A, B) = ((A.B')' + ((A)'(B)'))'$

1.6  $F(A, B) = (((A)' + B)'. ((A)' + (B)'))'$

#### 2. XOR gate using Behavioural and Structural code**Error! Bookmark not defined.**

#### 3. Structural Code for expressions: ..... **Error! Bookmark not defined.**

3.1  $F(A, B, C) = (A' + B' + C')(A + B' + C')(A' + B + C')(A' + B)'$

3.2  $F(A, B, C, D, E) = ((A + B).(C + D + E))'$

#### 4. Structural code using NAND and NOR gates ..... **Error! Bookmark not defined.**

4.1  $F(A, B, C) = (AB'C) + (AB'C')$

4.2  $F(A, B) = A'B' + AB' + A'B + AB$

#### 5. Instantiate XOR gate using AND, OR, NOT gate ... **Error! Bookmark not defined.**

#### 6. Implement $Y = A'.B'.C' + A'.B.C' + A.B'.C' + A.B'.C$ .....



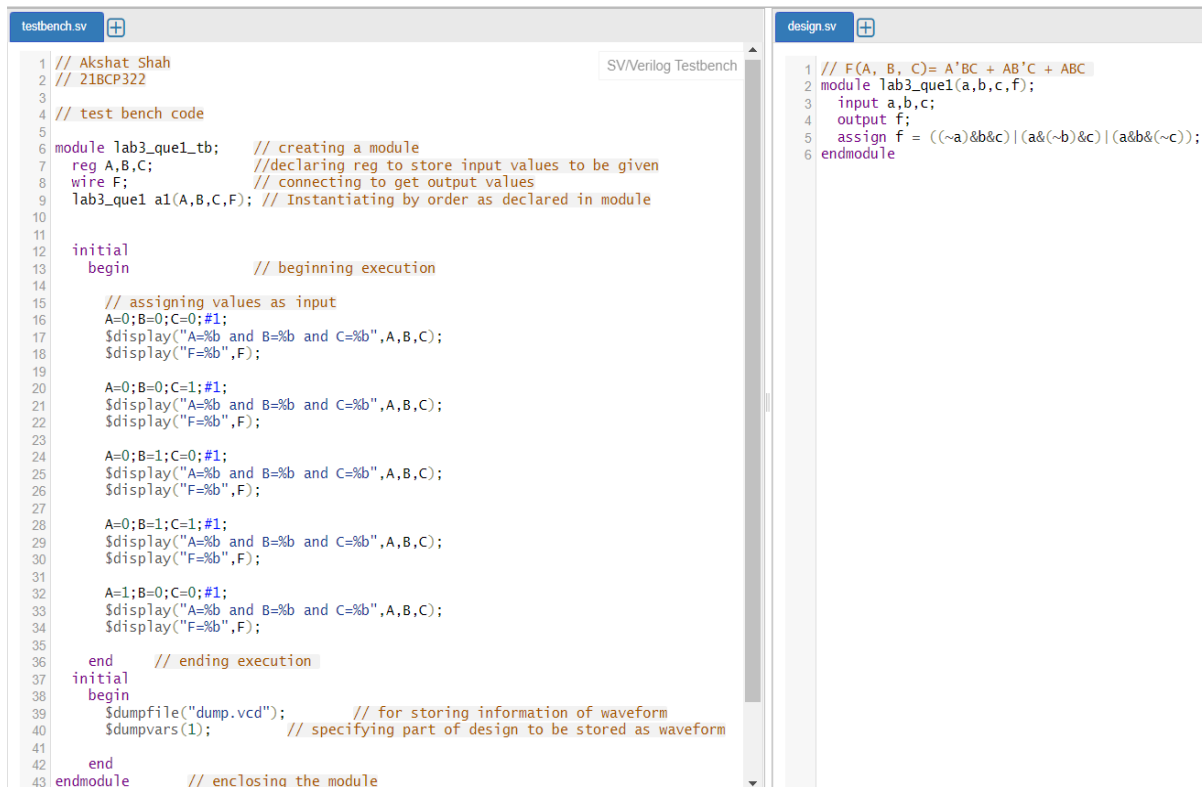


## List of Questions:

**Question 1:** Implement the following expression using the Verilog Hardware Description Language (HDL) then compare with truth table whether your circuit produced same output or not? Moreover, verify your circuit against the waveform.

1.1  $F(A, B, C) = A'BC + AB'C + ABC$

### Verilog Code:



```
testbench sv
1 // Akshat Shah
2 // 218CP322
3
4 // test bench code
5
6 module lab3_que1_tb; // creating a module
7 reg A,B,C; //declaring reg to store input values to be given
8 wire F; // connecting to get output values
9 lab3_que1 a1(A,B,C,F); // Instantiating by order as declared in module
10
11
12 initial
13 begin // beginning execution
14
15 // assigning values as input
16 A=0;B=0;C=0;#1;
17 $display("A=%b and B=%b and C=%b",A,B,C);
18 $display("F=%b",F);
19
20 A=0;B=0;C=1;#1;
21 $display("A=%b and B=%b and C=%b",A,B,C);
22 $display("F=%b",F);
23
24 A=0;B=1;C=0;#1;
25 $display("A=%b and B=%b and C=%b",A,B,C);
26 $display("F=%b",F);
27
28 A=0;B=1;C=1;#1;
29 $display("A=%b and B=%b and C=%b",A,B,C);
30 $display("F=%b",F);
31
32 A=1;B=0;C=0;#1;
33 $display("A=%b and B=%b and C=%b",A,B,C);
34 $display("F=%b",F);
35
36 end // ending execution
37 initial
38 begin
39 $dumpfile("dump.vcd"); // for storing information of waveform
40 $dumpvars(1); // specifying part of design to be stored as waveform
41
42 end
43 endmodule // enclosing the module

design sv
1 // F(A, B, C)= A'BC + AB'C + ABC
2 module lab3_que1(a,b,c,f);
3 input a,b,c;
4 output f;
5 assign f = ((~a)&b&c) | (a&(~b)&c) | (a&b&(~c));
6 endmodule
```

Fig 1.1.1- Testbench and design code

### Output:

```
A=0 and B=0 and C=0
F=0
A=0 and B=0 and C=1
F=0
A=0 and B=1 and C=0
F=0
A=0 and B=1 and C=1
F=1
A=1 and B=0 and C=0
F=0
```

Fig 1.1.2 - Output as Truth table

### Waveform:

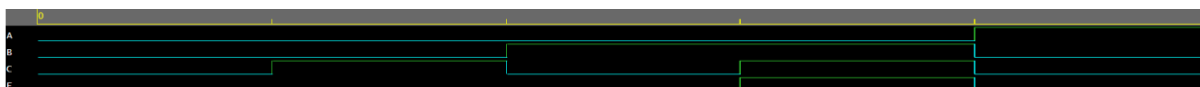


Fig 1.1.3- Waveform for output

## 1.2 $F(A, B, C, D) = ABCD' + A'BCD + AB'CD' + ABC$

### Verilog Code:

testbench sv

```
1 // Akshat Shah
2 // 21BCP322
3
4 module lab3_que1_2_tb; // creating a module
5   reg A,B,C,D;
6   wire F;
7   lab3_que1_2 a1(A,B,C,D,F); // Instantiating by order as declared in module
8
9
10  initial
11    begin // beginning execution
12
13      // assigning values as input
14      A=0;B=0;C=0;D=0;#1;
15      $display("A=%b and B=%b and C=%b and D=%b",A,B,C,D);
16      $display("F=%b",F);
17
18      A=0;B=0;C=1;D=1;#1;
19      $display("A=%b and B=%b and C=%b and D=%b",A,B,C,D);
20      $display("F=%b",F);
21
22      A=0;B=1;C=0;D=0;#1;
23      $display("A=%b and B=%b and C=%b and D=%b",A,B,C,D);
24      $display("F=%b",F);
25
26      A=0;B=1;C=1;D=1;#1;
27      $display("A=%b and B=%b and C=%b and D=%b",A,B,C,D);
28      $display("F=%b",F);
29
30      A=1;B=0;C=0;D=0;#1;
31      $display("A=%b and B=%b and C=%b and D=%b",A,B,C,D);
32      $display("F=%b",F);
33
34    end // ending execution
35  initial
36    begin
37      $dumpfile("dump.vcd"); // for storing information of waveform
38      $dumpvars(1); // specifying part of design to be stored as waveform
39    end
40 endmodule // enclosing the module
41
```

design sv

```
1 // F(A, B, C, D) = ABCD' + A'BCD + AB'CD' + ABC
2
3 module lab3_que1_2(a,b,c,d,f);
4   input a,b,c,d;
5   output f;
6   assign f = (a&b&c&(~d))|((~a)&b&c&d)|(a&(~b)&c&(~d))| (a&b&c);
7 endmodule
```

Fig 1.2.1- Testbench and design code

### Output:

```
A=0 and B=0 and C=0 and D=0
F=0
A=0 and B=0 and C=1 and D=1
F=0
A=0 and B=1 and C=0 and D=0
F=0
A=0 and B=1 and C=1 and D=1
F=1
A=1 and B=0 and C=0 and D=0
F=0
```

Fig 1.2.2 - Output as truth table

### Waveform:

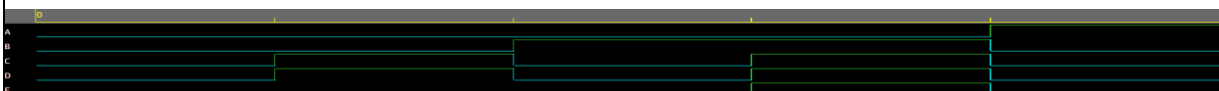


Fig 1.2.3- Waveform of output

### 1.3 $F(A, B, C, D, E, F) = ABC + DE + F$

#### Verilog Code:

testbench.sv

```
1 // Akshat Shah
2 // 21BCP322
3
4 module lab3_que1_3_tb; // creating a module
5     reg A,B,C,D,E,F;
6     wire W;
7     lab3_que1_3 a1(A,B,C,D,E,F,W); // Instantiating by order as declared in
8     module
9
10    initial
11        begin // beginning execution
12
13            // assigning values as input
14            A=0;B=0;C=0;D=0;E=0;F=0;#1;
15            $display("A=%b and B=%b and C=%b and D=%b and E=%b and F=%b",A,B,C,D,E,F);
16            $display("W=%b",W);
17
18            A=0;B=0;C=0;D=0;E=1;F=1;#1;
19            $display("A=%b and B=%b and C=%b and D=%b and E=%b and F=%b",A,B,C,D,E,F);
20            $display("W=%b",W);
21
22            A=0;B=0;C=0;D=0;E=1;F=0;#1;
23            $display("A=%b and B=%b and C=%b and D=%b and E=%b and F=%b",A,B,C,D,E,F);
24            $display("W=%b",W);
25
26            A=0;B=0;C=0;D=0;E=1;F=1;#1;
27            $display("A=%b and B=%b and C=%b and D=%b and E=%b and F=%b",A,B,C,D,E,F);
28            $display("W=%b",W);
29
30        end // ending execution
31    initial
32        begin
33            $dumpfile("dump.vcd"); // for storing information of waveform
34            $dumpvars(1); // specifying part of design to be stored as waveform
35
36        end
37 endmodule // enclosing the module
```

design.sv

```
1 // F(A, B, C, D, E, F) = ABC + DE + F
2
3 module lab3_que1_3(a,b,c,d,e,f,w);
4     input a,b,c,d,e,f;
5     output w;
6     assign w = (a&b&c)|(d&e)|(f);
7 endmodule
```

Fig 1.3.1- Testbench and design code

#### Output:

A=0 and B=0 and C=0 and D=0 and E=0 and F=0  
W=0  
A=0 and B=0 and C=0 and D=0 and E=0 and F=1  
W=1  
A=0 and B=0 and C=0 and D=0 and E=1 and F=0  
W=0  
A=0 and B=0 and C=0 and D=0 and E=1 and F=1  
W=1

Fig 1.3.2 - Output as truth table

#### Waveform:

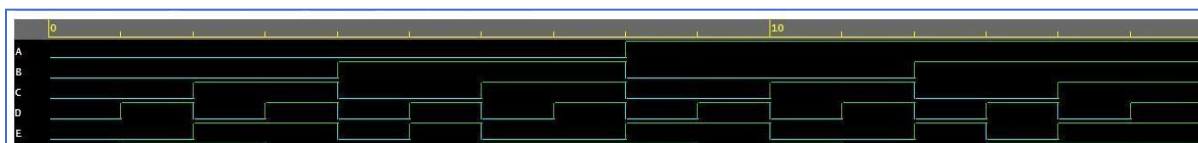


Fig 1.3.3- Waveform of output

## 1.4 $F(A, B) = (A' + B')(A + B')(A' + B)(A + B)$

### Verilog Code:

```
testbench.sv
1 // Akshat Shah
2 // 21BCP322
3
4 module lab3_que1_tb; // creating a module
5     reg A,B;
6     wire F;
7     lab3_que1 a1(A,B,F); // Instantiating by order as declared in module
8
9
10    initial
11        begin // beginning execution
12
13            // assigning values as input
14            A=0;B=0;#1;
15            $display("A=%b and B=%b ",A,B);
16            $display("F=%b",F);
17
18            A=0;B=1;#1;
19            $display("A=%b and B=%b ",A,B); // for display of values entered
20            $display("F=%b",F);
21
22            A=1;B=0;#1;
23            $display("A=%b and B=%b ",A,B);
24            $display("F=%b",F);
25
26            A=1;B=1;#1;
27            $display("A=%b and B=%b ",A,B);
28            $display("F=%b",F);
29
30            A=1;B=0;#1;
31            $display("A=%b and B=%b ",A,B);
32            $display("F=%b",F);
33
34        end // ending execution
35    initial
36        begin
37            $dumpfile("dump.vcd"); // for storing information of waveform
38            $dumpvars(1); // specifying part of design to be stored as waveform
39        end
40 endmodule // enclosing the module

design.sv
1 // F(A, B) = (A'+B')(A+B')(A'+B)(A+B)
2 module lab3_que1(a,b,f);
3     input a,b;
4     output f;
5     assign f = ((~a)|(~b)) & (a|(~b)) & ((~a)|b) & (a|b);
6 endmodule
```

Fig 1.4.1- Testbench and design code

### Output:

```
A=0 and B=0
F=0
A=0 and B=1
F=0
A=1 and B=0
F=0
A=1 and B=1
F=0
A=1 and B=0
F=0
```

Fig 1.4.2- output as truth table

### Waveform:

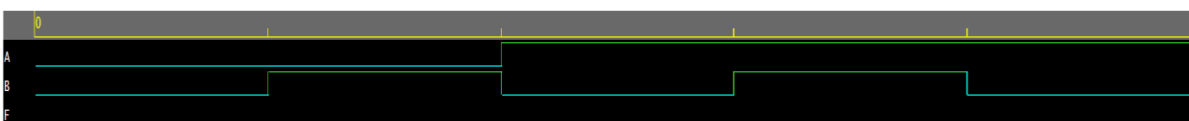


Fig 1.4.3- Waveform of output



## 1.5 $F(A, B) = ((A.B')' + ((A)'(B)'))'$

### Verilog Code:

```
testbench.sv
1 // Akshat Shah
2 // 218CP322
3
4 module lab3_que1_tb;    // creating a module
5 reg A,B;
6 wire F;
7 lab3_que1 a1(A,B,F); // Instantiating by order as declared in module
8
9
10 initial
11 begin                // beginning execution
12
13     // assigning values as input
14     A=0;B=0;#1;
15     $display("A=%b and B=%b ",A,B);
16     $display("F=%b",F);
17
18     A=0;B=1;#1;
19     $display("A=%b and B=%b ",A,B);    // for display of values entered
20     $display("F=%b",F);
21
22     A=1;B=0;#1;
23     $display("A=%b and B=%b",A,B);
24     $display("F=%b",F);
25
26     A=1;B=1;#1;
27     $display("A=%b and B=%b ",A,B);
28     $display("F=%b",F);
29
30     A=1;B=0;#1;
31     $display("A=%b and B=%b",A,B);
32     $display("F=%b",F);
33
34 end                // ending execution
35 initial
36 begin
37     $dumpfile("dump.vcd");    // for storing information of waveform
38     $dumpvars(1);            // specifying part of design to be stored as waveform
39 end
40 endmodule            // enclosing the module
41
design.sv
1 // F(A, B)= ((A.B')'+((A)'(B)'))'
2
3 module lab3_que1(a,b,f);
4 input a,b;
5 output f;
6 assign f = ~((~(a&(~b))) | (~((~a)&(~b)))));
7 endmodule
8
```

Fig 1.5.1- Testbench and design code

### Output:

A=0 and B=0  
F=1  
A=0 and B=1  
F=1  
A=1 and B=0  
F=1  
A=1 and B=1  
F=1  
A=1 and B=0  
F=1

Fig 1.5.2- Output as truth table

### Waveform:

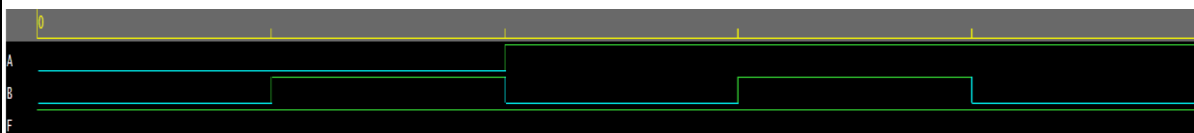


Fig 1.5.3- Waveform of output

$$1.6 \quad F(A, B) = (((A)' + B)'. ((A)' + (B)'))'$$

Verilog code:

testbench.sv

```

1 // Akshat Shah
2 // 21BCP322
3
4 module lab3_que1_tb;    // creating a module
5   reg A,B;
6   wire F;
7   lab3_que1 a1(A,B,F); // Instantiating by order as declared in module
8
9
10  initial
11    begin              // beginning execution
12
13      // assigning values as input
14      A=0;B=0;#1;
15      $display("A=%b and B=%b ",A,B);
16      $display("F=%b",F);
17
18      A=0;B=1;#1;
19      $display("A=%b and B=%b ",A,B);    // for display of values entered
20      $display("F=%b",F);
21
22      A=1;B=0;#1;
23      $display("A=%b and B=%b ",A,B);
24      $display("F=%b",F);
25
26      A=1;B=1;#1;
27      $display("A=%b and B=%b ",A,B);
28      $display("F=%b",F);
29
30      A=1;B=0;#1;
31      $display("A=%b and B=%b ",A,B);
32      $display("F=%b",F);
33
34    end                // ending execution
35  initial
36    begin
37      $dumpfile("dump.vcd"); // for storing information of waveform
38      $dumpvars(1);         // specifying part of design to be stored as waveform
39    end
40 endmodule              // enclosing the module

```

design.sv

```

1 // F(A, B) = (((A)' + B)'. ((A)' + (B)'))'
2
3 module lab3_que1(a,b,f);
4   input a,b;
5   output f;
6   assign f = ~((~a|b)& (~((~a)|(~b)))) ;
7 endmodule
8

```

Fig 1.6.1- Testbench and design code

Output:

```

A=0 and B=0
F=1
A=0 and B=1
F=1
A=1 and B=0
F=1
A=1 and B=1
F=1
A=1 and B=0
F=1

```

Fig 1.6.2- Output as truth table

Waveform:

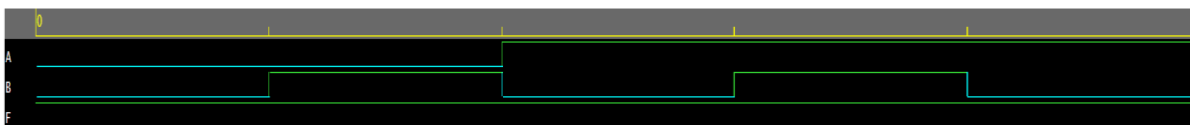


Fig 1.6.3- Waveform of output

## Question 2: Implement the XOR gate using Behavioural and Structural code of Verilog Hardware Description Language.

### Verilog Code:

```
testbench.vv +
1 // Akshat Shah
2 // 218CP322
3
4 // test bench code for XOR gate
5
6 module lab3_que2_tb; // creating a module
7 reg A,B;
8 wire F;
9 lab3_que2 a1(A,B,F); // Instantiating by order as declared in module
10
11
12 initial
13 begin // beginning execution
14
15 // assigning values as input
16 A=0;B=0;#1;
17 $display("A=%b and B=%b ",A,B);
18 $display("F=%b",F);
19
20 A=0;B=1;#1;
21 $display("A=%b and B=%b ",A,B); // for display of values entered
22 $display("F=%b",F);
23
24 A=1;B=0;#1;
25 $display("A=%b and B=%b ",A,B);
26 $display("F=%b",F);
27
28 A=1;B=1;#1;
29 $display("A=%b and B=%b ",A,B);
30 $display("F=%b",F);
31
32
33 end // ending execution
34
35 initial
36 begin
37 $dumpfile("dump.vcd"); // for storing information of waveform
38 $dumpvars(1); // specifying part of design to be stored as waveform
39 end
40 endmodule // enclosing the module
41
design.vv +
1 // XOR_GATE
2
3 // Behavioral Code
4
5 module lab3_que2(a,b,f);
6 input a,b;
7 output f;
8 assign f = ((~a)&b| a&(~b)) ;
9 endmodule
10
11
12
13
14
15
16 // Structural code
17
18 /* module lab3_que2(a,b,c);
19 input a,b;
20 output f;
21 wire a_not,b_not,x,y;
22 not(a_not,a);
23 not(b_not,b);
24 and(x,a_not,b);
25 and(y,a,b_not);
26 or(f,x,y);
27 end module
28 */
```

Fig 2.1- Testbench and design code

### Output:

A=0 and B=0  
F=0  
A=0 and B=1  
F=1  
A=1 and B=0  
F=1  
A=1 and B=1  
F=0

Fig 2.2 Output as truth table

### Waveform:

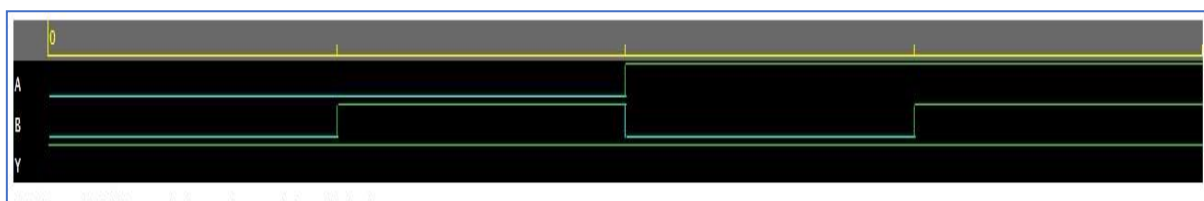


Fig 2.3- Waveform

**Question: 3:** Implement the following expression using the Verilog Hardware Description Language (HDL) (Structural Coding).

$$3.1 \quad F(A, B, C) = (A' + B' + C')(A + B' + C')(A' + B + C')(A' + B')$$

**Verilog Code:**

The image shows two panels of Verilog code. The left panel, titled 'testbench.sv', contains a testbench module 'lab3\_que3\_tb' that instantiates the 'lab3\_que3' module and applies various input values to A, B, and C. The right panel, titled 'design.sv', contains the structural code for the 'lab3\_que3' module, which implements the logic of the given Boolean expression using basic gates (NOT, AND, OR).

```

1 // Akshat Shah
2 // 218CP322
3
4 // Test bench code
5
6
7 module lab3_que3_tb; // creating a module
8   reg A,B,C;
9   wire F;
10  lab3_que3 a1(A,B,C,F); // Instantiating by order as declared in module
11
12
13  initial
14  begin // beginning execution
15
16      // assigning values as input
17      A=0;B=0;C=0;#1;
18      $display("A=%b and B=%b and C=%b",A,B,C);
19      $display("F=%b",F);
20
21      A=0;B=0;C=1;#1;
22      $display("A=%b and B=%b and C=%b",A,B,C); // for display of values entered
23      $display("F=%b",F);
24
25      A=0;B=1;C=0;#1;
26      $display("A=%b and B=%b and C=%b",A,B,C);
27      $display("F=%b",F);
28
29      A=0;B=1;C=1;#1;
30      $display("A=%b and B=%b and C=%b",A,B,C);
31      $display("F=%b",F);
32
33
34  end // ending execution
35  initial
36  begin
37      $dumpfile("dump.vcd"); // for storing information of waveform
38      $dumpvars(1); // specifying part of design to be stored as waveform
39  end
40 endmodule // enclosing the module
41
42
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97
98
99

```

Fig 3.1.1 - Testbench and design code

**Output:**

```

A=0 and B=0 and C=0
F=0
A=0 and B=0 and C=1
F=0
A=0 and B=1 and C=0
F=0
A=0 and B=1 and C=1
F=0

```

Fig 3.1.2- Output as truth table

**Waveform:**

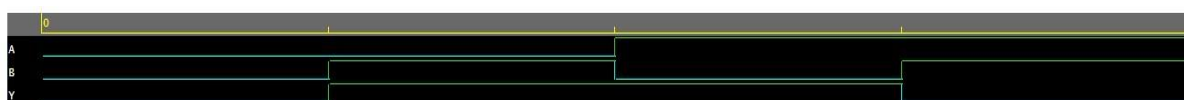
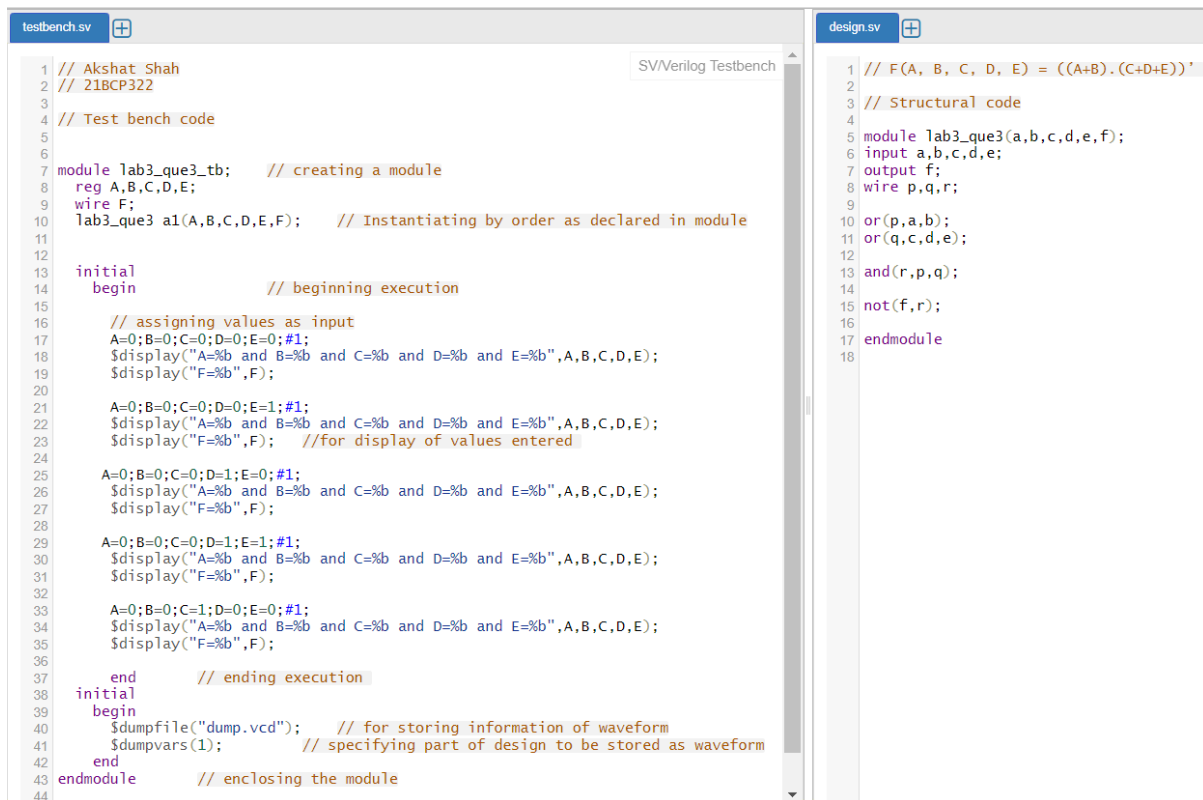


Fig 3.1.3- Output as truth table

## 3.2 $F(A, B, C, D, E) = ((A+B).(C+D+E))'$

### Verilog code:



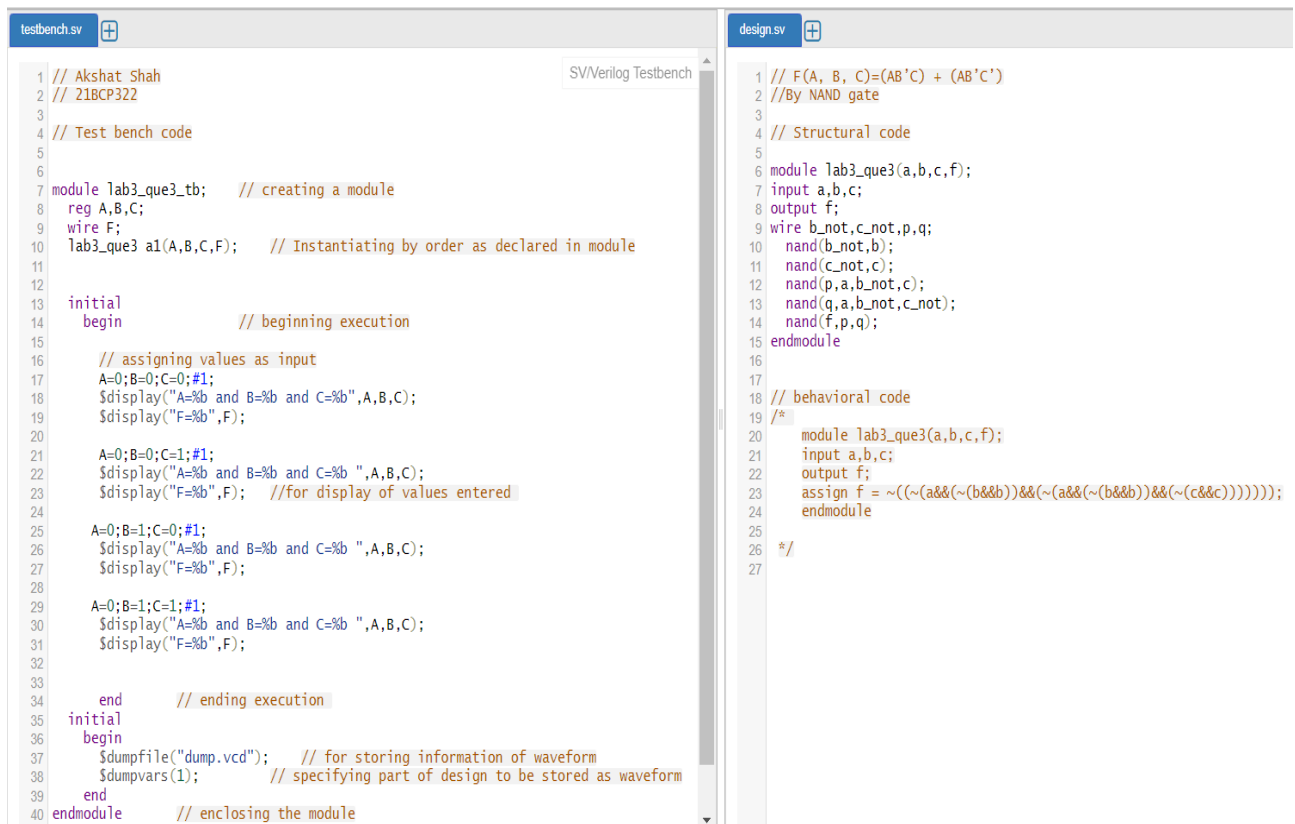
```
testbench.sv
1 // Akshat Shah
2 // 21BCP322
3
4 // Test bench code
5
6 module lab3_que3_tb; // creating a module
7 reg A,B,C,D,E;
8 wire F;
9 lab3_que3 a1(A,B,C,D,E,F); // Instantiating by order as declared in module
10
11 initial
12 begin // beginning execution
13
14 // assigning values as input
15 A=0;B=0;C=0;D=0;E=0;#1;
16 $display("A=%b and B=%b and C=%b and D=%b and E=%b",A,B,C,D,E);
17 $display("F=%b",F);
18
19 A=0;B=0;C=0;D=1;E=0;#1;
20 $display("A=%b and B=%b and C=%b and D=%b and E=%b",A,B,C,D,E);
21 $display("F=%b",F); //for display of values entered
22
23 A=0;B=0;C=0;D=1;E=1;#1;
24 $display("A=%b and B=%b and C=%b and D=%b and E=%b",A,B,C,D,E);
25 $display("F=%b",F);
26
27 A=0;B=0;C=1;D=0;E=0;#1;
28 $display("A=%b and B=%b and C=%b and D=%b and E=%b",A,B,C,D,E);
29 $display("F=%b",F);
30
31 A=0;B=0;C=1;D=0;E=1;#1;
32 $display("A=%b and B=%b and C=%b and D=%b and E=%b",A,B,C,D,E);
33 $display("F=%b",F);
34
35 end // ending execution
36
37 initial
38 begin
39 $dumpfile("dump.vcd"); // for storing information of waveform
40 $dumpvars(1); // specifying part of design to be stored as waveform
41 end
42 endmodule // enclosing the module
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**Question 4:** Implement the following expression using universal NAND and NOR gate. Write down Verilog Structural and Behavioral code for that expression.

$$4.1 F(A, B, C) = (AB'C) + (AB'C')$$

1. By NAND gate

Verilog Code:



```

testbench.vv
1 // Akshat Shah
2 // 21BCP322
3
4 // Test bench code
5
6
7 module lab3_que3_tb; // creating a module
8   reg A,B,C;
9   wire F;
10  lab3_que3 a1(A,B,C,F); // Instantiating by order as declared in module
11
12
13  initial
14      begin // beginning execution
15
16          // assigning values as input
17          A=0;B=0;C=0;#1;
18          $display("A=%b and B=%b and C=%b",A,B,C);
19          $display("F=%b",F);
20
21          A=0;B=0;C=1;#1;
22          $display("A=%b and B=%b and C=%b ",A,B,C);
23          $display("F=%b",F); //for display of values entered
24
25          A=0;B=1;C=0;#1;
26          $display("A=%b and B=%b and C=%b ",A,B,C);
27          $display("F=%b",F);
28
29          A=0;B=1;C=1;#1;
30          $display("A=%b and B=%b and C=%b ",A,B,C);
31          $display("F=%b",F);
32
33      end // ending execution
34  initial
35      begin
36          $dumpfile("dump.vcd"); // for storing information of waveform
37          $dumpvars(1); // specifying part of design to be stored as waveform
38      end
39  endmodule // enclosing the module

```

```

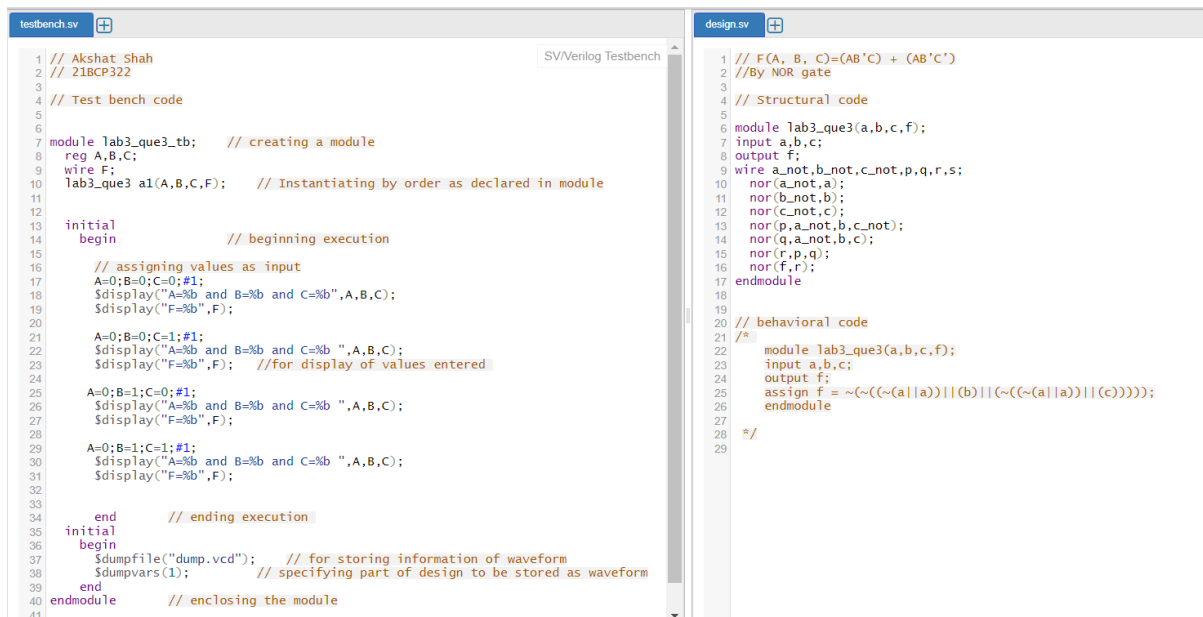
design.vv
1 // F(A, B, C)=(AB'C) + (AB'C')
2 //By NAND gate
3
4 // Structural code
5
6 module lab3_que3(a,b,c,f);
7   input a,b,c;
8   output f;
9   wire b_not,c_not,p,q;
10  nand(b_not,b);
11  nand(c_not,c);
12  nand(p,a,b_not,c);
13  nand(q,a,b_not,c_not);
14  nand(f,p,q);
15 endmodule
16
17
18 // behavioral code
19 /*
20 module lab3_que3(a,b,c,f);
21   input a,b,c;
22   output f;
23   assign f = ~((~(a&&(~(b&&b)))&&(~(a&&(~(b&&b)))&&(~(c&&c)))));
24 endmodule
25
26 */
27

```

Fig 4.1.1- Test bench and design code

## 2. By NOR gate:

### Verilog Code:



```
testbench.v
1 // Akshat Shah
2 // 21BCP322
3
4 // Test bench code
5
6 module lab3_que3_tb; // creating a module
7 reg A,B,C;
8 wire F;
9 lab3_que3 a1(A,B,C,F); // Instantiating by order as declared in module
10
11
12 initial
13 begin // beginning execution
14
15 // assigning values as input
16 A=0;B=0;C=0;#1;
17 $display("A=%b and B=%b and C=%b",A,B,C);
18 $display("F=%b",F);
19
20 A=0;B=0;C=1;#1;
21 $display("A=%b and B=%b and C=%b ",A,B,C);
22 $display("F=%b",F); //for display of values entered
23
24 A=0;B=1;C=0;#1;
25 $display("A=%b and B=%b and C=%b ",A,B,C);
26 $display("F=%b",F);
27
28 A=0;B=1;C=1;#1;
29 $display("A=%b and B=%b and C=%b ",A,B,C);
30 $display("F=%b",F);
31
32 end // ending execution
33
34 initial
35 begin
36 $dumpfile("dump.vcd"); // for storing information of waveform
37 $dumpvars(1); // specifying part of design to be stored as waveform
38 end
39
40 endmodule // enclosing the module
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```

## 4.2 $F(A, B) = A'B' + AB' + A'B + AB$

### 1. By NOR gate

#### Verilog Code:

```
testbench.vv
1 // Akshat Shah
2 // 21BCP322
3
4 // Test bench code
5
6
7 module lab3_que3_tb; // creating a module
8 reg A,B;
9 wire F;
10 lab3_que3 a1(A,B,F); // Instantiating by order as declared in module
11
12
13 initial
14 begin // beginning execution
15
16 // assigning values as input
17 A=0;B=0;#1;
18 $display("A=%b and B=%b",A,B);
19 $display("F=%b",F);
20
21 A=0;B=0;#1;
22 $display("A=%b and B=%b ",A,B);
23 $display("F=%b",F); //for display of values entered
24
25 A=0;B=1;#1;
26 $display("A=%b and B=%b ",A,B);
27 $display("F=%b",F);
28
29 A=0;B=1;#1;
30 $display("A=%b and B=%b ",A,B);
31 $display("F=%b",F);
32
33 end // ending execution
34
35 initial
36 begin
37 $dumpfile("dump.vcd"); // for storing information of waveform
38 $dumpvars(1); // specifying part of design to be stored as waveform
39 end
40 endmodule // enclosing the module

design.vv
1 // F(A, B)= A'B' + AB' + A'B + AB
2 //By NOR gate
3
4 // Structural code
5
6 module lab3_que3(a,b,f);
7 input a,b;
8 output f;
9 wire a_not,b_not,p,q,r,s,t;
10 nor(a_not,a);
11 nor(b_not,b);
12 nor(p,a,b);
13 nor(q,a_not,b);
14 nor(r,a,b_not);
15 nor(s,a_not,b_not);
16 nor(t,p,q,r,s);
17 nor(f,t);
18 endmodule
19
20
21 // behavioral code
22 /*
23 module lab3_que3(a,b,f);
24 input a,b;
25 output f;
26 assign f = ~((~(a|~b))|(~a|~b))|(~(a | b)) | ~(a|b));
27 endmodule
28
29 */
30
```

Fig 4.2.1- Test bench and design code

### 2. By NAND gate:

#### Verilog code:

```
testbench.vv
1 // Akshat Shah
2 // 21BCP322
3
4 // Test bench code
5
6
7 module lab3_que4_tb; // creating a module
8 reg A,B;
9 wire F;
10 lab3_que4 a1(A,B,F); // Instantiating by order as declared in module
11
12
13 initial
14 begin // beginning execution
15
16 // assigning values as input
17 A=0;B=0;#1;
18 $display("A=%b and B=%b",A,B);
19 $display("F=%b",F);
20
21 A=0;B=1;#1;
22 $display("A=%b and B=%b ",A,B);
23 $display("F=%b",F); //for display of values entered
24
25 A=1;B=0;#1;
26 $display("A=%b and B=%b ",A,B);
27 $display("F=%b",F);
28
29 A=1;B=1;#1;
30 $display("A=%b and B=%b ",A,B);
31 $display("F=%b",F);
32
33 end // ending execution
34
35 initial
36 begin
37 $dumpfile("dump.vcd"); // for storing information of waveform
38 $dumpvars(1); // specifying part of design to be stored as waveform
39 end
40 endmodule // enclosing the module

design.vv
1 // F(A,B) = A'B' + AB' + A'B + AB
2 //Structural Code
3
4 module lab3_que4(a,b,f);
5
6 input a,b;
7 output f;
8 wire p,q,r,s;
9 nand(a_not,a);
10 nand(b_not,b);
11 nand(p,a_not,b_not);
12 nand(q,a,b_not);
13 nand(r,a_not,b);
14 nand(s,a,b);
15 nand(f,p,q,r,s);
16 endmodule
17
18 /*
19 Behavioral Code
20 module lab3_que4(a,b,f);
21 input a,b;
22 output f;
23 assign f= ~((~(a&b)) & ~(a&b)) & ~(a&b)) & ~(a&b));
24
25 */
26
27
28
```



### Output:

A=0 and B=0  
F=1  
A=0 and B=0  
F=1  
A=0 and B=1  
F=1  
A=0 and B=1  
F=1

Fig 4.2.2 Output as truth table

### Waveform:

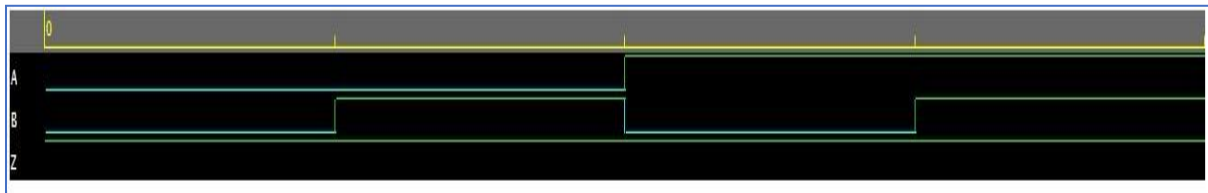
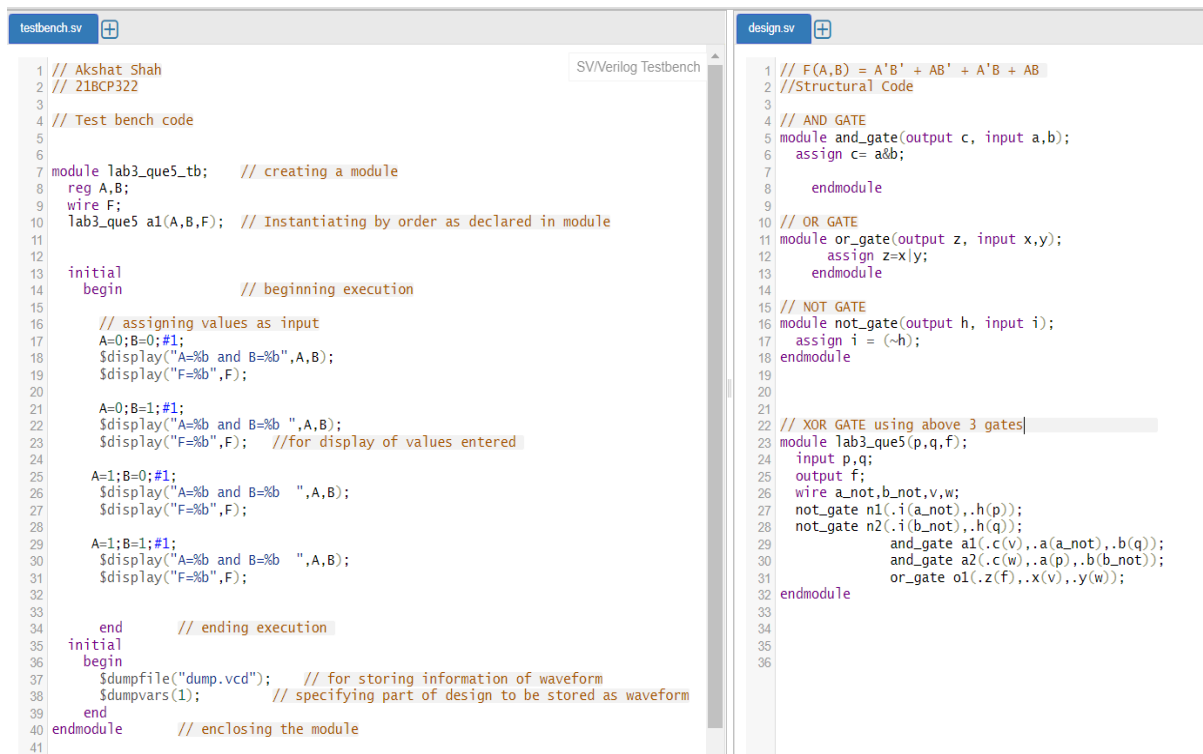


Fig 4.2.3- Waveform of output

**Question 5:** Write down three modules in a single Verilog code to design AND, OR and NOT gate . Now use those modules to design the XOR gate. Use AND, OR and NOT gate as the instances to implement the XOR gate. Write the corresponding Testbench code for the verification of your XOR gate.

Verilog Code:



```

testbench.vv
1 // Akshat Shah
2 // 218CP322
3
4 // Test bench code
5
6
7 module lab3_que5_tb; // creating a module
8   reg A,B;
9   wire F;
10  lab3_que5 a1(A,B,F); // Instantiating by order as declared in module
11
12
13  initial
14  begin
15      // beginning execution
16
17      // assigning values as input
18      A=0;B=0;#1;
19      $display("A=%b and B=%b",A,B);
20      $display("F=%b",F);
21
22      A=0;B=1;#1;
23      $display("A=%b and B=%b ",A,B);
24      $display("F=%b",F); //for display of values entered
25
26      A=1;B=0;#1;
27      $display("A=%b and B=%b ",A,B);
28      $display("F=%b",F);
29
30      A=1;B=1;#1;
31      $display("A=%b and B=%b ",A,B);
32      $display("F=%b",F);
33
34  end // ending execution
35  initial
36  begin
37      $dumpfile("dump.vcd"); // for storing information of waveform
38      $dumpvars(1); // specifying part of design to be stored as waveform
39  end
40 endmodule // enclosing the module
41
design.vv
1 // F(A,B) = A'B' + AB' + A'B + AB
2 //Structural Code
3
4 // AND GATE
5 module and_gate(output c, input a,b);
6   assign c= a&b;
7
8   endmodule
9
10 // OR GATE
11 module or_gate(output z, input x,y);
12   assign z=x|y;
13   endmodule
14
15 // NOT GATE
16 module not_gate(output h, input i);
17   assign i = (~h);
18 endmodule
19
20
21
22 // XOR GATE using above 3 gates
23 module lab3_que5(p,q,f);
24   input p,q;
25   output f;
26   wire a_not,b_not,v,w;
27   not_gate n1(.i(a_not),.h(p));
28   not_gate n2(.i(b_not),.h(q));
29   and_gate a1(.c(v),.a(a_not),.b(q));
30   and_gate a2(.c(w),.a(p),.b(b_not));
31   or_gate o1(.z(f),.x(v),.y(w));
32 endmodule
33
34
35
36

```

Fig 5.1- Test bench and design code

Output:

```

A=0 and B=0
F=0
A=0 and B=1
F=1
A=1 and B=0
F=1
A=1 and B=1
F=0

```

Fig 5.2- Output as truth table

Waveform:

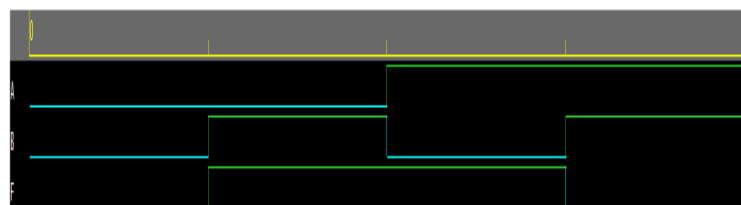


Fig 5.3- Waveform of output

Question 6: Consider the following expression:

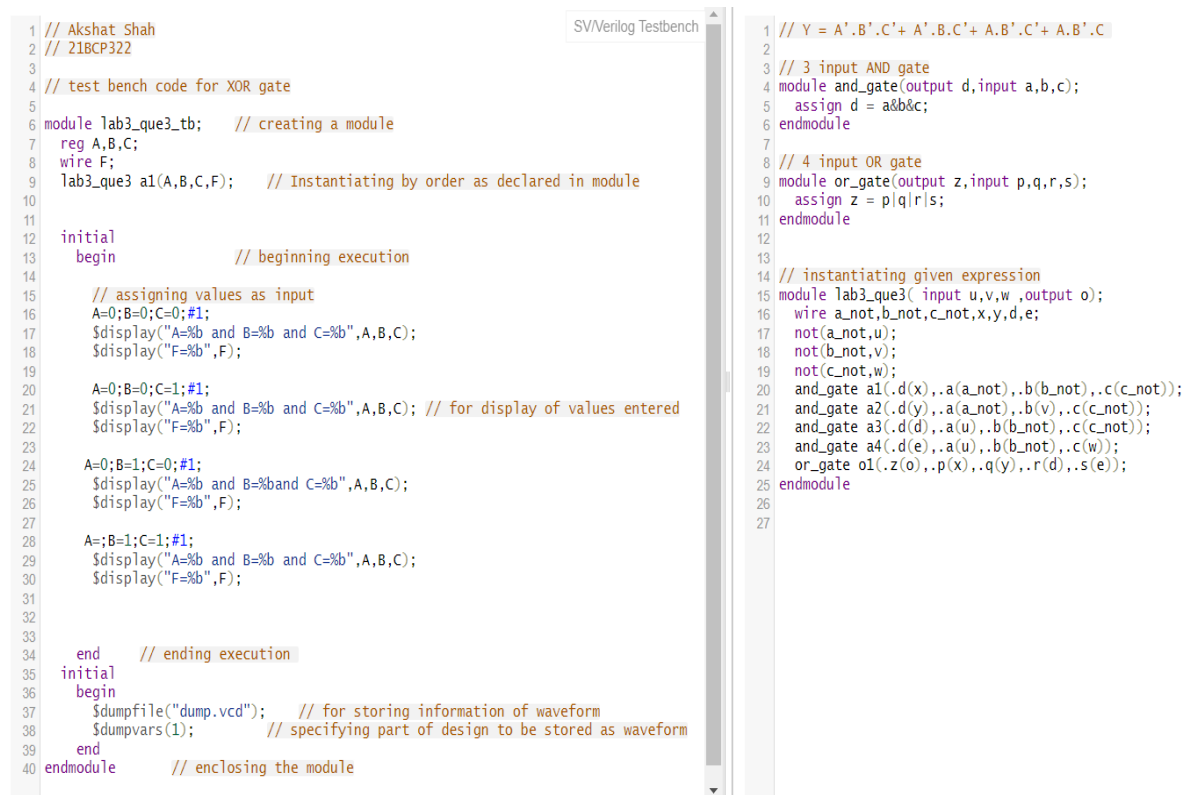
$$Y = A'.B'.C' + A'.B.C' + A.B'.C' + A.B'.C$$

- (i) Generate the Truth Table manually for the same.
- (ii) Design one three input 'And' gate module and one four input 'OR' gate module using Verilog. Instantiate those two modules to design the above-mentioned expression. Design the corresponding TestBench code for the verification purpose.
- (iii) Now Minimize the given expression.
- (iv) Design again 'AND' gate and 'OR' gate module with required number of inputs and instantiate them to implement the minimized expression. Design the corresponding Test Bench code for the verification purpose.

(i) Truth table:

A	B	C	A'B'C'	A'BC'	AB'C'	AB'C	Y
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	0
0	1	0	0	1	0	0	1
0	1	1	0	0	1	0	1
1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0

## (ii) Verilog Code:



```

1 // Akshat Shah
2 // 21BCP322
3
4 // test bench code for XOR gate
5
6 module lab3_que3_tb;    // creating a module
7     reg A,B,C;
8     wire F;
9     lab3_que3 a1(A,B,C,F);    // Instantiating by order as declared in module
10
11
12     initial
13     begin                // beginning execution
14
15         // assigning values as input
16         A=0;B=0;C=0;#1;
17         $display("A=%b and B=%b and C=%b",A,B,C);
18         $display("F=%b",F);
19
20         A=0;B=0;C=1;#1;
21         $display("A=%b and B=%b and C=%b",A,B,C); // for display of values entered
22         $display("F=%b",F);
23
24         A=0;B=1;C=0;#1;
25         $display("A=%b and B=%band C=%b",A,B,C);
26         $display("F=%b",F);
27
28         A=1;B=1;C=1;#1;
29         $display("A=%b and B=%b and C=%b",A,B,C);
30         $display("F=%b",F);
31
32
33     end                // ending execution
34     initial
35     begin
36         $dumpfile("dump.vcd");    // for storing information of waveform
37         $dumpvars(1);    // specifying part of design to be stored as waveform
38     end
39 endmodule    // enclosing the module

```

```

1 // Y = A'.B'.C' + A'.B.C' + A.B'.C' + A.B.C
2
3 // 3 input AND gate
4 module and_gate(output d,input a,b,c);
5     assign d = a&b&c;
6 endmodule
7
8 // 4 input OR gate
9 module or_gate(output z,input p,q,r,s);
10    assign z = p|q|r|s;
11 endmodule
12
13 // instantiating given expression
14 module lab3_que3( input u,v,w ,output o);
15     wire a_not,b_not,c_not,x,y,d,e;
16     not(a_not,u);
17     not(b_not,v);
18     not(c_not,w);
19     and_gate a1(.d(x),.a(a_not),.b(b_not),.c(c_not));
20     and_gate a2(.d(y),.a(a_not),.b(v),.c(c_not));
21     and_gate a3(.d(d),.a(u),.b(b_not),.c(c_not));
22     and_gate a4(.d(e),.a(u),.b(b_not),.c(w));
23     or_gate o1(.z(o),.p(x),.q(y),.r(d),.s(e));
24 endmodule
25
26
27

```

Fig 6.1- Test bench and design code

Output:

```

a=0, b=0, c=0
y=1
a=0, b=0, c=1
y=0
a=0, b=1, c=0
y=1
a=0, b=1, c=1
y=0

```

Fig 6.2- Output as truth table

(iii) Minimal Expression:  $Y = A'C' + AB'$

#### (iv) Verilog Code:

```
1 // Akshat Shah
2 // 21BCP322
3
4 // test bench code for XOR gate
5
6 module lab3_que6_tb; // creating a module
7     reg A,B,C;
8     wire F;
9     lab3_que6 a1(A,B,C,F); // Instantiating by order as declared in module
10
11
12     initial
13     begin // beginning execution
14
15         // assigning values as input
16         A=0;B=0;C=0;#1;
17         $display("A=%b and B=%b and C=%b",A,B,C);
18         $display("F=%b",F);
19
20         A=0;B=0;C=1;#1;
21         $display("A=%b and B=%b and C=%b",A,B,C); // for display of values entered
22         $display("F=%b",F);
23
24         A=0;B=1;C=0;#1;
25         $display("A=%b and B=%band C=%b",A,B,C);
26         $display("F=%b",F);
27
28         A=0;B=1;C=1;#1;
29         $display("A=%b and B=%b and C=%b",A,B,C);
30         $display("F=%b",F);
31
32
33     end // ending execution
34
35     initial
36     begin
37         $dumpfile("dump.vcd"); // for storing information of waveform
38         $dumpvars(1); // specifying part of design to be stored as waveform
39     end
40 endmodule // enclosing the module
```

```
1 module and_gate(input a,b, output c);
2     assign c = a & b;
3 endmodule
4
5 module or_gate(input x,y, output z);
6     assign z= x|y;
7 endmodule
8
9 module not_gate(input h, output i);
10    assign i = ~h;
11 endmodule
12
13 module lab3_que6(u,v,w,o);
14     input u,v,w;
15     output o;
16
17     wire u_not,v_not,w_not,p,q;
18     not_gate n1(u,u_not);
19     not_gate n2(v,v_not);
20     not_gate n3(w,w_not);
21
22     and_gate a1(u,v_not,q);
23     and_gate a2(u_not,w_not,p);
24     or_gate o1(q,p,o);
25 endmodule
26
```

Fig 6.3- Test bench and design code

#### Output:

```
A=0 and B=0 and C=0
F=1
A=0 and B=0 and C=1
F=0
A=0 and B=1and C=0
F=1
A=0 and B=1 and C=1
F=0
```

Fig 6.4- Output as truth table

#### Waveform:

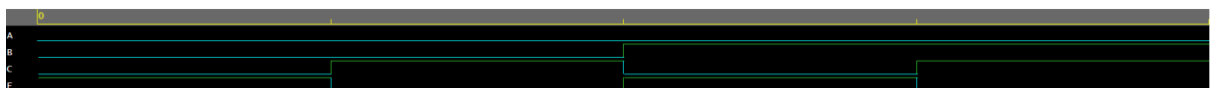


Fig 6.5- Waveform of output

