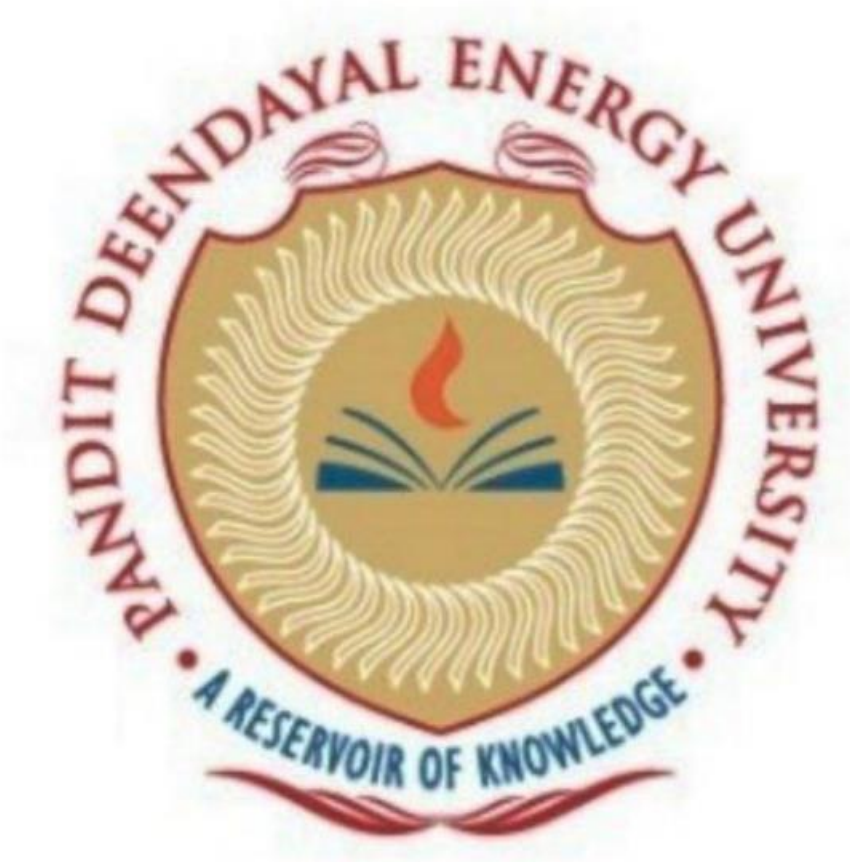
Name - Akshat Shah

Roll No - 21BCP322

Sem – III

Digital Electronics and Computer Organization Lab

Course Code – 20CP203P



Department of Computer Science Engineering
School of Technology,
Pandit Deendayal Energy University

Date: 07-09-2022

Assignment-4

Aim: To implement Combinational circuits of half adder and full adders

Table of Contents

List of Questions:

Question 1: Write Verilog code for half adder. Test using waveform.

Verilog Code:

Design Code:

```
module HA(input a,b,output carry,sum);
assign sum=a^b;
assign carry=a&b;
endmodule
```

Test bench Code:

```
module tb_HA;
reg A,B; wire C,S;
HA  a1(A,B,C,S);
initial
begin
    A=0;B=0; #1;
    $display("a=%b and b=%b",A,B);
    $display("c=%b",C);
    $display("s=%b",S); A=0;B=1; #1;
    $display("a=%b and b=%b",A,B);
    $display("c=%b",C);
    $display("s=%b",S); A=1;B=0; #1;
    $display("a=%b and b=%b",A,B);
    $display("c=%b",C);
    $display("s=%b",S); A=1;B=1; #1;
    $display("a=%b and b=%b",A,B);

    $display("c=%b",C);
    $display("s=%b",S);
     end
```

```
 initial begin
$dumpfile("dump.vcd");
$dumpvars(1);
 end
endmodule
```

Output:

```
[2022-09-07 09:57:24 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0 and b=0
c=0
s=0
a=0 and b=1
c=0
s=1
a=1 and b=0
c=0
s=1
a=1 and b=1
c=1
s=0
Finding VCD file...
./dump.vcd
[2022-09-07 09:57:24 EDT] Opening EPWave...
Done
```

Fig 1.1.2 - Output as Truth table

Waveform:

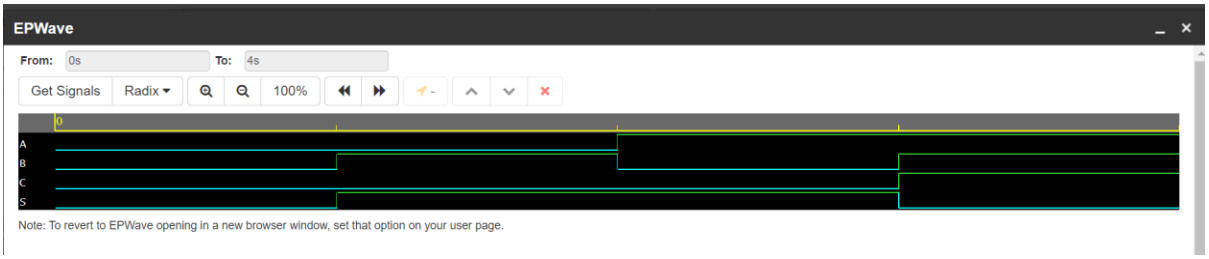
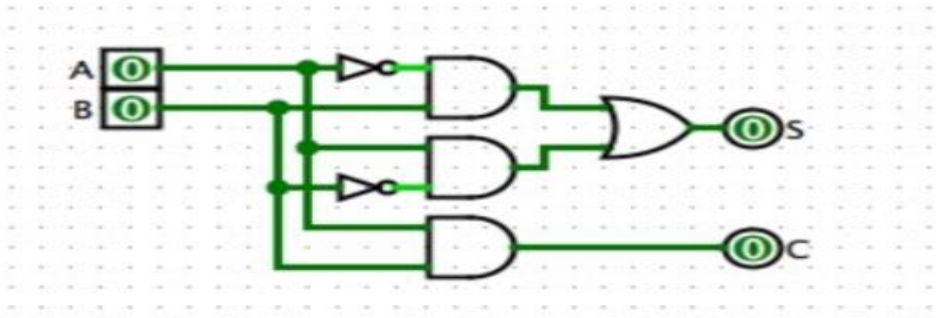


Fig 1.1.3- Waveform for output

Circuit diagram:



Question 2. Write Verilog code for full adder. Test using waveform.

Verilog Code:

Design Code:

```
module FA(input a,b,c_in,output sum,c_out);
assign sum=a^b^c_in;
assign  c_out=((a^b)&c_in)|(a&b);
endmodule
```

Test bench code:

```
module tb_FA;
reg A,B,C; wire S,Co;
FA  f1(A,B,C,S,Co);
initial begin
A=0;B=0;C=0;#1;
$display("A=%b and B=%b and C=%b",A,B,C);
$display("s=%b",S);
$display("carry=%b",Co);
        A=0;B=1;C=0;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",S);
        $display("carry=%b",Co);

        A=0;B=1;C=1;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",S);
        $display("carry=%b",Co);

        A=1;B=0;C=0;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",S);
        $display("carry=%b",Co);

        A=1;B=0;C=1;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",S);
        $display("carry=%b",Co);
```

```
        A=1;B=1;C=0;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",S);
        $display("carry=%b",Co);

        A=1;B=1;C=1;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",S);
        $display("carry=%b",Co);
      end

  initial begin
        $dumpfile("dump.vcd");
        $dumpvars(1);
      End
       endmodule
```

Output:

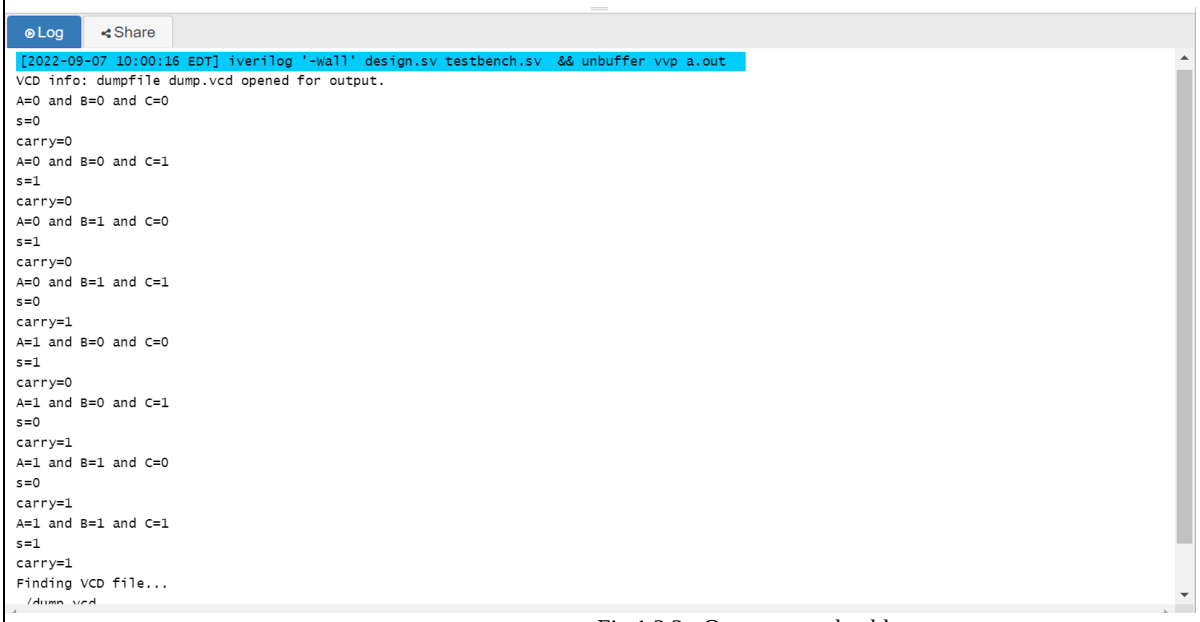


Fig 1.2.2 - Output as truth table

Waveform:

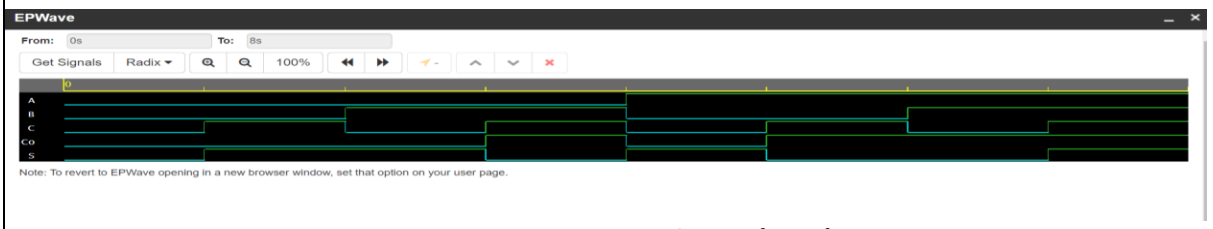
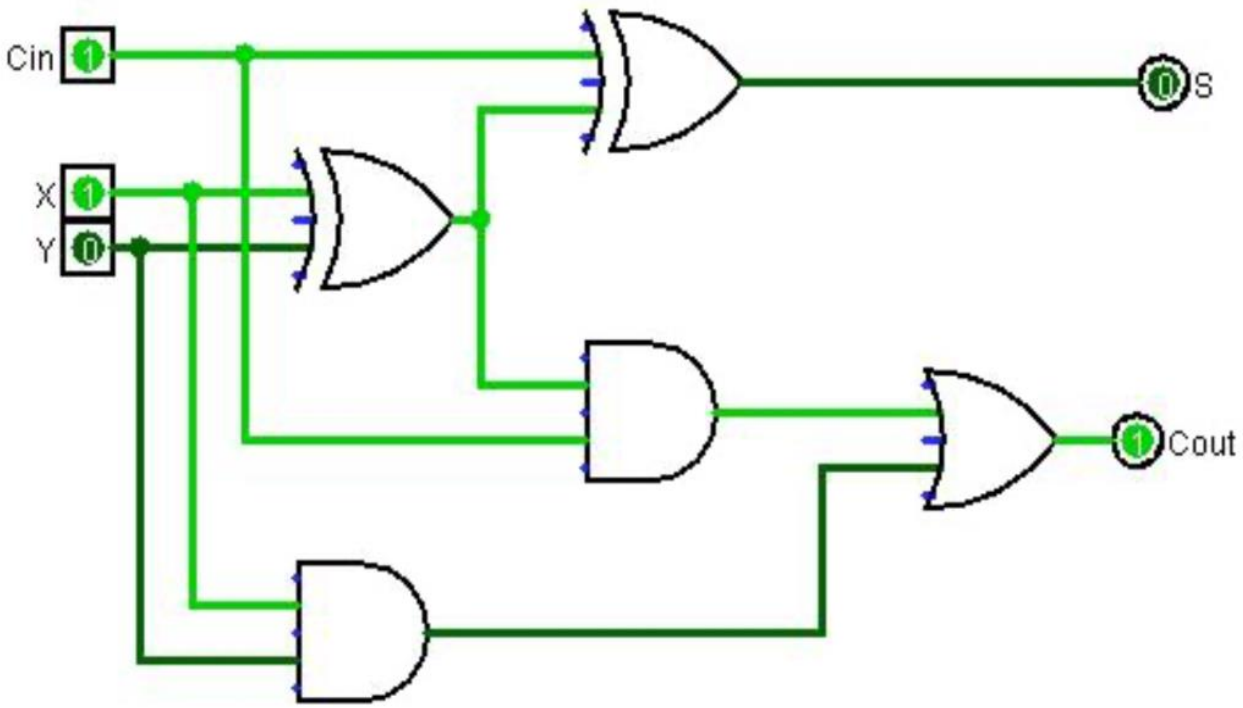


Fig 1.2.3- Waveform of output

Circuit diagram:



Question 4. Write Verilog code for full adder using module instantiation of half adder. Test using waveform.

Verilog Code:

Design Code:

```
module HA(input a,b,output s,c);
  assign s=a^b;
  assign c=a&b; endmodule
  module FA(input p,q,r,output sum,carry); wire s1,c1,c2;
  HA  h1(p,q,s1,c1);
  HA  h2(s1,r,sum,c2);
  or(carry,c1,c2);
  endmodule
```

Test bench Code:

```
module   tb_FA;
 reg   A,B,C; wire SUM,CARRY;
  FA  f1(A,B,C,SUM,CARRY);
  initial begin
        A=0;B=0;C=0;#1;
      $display("A=%b and B=%b and C=%b",A,B,C);
      $display("s=%b",SUM);
      $display("carry=%b",CARRY);

      A=0;B=0;C=1;#1;
      $display("A=%b and B=%b and C=%b",A,B,C);
      $display("s=%b",SUM);
      $display("carry=%b",CARRY);

      A=0;B=1;C=0;#1
      $display("A=%b and B=%b and C=%b",A,B,C);
```

```
        $display("s=%b",SUM);
        $display("carry=%b",CARRY);

        A=0;B=1;C=1;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",SUM);
        $display("carry=%b",CARRY);

        A=1;B=0;C=0;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",SUM);
        $display("carry=%b",CARRY);

        A=1;B=0;C=1;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",SUM);
        $display("carry=%b",CARRY);

        A=1;B=1;C=0;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",SUM);
        $display("carry=%b",CARRY);

        A=1;B=1;C=1;#1;
        $display("A=%b and B=%b and C=%b",A,B,C);
        $display("s=%b",SUM);
        $display("carry=%b",CARRY); end

initial begin
$dumpfile("dump.vcd");
```

```
$dumpvars(1); end

endmodule
```

Output:

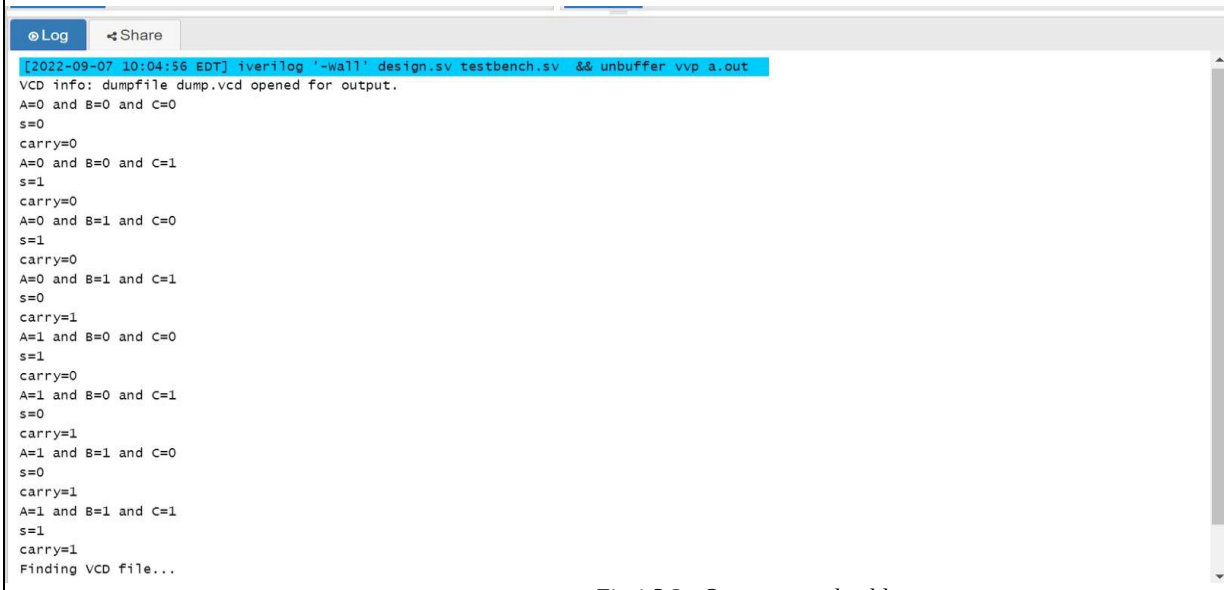


Fig 1.3.2 - Output as truth table

Waveform:

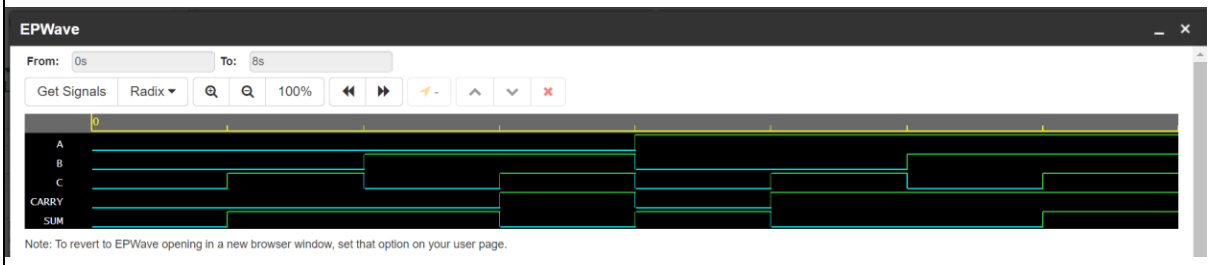


Fig 1.3.3- Waveform of full adder

Question 5. Write Verilog code for half adder using only NAND gate. Test using waveform.

Verilog Code:

Design Code:

```
module HA(input a,b,output sum,carry);
wire a_not,b_not,x,y;
nand(a_not,a); nand(b_not,b);
nand(x,a_not,b);
nand(y,a,b_not);
nand(sum,x,y);
nand(carry,z);       //  Calculating Carry
endmodule
```

Testbench Code:

```
module tb_FA; reg  A,B;
   wire SUM,CARRY;
   HA  f1(A,B,SUM,CARRY);
   initial begin
        A=0;B=0; #1;
        $display("a=%b and b=%b",A,B);
        $display("c=%b",CARRY);
        $display("s=%b",SUM); A=0;B=1; #1;
        $display("a=%b  and  b=%b",A,B);
        $display("c=%b",CARRY);
        $display("s=%b",SUM); A=1;B=0; #1;
        $display("a=%b and b=%b",A,B);
        $display("c=%b",CARRY);
        $display("s=%b",SUM);
        A=1;B=1; #1;
        $display("a=%b and b=%b",A,B);
        $display("c=%b",CARRY);
        $display("s=%b",SUM);
```

```
        end
        initial begin
        $dumpfile("dump.vcd");
        $dumpvars(1); end
      endmodule
```

Output:

```
Log  Share
[2022-09-07 10:10:19 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
design.sv:10: warning: implicit definition of wire logic tb_FA.f1.z.
VCD info: dumpfile dump.vcd opened for output.
a=0 and b=0
c=0
s=0
a=0 and b=1
c=0
s=1
a=1 and b=0
c=0
s=1
a=1 and b=1
c=1
s=0
Finding VCD file...
./dump.vcd
[2022-09-07 10:10:19 EDT] Opening EPWave...
Done
```

Fig 1.4.2- output as truth table

Waveform:

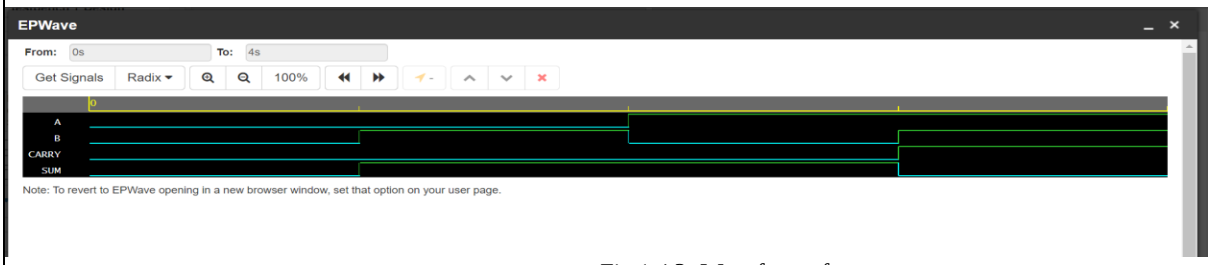
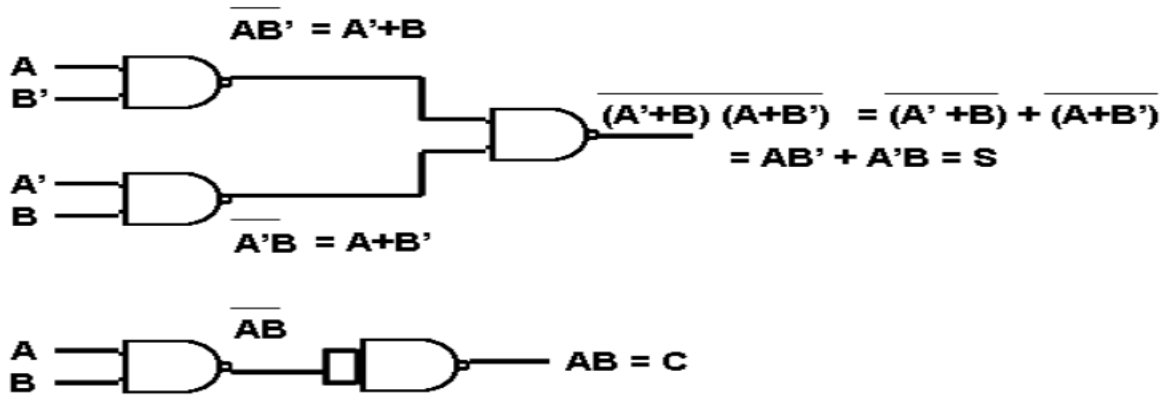


Fig 1.4.3- Waveform of output

Circuit diagram:



Question 6. Write Verilog code for half adder using only NOR gate. Test using waveform.

Verilog Code:

Design Code:

```
module HA(input a,b,output sum,carry);
wire  a_not,b_not,x,y,w;
   nor(a_not,a);
   nor(b_not,b);
   nor(x,a,b_not);
   nor(y,a_not,b);
   nor(w,x,y);
   nor(sum,w);
   nor(carry,a_not,b_not);
   endmodule
```

Test bench Code:

```
module tb_FA;
   reg A,B;
   wire SUM,CARRY;
   HA  f1(A,B,SUM,CARRY);
   initial
   begin
        A=0;B=0; #1;
        $display("a=%b and b=%b",A,B);
        $display("c=%b",CARRY);
        $display("s=%b",SUM);

        A=0;B=1; #1;
        $display("a=%b and b=%b",A,B);
        $display("c=%b",CARRY);
        $display("s=%b",SUM);
```

```
    A=1;B=0; #1;
    $display("a=%b and b=%b",A,B);
    $display("c=%b",CARRY);
    $display("s=%b",SUM);
    A=1;B=1; #1;
    $display("a=%b and b=%b",A,B);
    $display("c=%b",CARRY);
    $display("s=%b",SUM); end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars(1); end
  endmodule
```

Output:

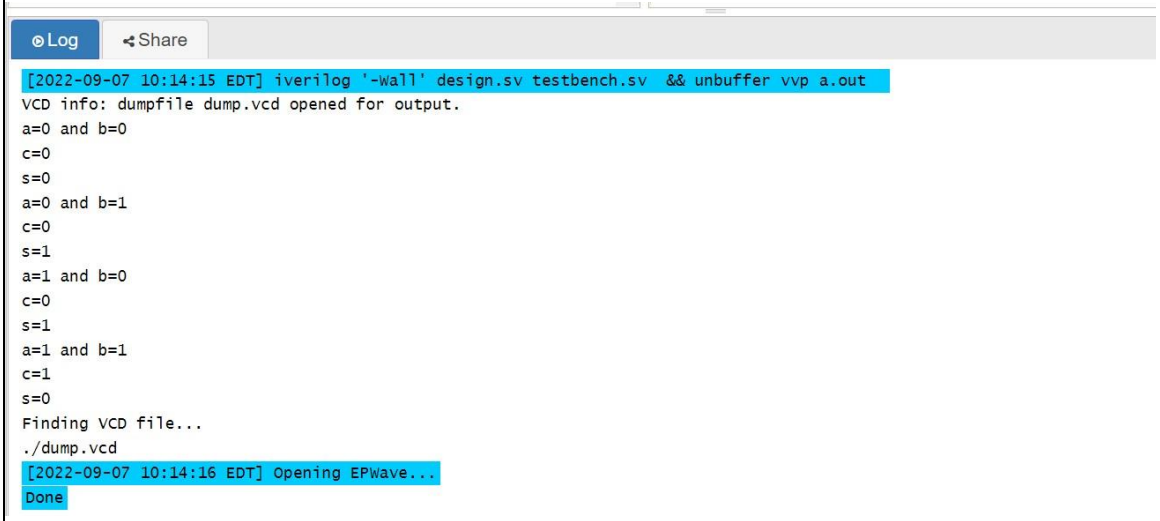


Fig 1.5.2- Output as truth table

Waveform:

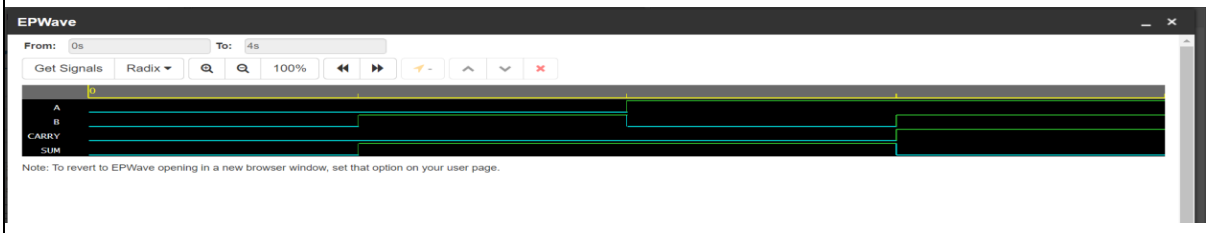
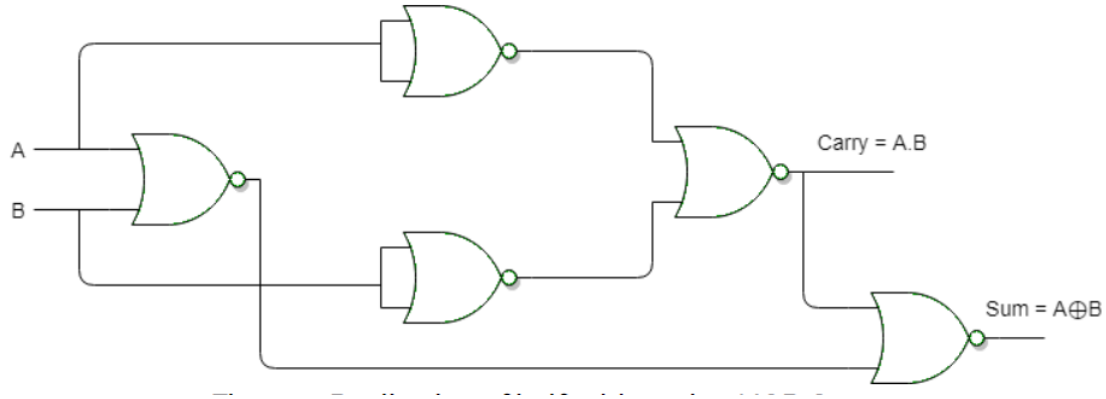


Fig 1.5.3- Waveform of output

Circuit diagram:



Half adder using NOR gates