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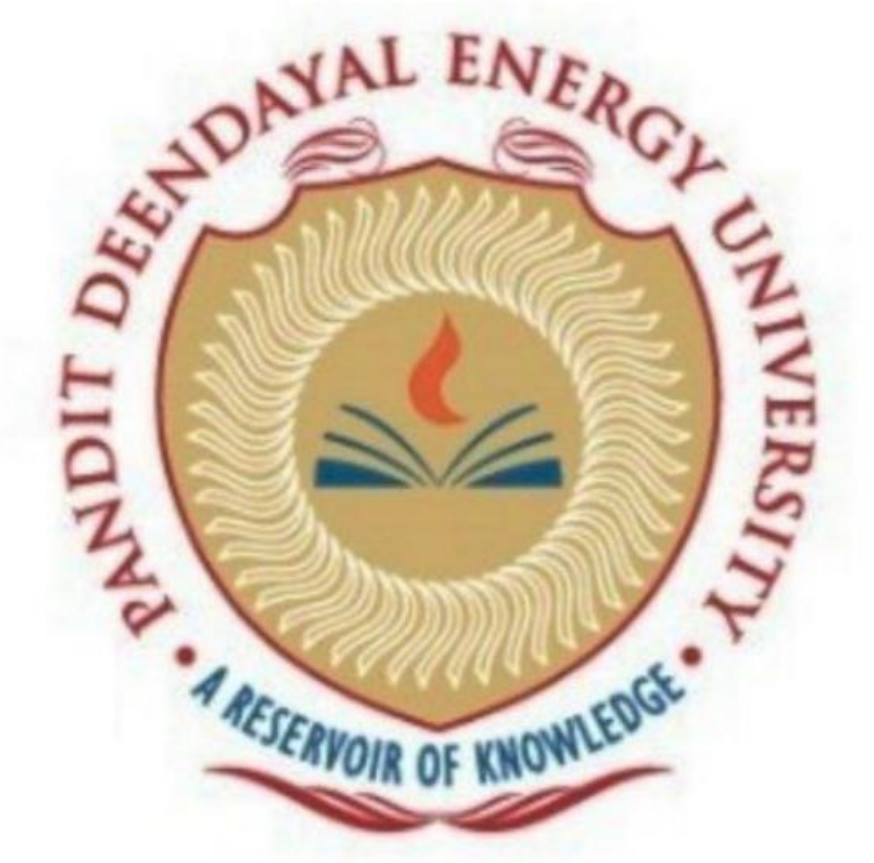
Sem – III

Digital Electronics and Computer Organization Lab

Course Code – 20CP203P

Department of CSE



Assignment-1

EXERCISE 1: Design the following logic functions using basic gates and test the output using truth table.

1.1: Y = ABC + DE + F

CIRCUIT DIAGRAM:

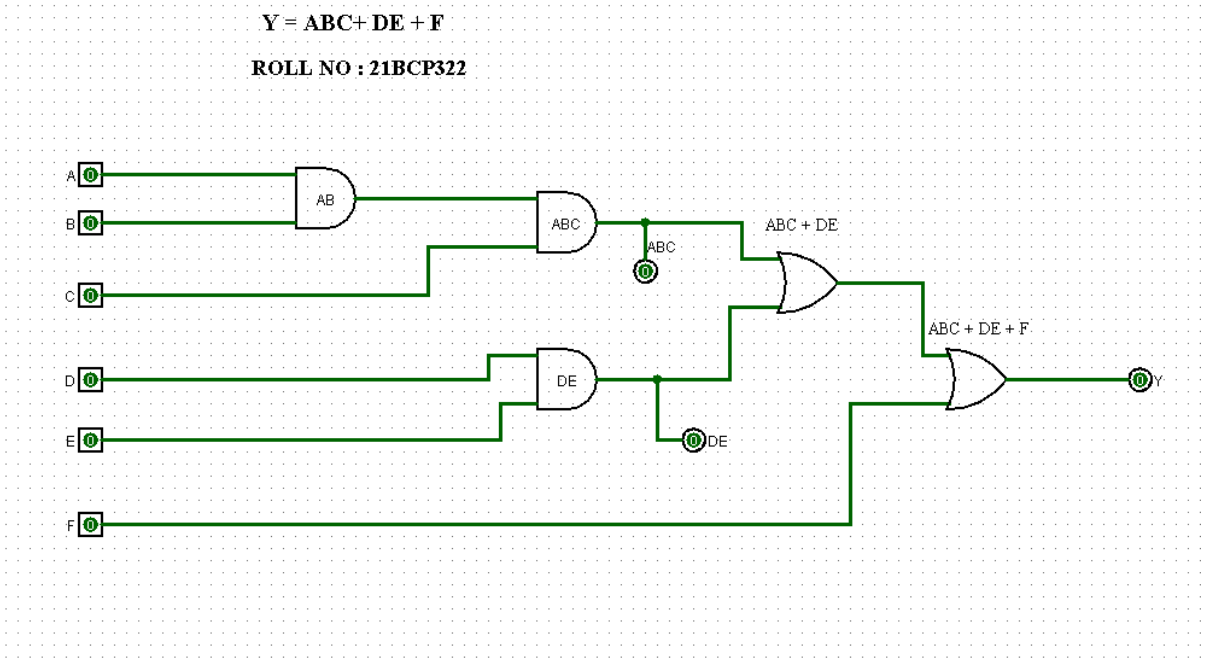


Figure 1.1 Digital Circuit representing Y = ABC + DE + F

Truth table:

A	B	C	D	E	F	ABC	Y	DE
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	0	0
0	0	0	0	1	1	0	1	0
0	0	0	1	0	0	0	0	0

0	0	0	1	0	1	0	1	0
0	0	0	1	1	0	0	1	1
0	0	0	1	1	1	0	1	1
0	0	1	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0
0	0	1	0	1	0	0	0	0
0	0	1	0	1	1	0	1	0
0	0	1	1	0	0	0	0	0
0	0	1	1	0	1	0	1	0
0	0	1	1	1	0	0	1	1
0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	0
0	1	0	0	1	1	0	1	0
0	1	0	1	0	0	0	0	0
0	1	0	1	0	1	0	1	0
0	1	0	1	1	0	0	1	1
0	1	0	1	1	1	0	1	1
0	1	1	0	0	0	0	0	0
0	1	1	0	0	1	0	1	0
0	1	1	0	1	0	0	0	0
0	1	1	0	1	1	0	1	0
0	1	1	1	0	0	0	0	0
0	1	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1	1
0	1	1	1	1	1	0	1	1
1	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	0
1	0	0	0	1	0	0	0	0
1	0	0	0	1	1	0	1	0
1	0	0	1	0	0	0	0	0
1	0	0	1	0	1	0	1	0
1	0	0	1	1	0	0	1	1
1	0	0	1	1	1	0	1	1
1	0	1	0	0	0	0	0	0
1	0	1	0	0	1	0	1	0
1	0	1	0	1	0	0	0	0
1	0	1	0	1	1	0	1	0
1	0	1	1	0	0	0	0	0
1	0	1	1	0	1	0	1	0
1	0	1	1	1	0	0	1	1
1	0	1	1	1	1	0	1	1
1	1	0	0	0	0	0	0	0
1	1	0	0	0	1	0	1	0
1	1	0	0	1	0	0	0	0
1	1	0	0	1	1	0	1	0
1	1	0	1	0	0	0	0	0
1	1	0	1	0	1	0	1	0
1	1	0	1	1	0	0	1	1

1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	0
1	1	1	0	0	1	1	1	0
1	1	1	0	1	0	1	1	0
1	1	1	0	1	1	1	1	0
1	1	1	1	0	0	1	1	0
1	1	1	1	0	1	1	1	0
1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1

Table 1.1 Representing Truth table of **Y = ABC + DE + F**

1.2: Z = A’B’ + AB’ + A’B + AB

CIRCUIT DIAGRAM -:

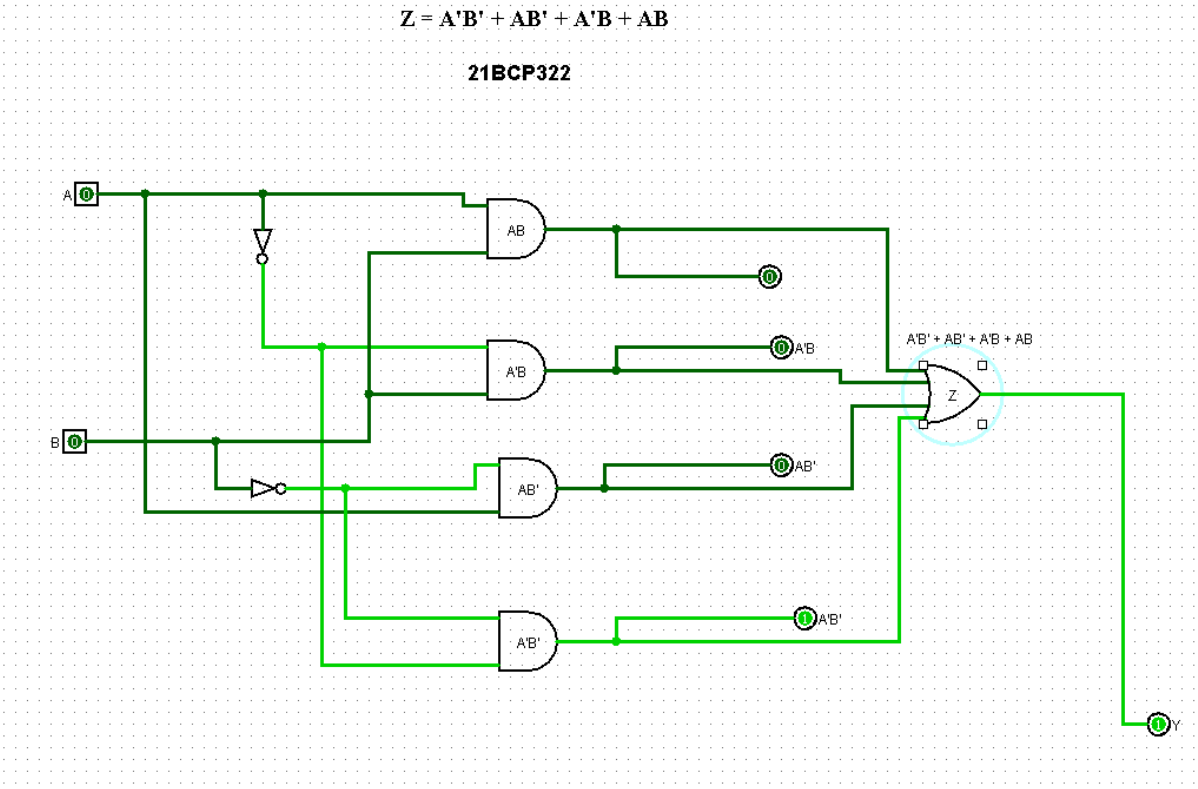


Figure 1.2 Representing Circuit of Z = A’B’ + AB’ + A’B + AB

Truth table:

A	B	AB	AB’	A’B	A’B’	Y
0	0	0	0	0	1	1
0	1	0	1	0	0	1
1	0	0	0	1	0	1
1	1	1	0	0	0	1

Table 1.2 Representing truth table of Z = A’B’ + AB’ + A’B + AB

1.3: K = (A’+B’) (A+B’) (A’+B) (A+B)

CIRCUIT DIAGRAM:

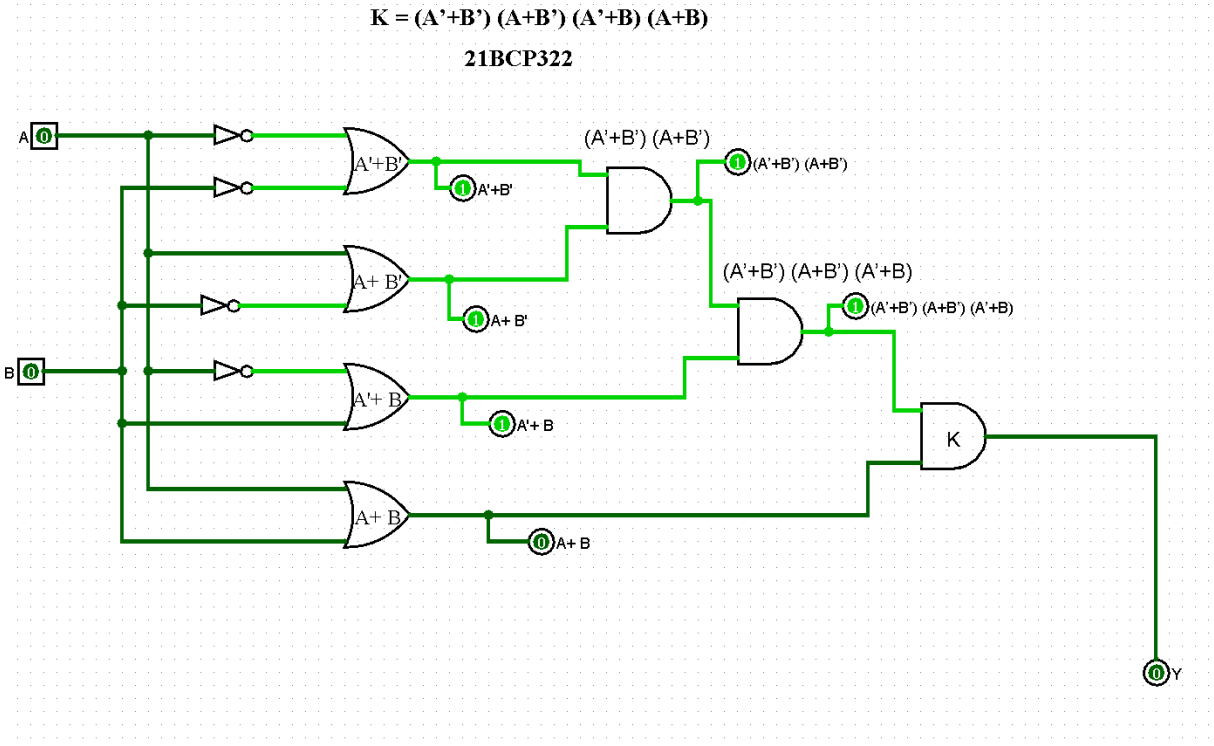


Figure 1.3 Representing Circuit of K = (A’+B’) (A+B’) (A’+B) (A+B)

Truth table:

A	B	ABAB	AB	ABABAB	AB2	AB3	AB4	Y
0	0	1	1	1	1	1	0	0
0	1	0	1	0	0	1	1	0

1	0	1	1	0	1	0	1	0
1	1	0	0	0	1	1	1	0

EXERCISE 2: Design the verify the functionality using existing library of basic gates in Logisim.

2.1: Y = ((A+B).(C+D+E))’

CIRCUIT DIAGRAM -:

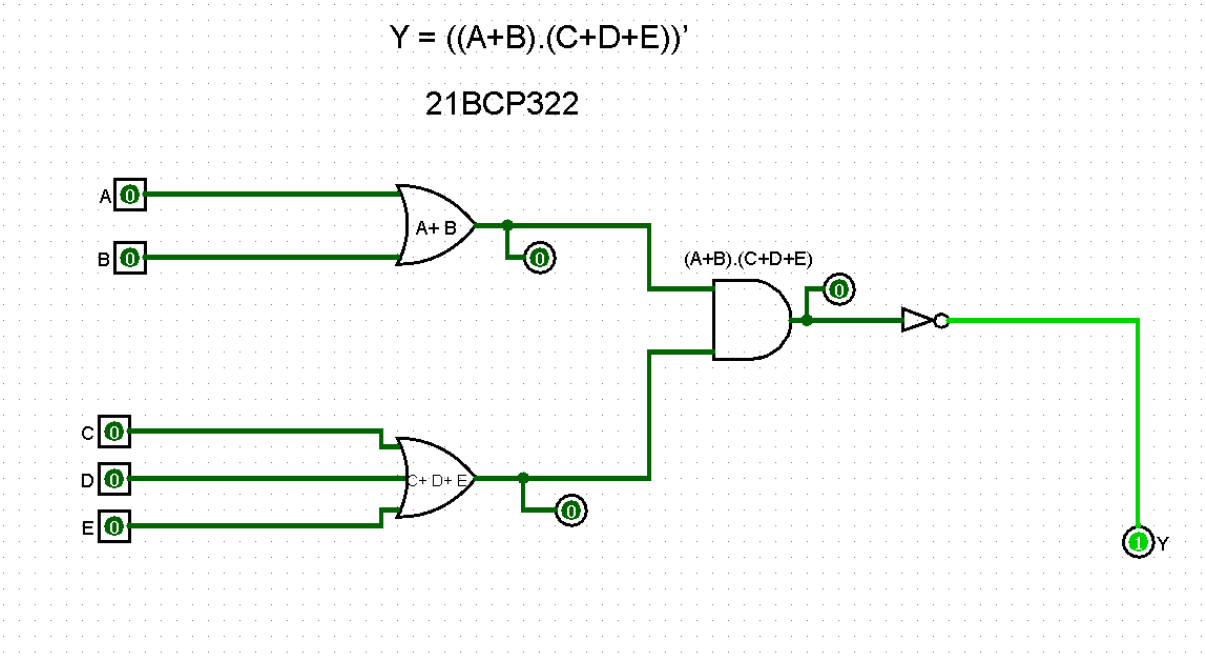


Figure 2.1 Representing Circuit of Y = ((A+B).(C+D+E))’

Truth table:

A	B	C	D	E	x	y	z	Y
0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1	1
0	0	0	1	0	0	0	1	1
0	0	0	1	1	0	0	1	1
0	0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1	1
0	0	1	1	0	0	0	1	1
0	0	1	1	1	0	0	1	1
0	1	0	0	0	1	0	0	1

0	1	0	0	1	1	1	1	0
0	1	0	1	0	1	1	1	0
0	1	0	1	1	1	1	1	0
0	1	1	0	0	1	1	1	0
0	1	1	0	1	1	1	1	0
0	1	1	1	0	1	1	1	0
0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	0	0	1
1	0	0	0	1	1	1	1	0
1	0	0	1	0	1	1	1	0
1	0	0	1	1	1	1	1	0
1	0	1	0	0	1	1	1	0
1	0	1	0	1	1	1	1	0
1	0	1	1	0	1	1	1	0
1	0	1	1	1	1	1	1	0
1	1	0	0	0	1	0	0	1
1	1	0	0	1	1	1	1	0
1	1	0	1	0	1	1	1	0
1	1	0	1	1	1	1	1	0
1	1	1	0	0	1	1	1	0
1	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0

Table 2.1 Represents truth table of Y = ((A+B).(C+D+E))’

2.2 F = ((A.B’)’+(A’B’)’)’

Circuit diagram:

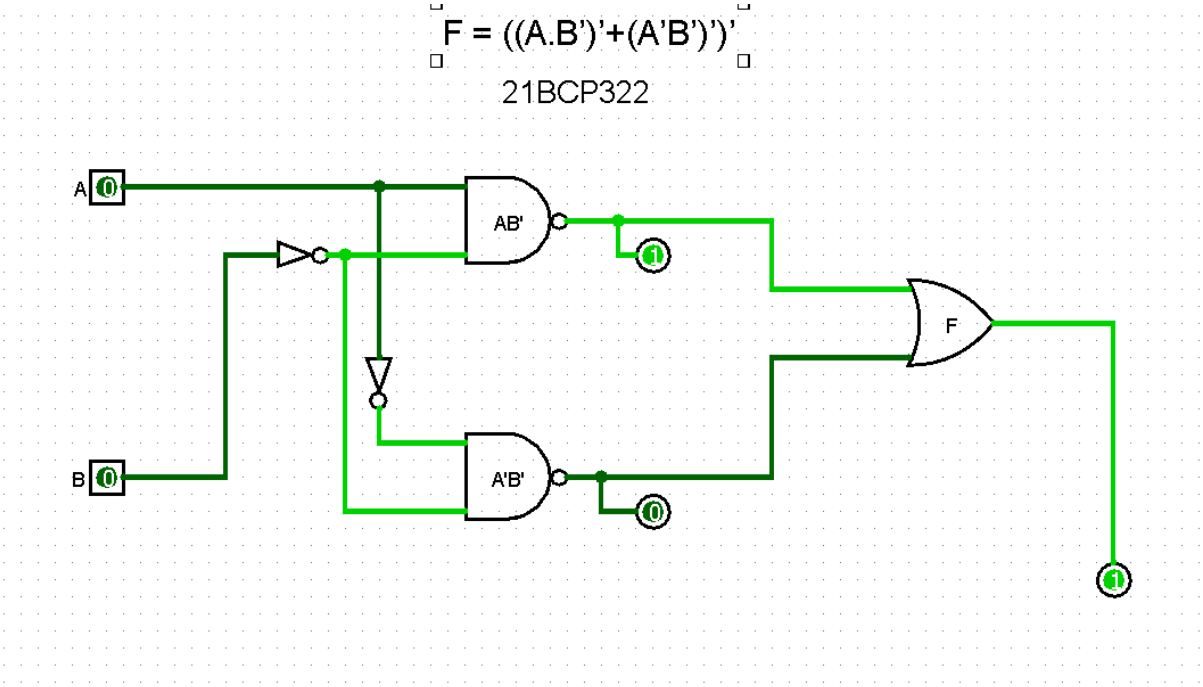


Figure 2.2 Representing Circuit of F = ((A.B')'+(A'B')')'

Truth table:

A	B	x	y	z
0	0	1	0	0
0	1	1	1	0
1	0	0	1	0
1	1	1	1	0

Table 2.2 represents truth table of F = ((A.B')'+(A'B')')'

2.3: K = ((A'+B)'.(A'+B')')'

Circuit Diagram:

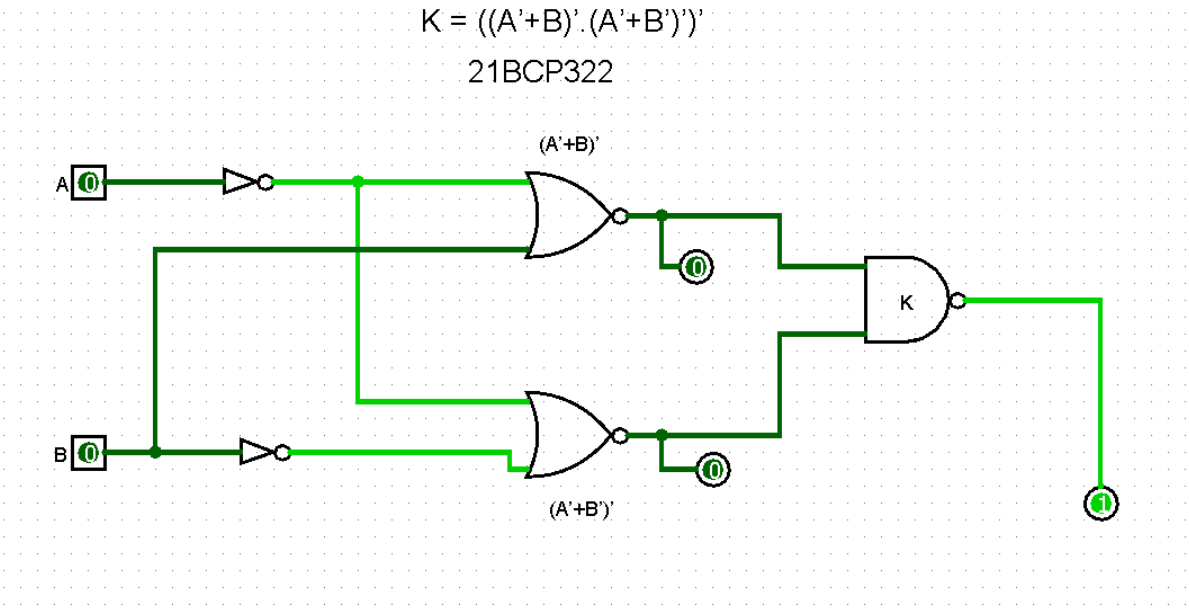


Figure 2.3 Representing Circuit of K = ((A'+B)'.(A'+B')')'

Truth table:

A	B	x	y	z
0	0	0	0	1
0	1	0	0	1
1	0	1	0	1
1	1	0	1	1

Table 2.3 represents truth table of K = ((A'+B)'.(A'+B')')'

EXERCISE 3 -: For each of the following problem statement, design a circuit, describe a Truth table and verify the outcome using Logisim.

3.1 -: Implement the functionality of XOR gate using only NAND gates**.**

Circuit Diagram:

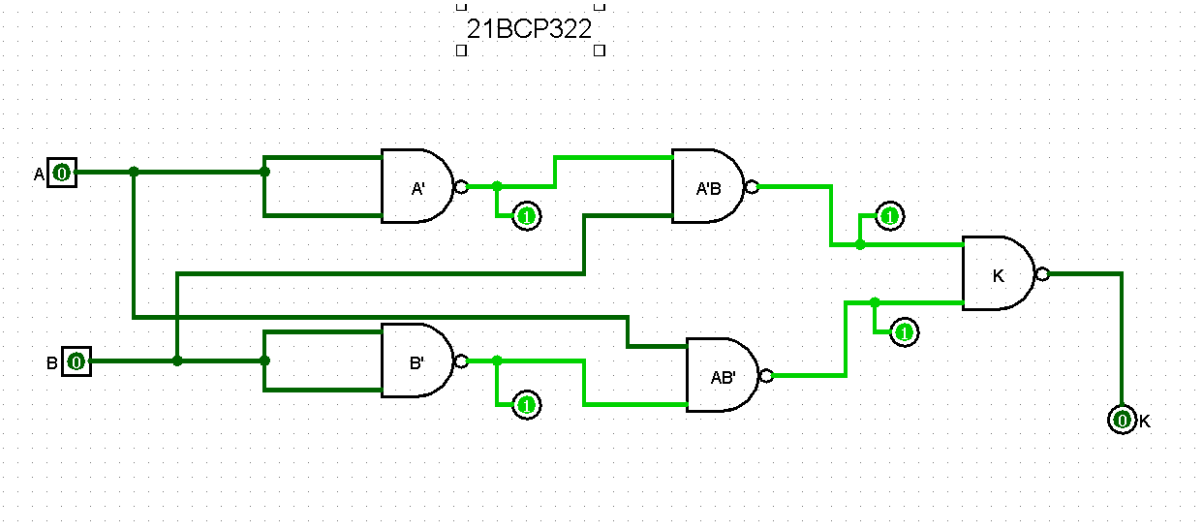


Figure 3.1 Representing Circuit of XOR gate using NAND gates

Truth table:

A	B	x	y	z	u	K
0	0	1	1	1	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	1	0	1	1	0	0

3.2: Implement the functionality of XNOR gate using only NOR gates.

CIRCUIT DIAGRAM:

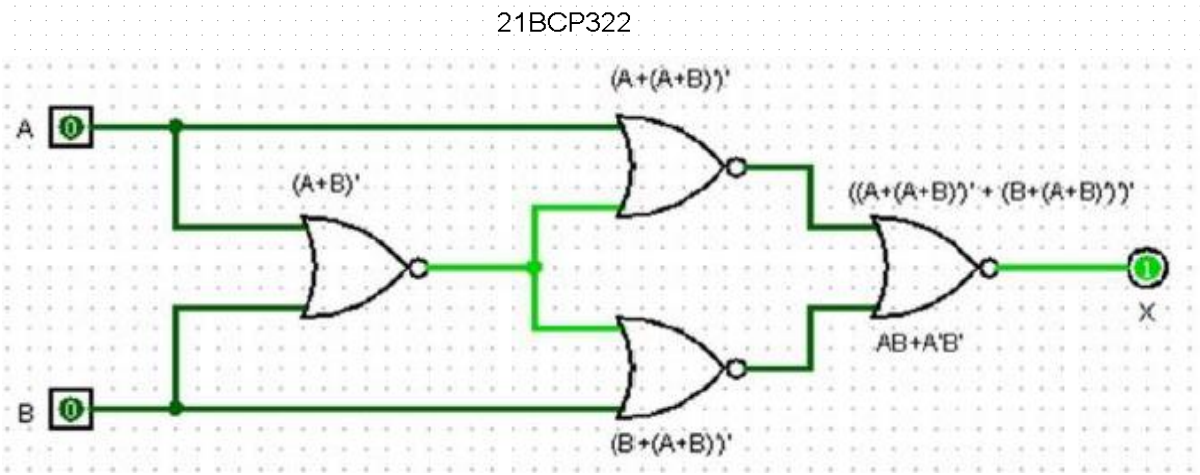


Figure 3.2 Representing Circuit of XNOR gate using NOR gates

Truth Table:

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

Table 3.2 represents the truth table of XNOR gate

3.3 -: Implement the functionality of AND gate using only NAND gates.

CIRCUIT DIAGRAM

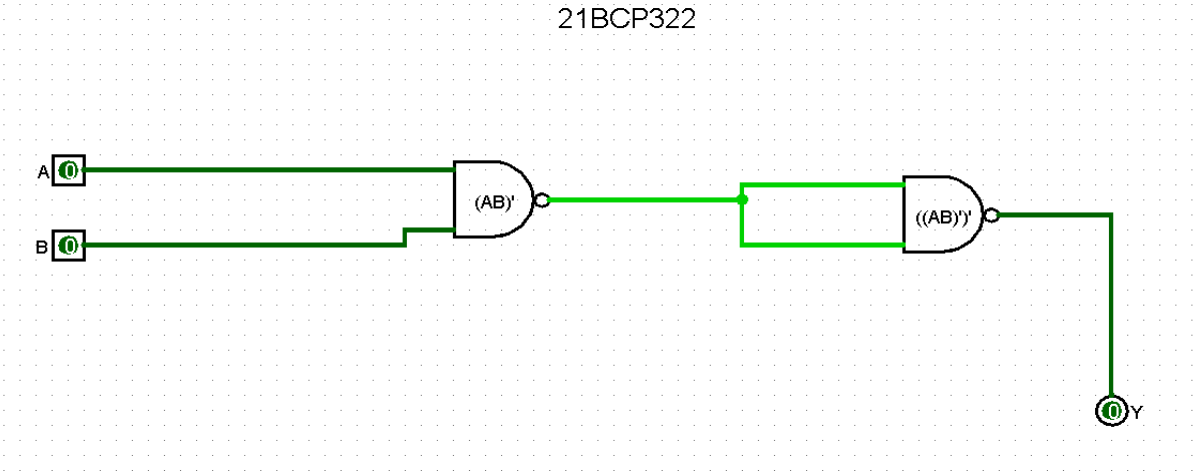


Figure 3.3 Representing Circuit of AND gate using NAND gate

Truth table:

A	B	x	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 3.3 represents truth table of AND gate

3.4**:** Implement the functionality of OR gate using only NOR gates.

CIRCUIT DIAGRAM:

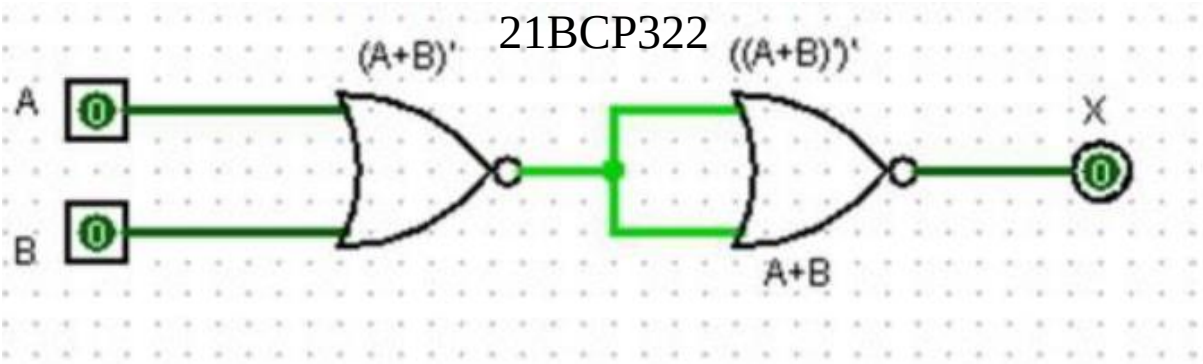


Figure 3.4 Representing Circuit of OR gate using NOR gates

Truth table:

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

Table 3.4 represents truth table of OR gate

3.5: Implement the functionality of NOT gate using only NAND gate.

CIRCUIT DIAGRAM:

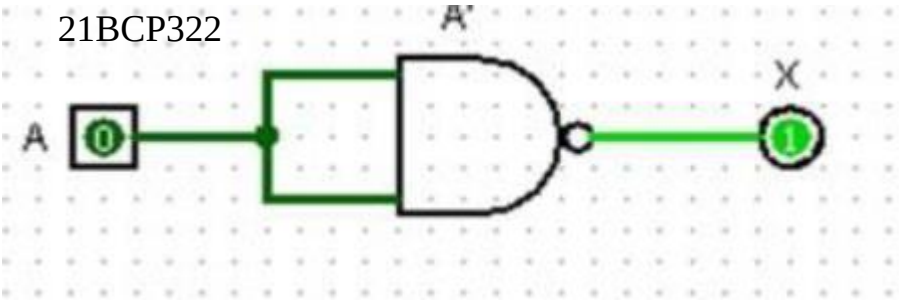


Figure 3.5 Representing Circuit of NOT gate using NAND gate

Truth table:

A	X
0	1
1	0

Table 3.5 represents truth table of NOT gate