CMPE 200 HW#5

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Speculative Computing (25pts + 25pts)

1.

id	Instruction	ISSUE	EXE	WB	COMMIT
I1	mul $t1, $t2, $t3	1	2-11	12	13
I2	add $t4, $t5, $t6	2	3	4	14
I3	beq $t1, $0, I7	3	12	-	15
I4	add $t4, $t4, $t7	4	5	6	
I5	ld $t3, 0($t8)	5	6-9	10	
I6	mul $t4, $t4, $t3	6	10-13		
I7	add $t4, $t1, $t3	14	15	16	17
I8	ld $t5, 0($t1)	15	16-19	20	21
I9	add $t2, $t4, $t5	16	20	21	22

2.

id	Instruction	ISSUE	EXE	WB	COMMIT
I1	mul $t1, $t2, $t3	1	2-11	12	13
I2	add $t4, $t5, $t6	2	3	4	14
I3	st $t4, 4($t1)	3	12	-	15
I4	add $t4, $t4, $t7	4	5	6	16
I5	ld $t3, 0($t8)	5	13-16	17	18
I6	mul $t4, $t4, $t3	6	17-26	27	28
I7	add $t4, $t1, $t3	7	17	18	29
I8	ld $t5, 0($t1)	8	13-16	19	30
I9	add $t2, $t4, $t5	9	19	20	31

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3. (a).

Number of blocks in a cache = $2^{26}/2^7 = 2^{19}$
Number of sets = $2^{19}/2^2 = 2^{17}$
Size of each line's tag in bits = 32 bits address – 17 bits index – 7 bits block offset = 8 bits

(b).
Number of bits in index = 11 bits
Number of bits in block offset = 32 bits address – 11 bits index – 12 bits tag = 9 bits
Block size = 2^9 = 512 bytes
Cache can store = 4 blocks per set * 2048 sets * 512 bytes = 4MB

(c).
Number of bits in block offset = 8 bits
Number of bits in index = 32 bits address – 14 bits tag – 8 line offset = 10 bits of index → 4-way set associative

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4. Miss rate of FIFO: 15/24 = 0.625

Access		a	b	c	d	c	b	a	e	f	f	g	f	a	e	f	g	d	c	b	a	e	f	g	a
Priority Order	0	A	B	C	D	D	D	D	E	F	F	G	G	A	A	A	A	D	C	B	B	E	F	G	A
	1		A	B	C	C	C	C	D	E	E	F	F	G	G	G	G	A	D	C	C	B	E	F	G
	2			A	B	B	B	B	C	D	D	E	E	F	F	F	F	G	A	D	D	C	B	E	F
	3				A	A	A	A	B	C	C	D	D	E	E	E	E	F	G	A	A	D	C	B	E
Cache miss		m	m	m	m	h	h	h	m	m	h	m	h	m	h	h	h	m	m	m	h	m	m	m	m

Miss rate of LRU: 14/24 = 0.583

Access		a	b	c	d	c	b	a	e	f	f	g	f	a	e	f	g	d	c	b	a	e	f	g	a
Priority Order	0	A	B	C	D	C	B	A	E	F	F	G	F	A	E	F	G	D	C	B	A	E	F	G	A
	1		A	B	C	D	C	B	A	E	E	F	G	F	A	E	F	G	D	C	B	A	E	F	G
	2			A	B	B	D	C	B	A	A	E	E	G	F	A	E	F	G	D	C	B	A	E	F
	3				A	A	A	D	C	B	B	A	A	E	G	G	A	E	F	G	D	C	B	A	E
Cache miss		m	m	m	m	h	h	h	m	m	h	m	h	h	h	h	h	m	m	m	m	m	m	m	h

Miss rate of Pseudo-LRU: 14/24 = 0.583

Access		a	b	c	d	c	b	a	e	f	f	g	f	a	e	f	g	d	c	b	a	e	f	g	a
Priority Order	0	A	B	C	D	C	B	A	E	F	F	G	F	A	E	F	G	D	C	B	A	E	F	G	A
	1		A	B	C	D	A	B	C	A	A	E	A	F	G	A	E	F	G	D	C	B	A	E	F

	2			A	B	B	C	C	A	E	E	F	G	G	A	E	F	G	D	C	B	A	E	F	G
	3				A	A	D	D	B	C	C	A	E	E	F	G	A	E	F	G	D	C	B	A	E
Cache miss		m	m	m	m	h	h	h	m	m	h	m	h	h	h	h	h	m	m	m	m	m	m	m	h

0 cache: MRU
3 cache: LRU
