CMPE 200 HW#6

Computer Engineering Department, San Jose State University

Name: Akshata Deo SJSU ID: 012565761

Cache replacement policy (15pts)

1.

a)

Trace		Initial	0	1	0	4	2	1	4	7	5	0	6	1	4	2
priority	Set															
MRU	0	0	0	0	0	4	2	2	4	4	4	0	6	6	4	2
		4	4	4	4	0	4	4	2	2	2	4	0	0	6	4
		2	2	2	2	2	0	0	0	0	0	2	4	4	0	6
LRU		6	6	6	6	6	6	6	6	6	6	6	2	2	2	0
MRU	1	7	7	1	1	1	1	1	1	7	5	5	5	1	1	1
		5	5	7	7	7	7	7	7	1	7	7	7	5	5	5
LRU		9	9	5	5	5	5	5	5	5	1	1	1	7	7	7
		3	3	9	9	9	9	9	9	9	9	9	9	9	9	9
cache miss			h	m	h	h	h	h	h	h	h	h	h	h	h	h

b). Miss ratio = 1/14 = 0.07

2.

1) a. 1st level: $2^4 \times 4 = 2^6$ Bytes = 64 Bytes 2nd level: $2^8 \times 4 = 2^{10}$ Bytes = 1 KB 3rd level: $2^4 \times 4 = 2^6$ Bytes = 64 Bytes

b. 1st level: 2^{28} Bytes = 256 MB 2nd level: 2^{20} Bytes = 1 MB

3rd level: 64 KB

2) a. 32 sets can be indexed by 5 bits (20 to 16 i.e. 5 bits)

b. 31 to 21

3.

1). Page size = 4 KB

Therefore, 12 bits for page offset and 20 bits for virtual page number

Total number of pages = 2^{20}

Size of a single-level page table = $2^{20} * 4 = 2^{22}$ bytes = 4 MB

2). Given a 2-level page table. The virtual page number is split into two equal-sized fields for the first-level and the second-level page tables. So, we have virtual page number with 20 bits. Hence, we will have two 10 bits fields.

Size of first level page table = $2^{10} * 4 = 2^{12} = 4$ KB

Now, according to the diagram, 3 second-level page tables are required per first-level table (1 for code, 1 for data and 1 for 1 for kernel)

Size of one second level page table = $2^{10}*4 = 4KB$

Total size = 4 + 3*4 KB = 16KB

3) For a three-level page table (20 bits)

First-level page table $(25\%) = 2^5*4 = 128$ Bytes

Second level page table $(25\%) = 2^{5}*4 = 128$ Bytes

Third level page table $(50\%) = 3*(2^{10})*4 = 12288$ Bytes

Total = 128 + 128 + 12288 = 12.25KB

Cache Coherence (25 pts)

4. Total number of cycles: 373

	r1(A)	r2(A)	w3(B)	w2(A)	r3(A)	r1(B)	r2(B)	w3(B)	r3(A)	r1(A)
hit/miss	M	М	М	Н	Н	М	Н	Н	Н	М
bus	BusRd	BusRd	BusRdX	Bus/upgr	-	busRd	-	BusUpgr	-	BusRd

State1	Е	0	I	I	I	S	S	I	S	S
State2	I	S	ĺ	М	S	S	S	Ì	S	I
State3	I	- 1	М	М	0	0	0	М	S	0
cycles	150	50	50	10	1	50	1	10	1	50