CMPE 200 HW#1

Due: Monday, Sep. 16, 11:59pm
Total Score: /100

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Performance (15pts)

1. Consider three different processors P1, P2, and P3 executing the same instruction set. And, their clock rate and CPI are like below:

	P1	P2	P3
Clock rate	3 GHz	4 GHz	5 GHz
CPI	1.5	2	2.5

   For the three processors, solve the three problems. Round off the calculated results to two decimal places if needed.
   a. Which processor has the highest performance expressed in instructions per second?
   b. Suppose that all three processors took 100 seconds to run a program. We want to achieve 2x speedup in running this program on all processors by increasing clock frequency. But, we found that the frequency increase led to an increase of CPI by 10%, 20% and 30% for P1, P2, and P3, respectively. So, we adjusted the clock frequency to accommodate the new CPI. What would be the final clock frequency of each of the three processors?

Instruction Set Architecture (35pts)

2. In this problem, we compare the efficiency of four ISAs with respect to code compaction and to memory traffic:
   - Stack-based
   - Memory-to-memory (all operands are located in main memory)
   - Register-based (pure Load/Store)

   Assume the following components to calculate instruction size:

   - In an instruction format,
     - opcodes are 1-byte wide
     - memory address fields are 4-byte wide
     - register fields (in the Load/Store machine) are 2-byte wide

   Consider the following high level language code:

   $$C = D - A$$
   $$B = B + C$$

   a. Implement this code using the three ISAs (stack, memory-to-memory, and Load/Store). In this code, A, B, C, and D are memory addresses. Therefore, you should store the result of each instruction's computation back to the memory (addresses C, and B should be updated by the two instructions respectively.). In the case of the memory-to-memory architecture, do not use any additional memory locations besides A, B, C, or D.

   b. For the code of each ISA, calculate the following metrics:

      1) Code size
         - Code size = # instructions × size of each instruction
         - Assume that each ISA uses uniform size instruction, which means that the length of the instructions in each ISA is identical. To figure out the instruction size of each ISA, check all the required fields (e.g. opcode, memory address field, and/or register) of each instruction and use the length of the longest instruction as the instruction length of the ISA.

      2) Memory accesses
         - # memory accesses = Total number of accesses to memory to load and store data

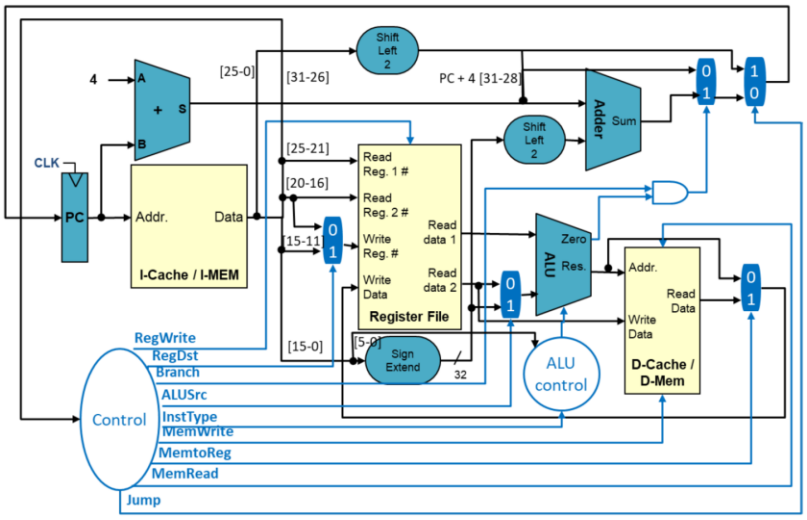
   c. Then, compare the three ISAs with regarding to the code size and memory accesses.

Single-cycle MIPS Architecture (25pts)

3. Assume that core components of single-cycle processor (shown below) have the following latencies:

I-Mem	Adder	Mux	ALU	Regs Rd/Wr	D-Mem	Sign-Extend	Shift-Left-2
40ps	50ps	20ps	100ps	80ps/60ps	200ps	20ps	20ps

Single-cycle processor data path:



Suppose that this data path executes only two types of instruction:

```
sub $rd, $rs, $rt
lw  $rt, offset($rs)
```

What would be the clock period for executing these two instructions? Assume that PC register doesn't take any latency (i.e. Propagating a new PC value to I-Cache/I-Mem doesn't take any cycle).

Pipelined Datapath and Data Hazards (25pts)

4. Assume that individual pipeline stages of a five-stage piplined architecture take the following latencies:

IF	ID	EX	MEM	WB
100ps	120ps	220ps	300ps	120ps

   a. What is the clock latency of single-cycle processor?

   b. What is the clock latency in a pipelined processor?

   c. Suppose that the clock latency is set as your answer above. What is the total latency of a Beq instruction in a pipelined and single-cycle processor?