CMPE 200 HW#3

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1. (a). Consider the following code.

```
L1: lw $t4, 0($t1)      // I1
    lw $t5, 4($t1)      // I2
    addi $t1, $t1, 4    // I3
    sll $t1, $t1, 2     // I4
    add $t2, $t4, $t5   // I5
    beq $t2, $zero, L1  // I6
    sw $t4, 0($t1)      // I7
    sw $t5, -4($t1)     // I8
```

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	CC11	CC12	CC13
I1	IF	ID	EXE	MEM	WB								
I2		IF	ID	EXE	MEM	WB							
I3			IF	ID	EXE	MEM	WB						
I4				IF	ID	EXE	MEM	WB					
I5					IF	ID	EXE	MEM	WB				
I6						IF	ID	EXE	MEM	WB			
I7							IF						
I1								IF	ID	EXE	MEM	WB	
I2									IF	ID	EXE	MEM	WB

(b).

W/O branch delay slot	With branch delay slot
`L1: lw $t4, 0($t1)  // I1`	`L1: lw $t4, 0($t1)  // I1`

```
lw $t5, 4($t1)       // I2
addi $t1, $t1, 4     // I3
sll $t1, $t1, 2      // I4
add $t2, $t4, $t5    // I5
beq $t2, $zero, L1   // I6
sw $t4, 0($t1)       // I7
sw $t5, -4($t1)      // I8
```

```
lw $t5, 4($t1)       // I2
addi $t1, $t1, 4     // I3
add $t2, $t4, $t5    // I4
beq $t2, $zero, L1   // I5
sll $t1, $t1, 2      // I6
sw $t4, 0($t1)       // I7
sw $t5, -4($t1)      // I8
```

I4 instruction must be executed regardless of branch outcome and is independent of branch instruction. Hence, we can reduce stall cycle by placing I4 instruction in branch delay slot (right after branch instruction as shown in table).

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2. (a). Misprediction for always taken: 04
Misprediction for always not taken: 04

(b). Misprediction rate = 4/8 = 50%

One bit branch predictor	Predicted Outcomes	Actual Outcomes	Misprediction
0	NT	NT	FALSE
0	NT	T	TRUE
1	T	T	FALSE
1	T	NT	TRUE
0	NT	NT	FALSE
0	NT	T	TRUE
1	T	T	FALSE
1	T	NT	TRUE

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3. (a). Misprediction for b1: 7/9
Misprediction for b2: 2/9

Iteration		1	2	3	4	5	6	7	8	9
X		2	5	6	11	13	18	5	6	11
b1's predictor		00	00	01	00	01	10	01	10	01
b2's predictor		00	01	10	11	11	11	11	11	11
b1	Predicted	NT	NT	NT	NT	NT	T	NT	T	NT
	Actual	NT	T	NT	T	T	NT	T	NT	T
b2	Predicted	NT	NT	T	T	T	T	T	T	T
	Actual	T	T	T	T	T	T	T	T	T

(b). Misprediction for b1: 5/9
Misprediction for b2: 3/9

iteration		1	2	3	4	5	6	7	8	9
X		2	5	6	11	13	18	5	6	11
global history	Initial	0	1	1	1	1	1	1	1	1
	After b1	0	1	0	1	1	0	1	0	1
b1	Predicted	NT	NT	T	NT	T	T	T	T	T
	Actual	NT	T	NT	T	T	NT	T	NT	T
b2	Predicted	NT	NT	NT	T	T	T	T	T	T
	Actual	T	T	T	T	T	T	T	T	T

Predictor buffer 0	00 →00→01 →10→11
Predictor buffer 1	00 →01 →10→01 →10→11 →10→11 →10→11