CMPE 200 HW#2

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1. **(a).** The length of longest stage is 300ps. Therefore, the clock latency in a pipelined processor is 3**00ps**

   (b). The total latency in a Beq instruction in a pipelined processor is (5*300) = **1500ps**

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2. **(a).**

Type	Dependencies in the code Format: "register id" of "instruction id" -> "dependent instructions id" (i.e. $t0 of I1 -> I2)
Read-After-Write (RAW)	$sp of I1→I2, I1→I5, I1→I6 $a0 of I2→I3 $t0 of I3→I4,I3→I5
Write-After-Write (WAW)	$sp of I1→I6 $t0 of I3→I4
Write-After-Read (WAR) Do not consider the dependency within an instruction (ex. Register value is read and the same register is written with a calculation result)	$sp of I2→I6, I5→I6

(b). Read-After-Write (RAW), because we can not read a register until it is updated with latest value. If the value of the register is read before write, hazard happens.

(c). It will take **20 cycles** to execute the following code.

```
addi  $sp,  $sp, -4
lw     $a0, 0($sp)
slti    $t0,  $a0, 60
addi  $t0,  $t0, 1
sw    $t0,  0($sp)
addi  $sp, $sp, 4
```

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
addi	IF	ID	EXE	MEM	WB					
lw		IF	ID	ID	ID	EXE	MEM	WB		
slti			IF	IF	IF	ID	ID	ID	EXE	MEM
addi						IF	IF	IF	ID	ID
sw									IF	IF
addi										

	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20
addi										
lw										
slti	WB									
addi	ID	EXE	MEM	WB						
sw	IF	ID	ID	ID	EXE	MEM	WB			
addi		IF	IF	IF	ID	ID	ID	EXE	MEM	WB

(d). It will take **13 cycles** to execute the following code.

```
addi  $sp,  $sp, -4
lw    $a0, 0($sp)
slti   $t0,  $a0, 60
addi  $t0,  $t0, 1
sw    $t0,  0($sp)
addi  $sp, $sp, 4
```

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13
addi	IF	ID	EXE	MEM	WB								
lw		IF	ID	EXE	MEM	WB							
slti			IF	ID	ID	EXE	MEM	WB					
addi				IF	IF	ID	ID	EXE	MEM	WB			
sw						IF	IF	ID	EXE	MEM	WB		
addi								IF	ID	ID	EXE	MEM	WB

3.

```
I1: LOOP: lw $a0, 0($sp)
I2:       slti $t0, $a0, 1
I3:       beq $t0, $zero, L1
I4:       addi $sp, $sp, 8
I5: L1:   lw $ra, 4($sp)
I6:       addi $t4, $ra, 8
I7:       sw $t4, 0($t1)
I8:       addi $v0, $zero, 1
I9:       b LOOP
I10:      add $t4, $t4, $t3
```

	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	CC11	CC12	CC13	CC14	CC15	CC16	CC17	CC18
I1	IF	ID	EXE	MEM	WB													
I2		IF	ID	ID	EXE	MEM	WB											
I3			IF	IF	ID	ID	EXE	MEM	WB									

I4					IF	IF												
I5							IF	ID	EXE	MEM	WB							
I6								IF	ID	ID	EXE	MEM	WB					
I7									IF	IF	ID	EXE	MEM	WB				
I8											IF	ID	EXE	MEM	WB			
I9												IF	ID	EXE	MEM	WB		
I10													IF					
I1														IF	ID	EXE	MEM	WB
I2															IF	ID	ID	EXE
I3																IF	IF	ID