CMPE 200 HW#5

Due: Monday, Nov 25, 11:59pm
Total Score: /100

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Speculative Computing (25pts + 25pts)

1. Use the following assumption:
   - One instruction can issue per cycle
   - Latencies (cycles):
     - add : 1
     - ld : 4
     - mul : 10
     - beq : 1
   - There are no RS or ROB stalls (similar to infinite sized RS/ROB)
   - There are no functional unit stalls (similar to infinite ALUs)
   - WB and EXE occur in the same cycle (i.e. an instruction writes to the CDB in cycle n, and its dependent instruction can start execution in cycle n as well)
   - There is a single CDB

   For the following code, show the timing assumption that the branch (I3) is initially predicted untaken. But, I3's actual outcome is turned out to be taken. If I3 executes, say on cycle *i*, I4, I5, and I6 should be flushed in cycle *i*+1, and then I7 issues in cycle *i*+2.

id	Instruction	ISSUE	EXE	WB	COMMIT
I1	mul $t1, $t2, $t3				
I2	add $t4, $t5, $t6				
I3	beq $t1, $0, I7				
I4	add $t4, $t4, $t7				
I5	ld $t3, 0($t8)				
I6	mul $t4, $t4, $t3				
I7	add $t4, $t1, $t3				
I8	ld $t5, 0($t1)				
I9	add $t2, $t4, $t5				

2. Use the same assumption with prob. 3. But in this case, we will evaluate the architecture with correct load and store executions. Assume that store instruction takes 1 cycle. Fill the following timing table by assume that we use a conservative memory disambiguation approach.

id	Instruction	ISSUE	EXE	WB	COMMIT
I1	mul $t1, $t2, $t3				
I2	add $t4, $t5, $t6				
I3	st $t4, 4($t1)				
I4	add $t4, $t4, $t7				
I5	ld $t3, 0($t8)				
I6	mul $t4, $t4, $t3				
I7	add $t4, $t1, $t3				
I8	ld $t5, 0($t1)				
I9	add $t2, $t4, $t5				

Caches (25pts + 25pts)

3. Assume that the system uses 32-bit address.
   a. Consider a cache with 64MB of data, 4-way set associativity, and 128-byte line (block) size. What is the size of each line's tag in bits?

   b. Consider a cache with 2048 sets, 4-way set associativity, and 12-bit tags. How many bytes can the cache store? (What is the data capacity not including overhead of storing tags, valid bits, etc.?)

   c. Consider a cache with a 256-byte line size and 14-bit tags. The cache has 4096 lines. What is the set associativity of the cache?

4. In this problem, we compare cache replacement policies for a given trace of accesses to a set. A trace is made of consecutive block addresses dynamically accessed by a program. Take the following trace, where each letter is a block address:

   abcdcbaeffgfaefgdcbaefga

   Assume that the fully associative cache that has four cache lines is cold (empty) at the beginning. What is the miss rate under the following replacement policies:

   - FIFO
   - LRU
   - Pseudo-LRU