CMPE 200 HW#4

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1. In the static pipelining with superscalar architecture, loop unrolling adopts parallelism. Hence, improve the performance. It transforms M iteration loop into M/N iteration loop (if unrolled N times) effectively decreasing Branch instructions from M to M/N. It provides better scheduling of the algorithm. Address calculation removed from the mid and offset is updated only once calculating address for combined instructions. For an example:

Without loop unrolling, following instructions executed twice (8*2=16 instructions)	**With loop unrolling following instructions executed only once (10 instructions)**
ld.s$f0, 0($t1)	ld.s$f0, 0($t1)
ld.s$f1, 0($t2)	ld.s$f1, 0($t2)
add.s$f2, $f1, $f0	ld.s$f3, 4($t1)
st.s$f2, 0($t1)	ld.s$f4, 4($t2)
add $t1, $t1, #4	subi$t3, $t3, #2
addi$t2, $t2, #4	addi$t1, $t1, #8
subi$t3, $t3, #1	addi$t2, $t2, #8
benz $t3, Loop	st.s$f2, -8($t1)
	st.s$f5, -4($t1)
	bnez$t3, Loop

2.

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      lw $t0, 0($t1)          // I1
LOOP: lw $t2, -8($t1)         // I2
      lw $t3, -16($t1)        // I3 (extra added)
      subi $t1, $t1, #16      // I4 (shifted from bottom to up)
      add $t4, $t2, $t0       // I5
      add $t0, $t3, $t4       // I6 (added extra)
      sw $t4, 8($t1)          // I7
      sw $t0, 0($t1)          // I8 (added extra)
      bne $t1, $t2, LOOP      // I9
```

3.

Instruction	RS	Source(s)	ISSUE	EXE	WB
div $t1, $t2, $t3	md1	$t2, $t3	1	2-21	22
ld $t4, 0($t5)	ld1	$t5	2	3-6	7
mul $t2, $t1, $t6	md2	md1, $t6	3	22-29	30
add $t3, $t5, $t6	add1	$t5, $t6	4	5	6
div $t6, $t7, $t3	md1	$t7, add1	23	30-49	50
add $t1, $t4, $t3	add1	$t4, $t3	24	25	26
ld $t4, 4($t5)	ld1	$t5	25	26-29	31
add $t1, $t1, $t2	add2	add1, md2	26	30	32
add $t1, $t1, $t5	add1	add2, $t5	27	28	29
ld $t3, 0($t5)	ld2	$t5	28	30-33	34

4.

Instruction	RS	ROB	Source(s)	ISSUE	EXE	WB	COMMIT
div $t1, $t2, $t3	md1	rob1	$t2, $t3	1	2-21	22	23
ld $t4, 0($t5)	ld1	rob2	$t5	2	3-6	7	24
mul $t2, $t1, $t6	md2	rob3	md1, $t6	3	22-29	30	31
add $t3, $t5, $t6	add1	rob4	$t5, $t6	4	5	6	32
div $t6, $t7, $t3	md1	rob5	$t7, add1	23	30-49	50	51
add $t1, $t4, $t3	add2	rob6	ld1, add1	24	25	26	52
ld $t4, 4($t5)	ld1	rob1	$t5	25	26-29	31	53
add $t1, $t1, $t2	add3	rob2	add2, md2	26	30	32	54
add $t1, $t1, $t5	add1	rob3	add2, $t5	32	33	34	55
ld $t3, 0($t5)	ld1	rob4	$t5	33	34-37	38	56

5.

Instruction	ISSUE	EXE	WB	COMMIT
div $t1, $t2, $t3	1	2-21	22	23
ld $t4, 0($t5)	1	2-5	6	23
mul $t2, $t1, $t6	2	22-29	30	31
add $t3, $t5, $t6	2	3	4	31
div $t6, $t7, $t3	3	22-41	42	43
add $t1, $t4, $t3	3	6	7	43
ld $t4, 4($t5)	24	25-28	29	44

add $t1, $t1, $t2	24	30	31	44
add $t1, $t1, $t5	32	33	34	45
ld $t3, 0($t5)	32	33-36	37	45