PROJECT - III

EE 619A: VLSI SYSTEM DESIGN

GROUP NAME: Backbench Designers

GROUP MEMBERS:

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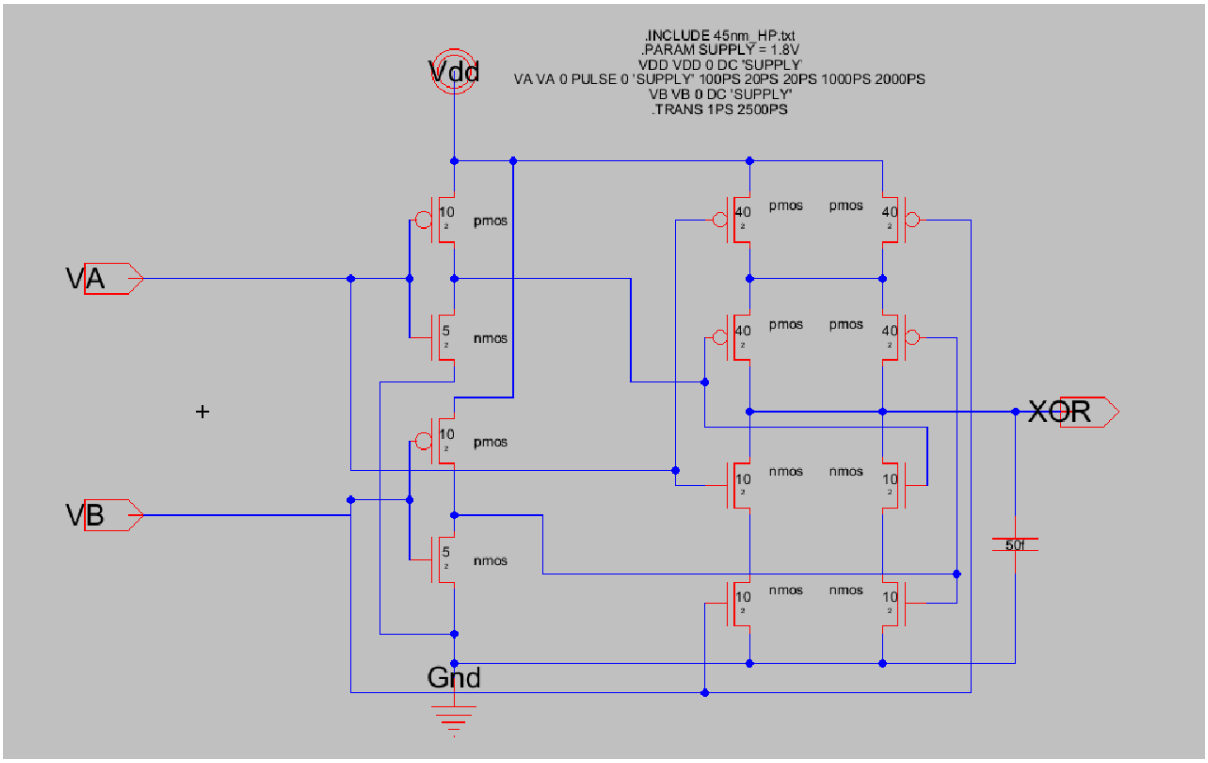
- N Bhuvan - 190521 - nbhuvan@iitk.ac.in

DESIGN RESPONSIBILITY:

- 2-input XOR Gate: N Bhuvan
- 2-input NAND Gate: Akshay Mehta
- 2-input NOR Gate: Bibek Lakra

First Standard Cell : 2-input XOR gate

Screenshot of the schematic:

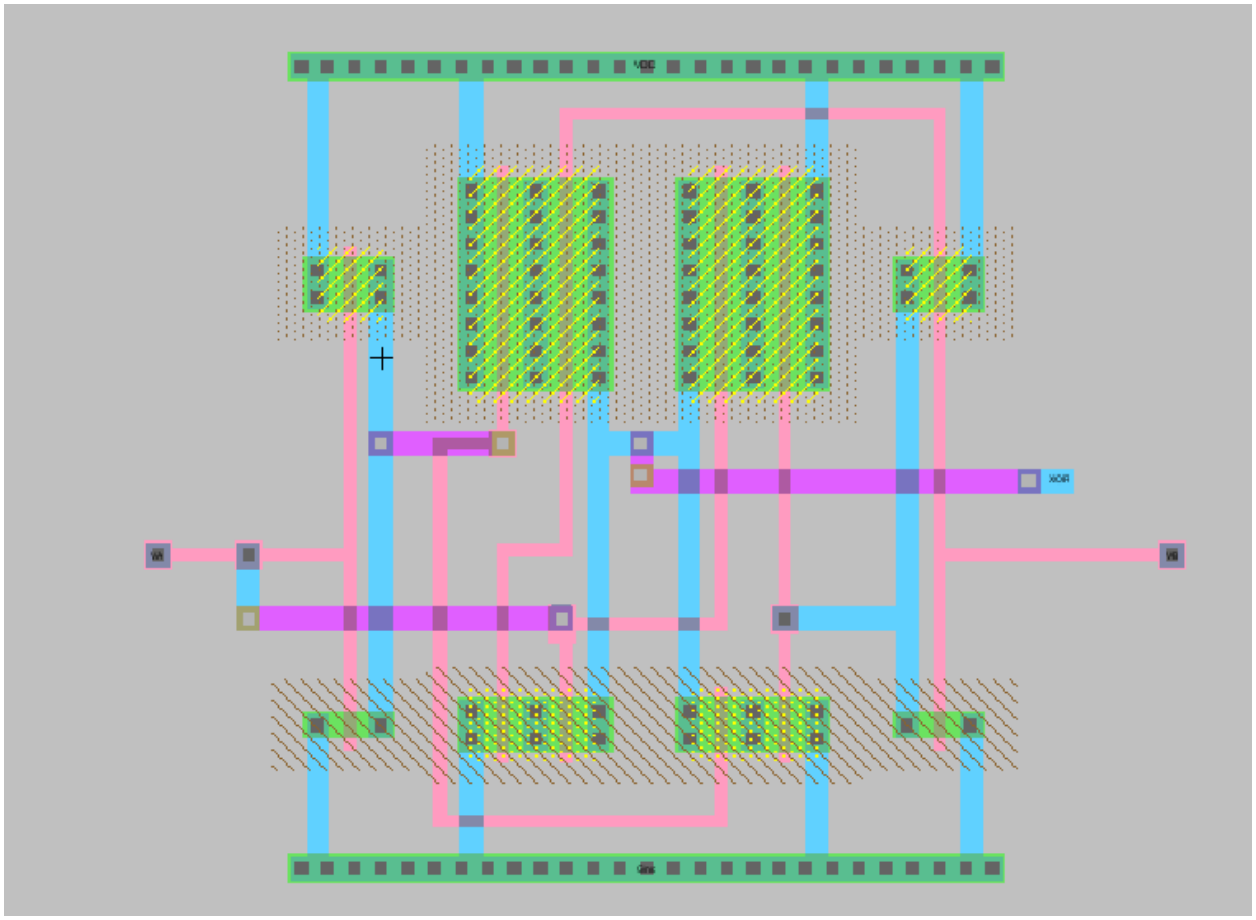


Explanation on how the transistor sizes were chosen:

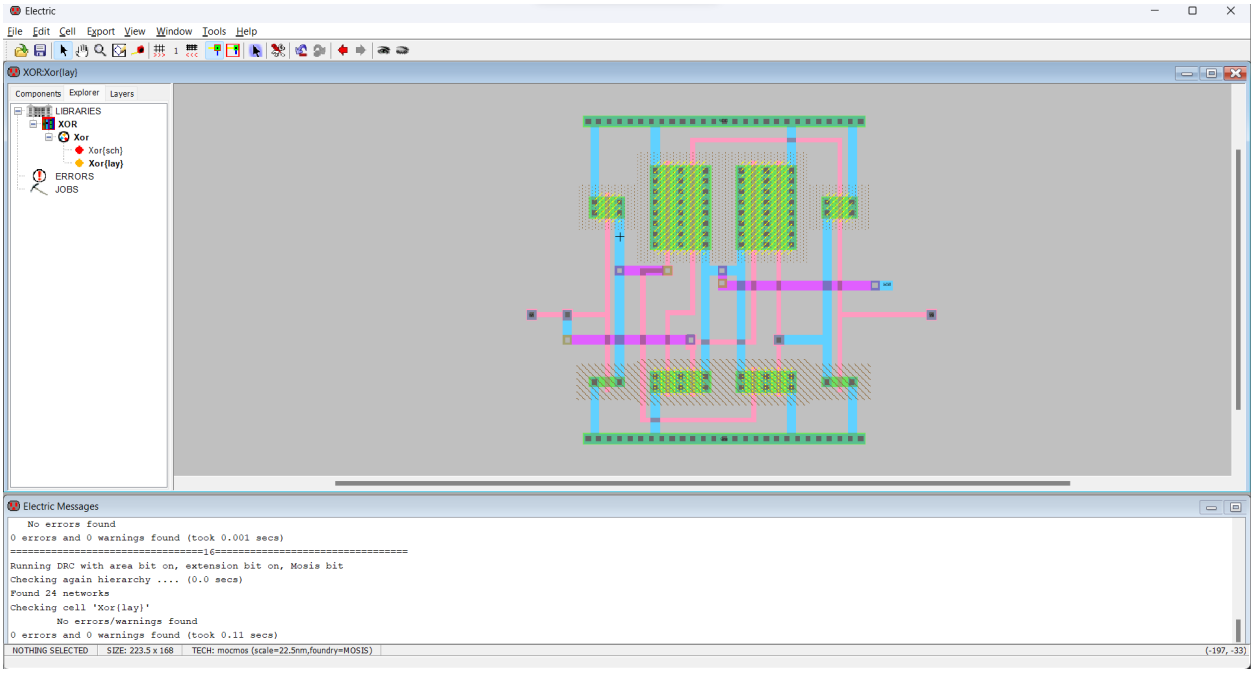
In the inverter, the PMOS is 10λ sized and NMOS transistor is 5λ sized, this we know from the standard inverter which has a Wp:Wn = 2 : 1 and we scaled it to 5. For XOR we first found out the schematic from taking Y' and got Y' = (A & B) + (A' & B'), from which we got the pulldown network. And then we just took the dual of this to get the pull up network.

The sizing has been done in such a way that it has the same worst case delay as that of the inverter used for getting A' and B'. Worst case delay occurs when only one series NMOS tries to pull the output. As there are two NMOS in series each should have a sizing of 2x. And for pull up it occurs when only two PMOS tries to pull up the output, here the sizing should be 4x. So each of the PMOS is 40λ sized and NMOS is 10λ sized.

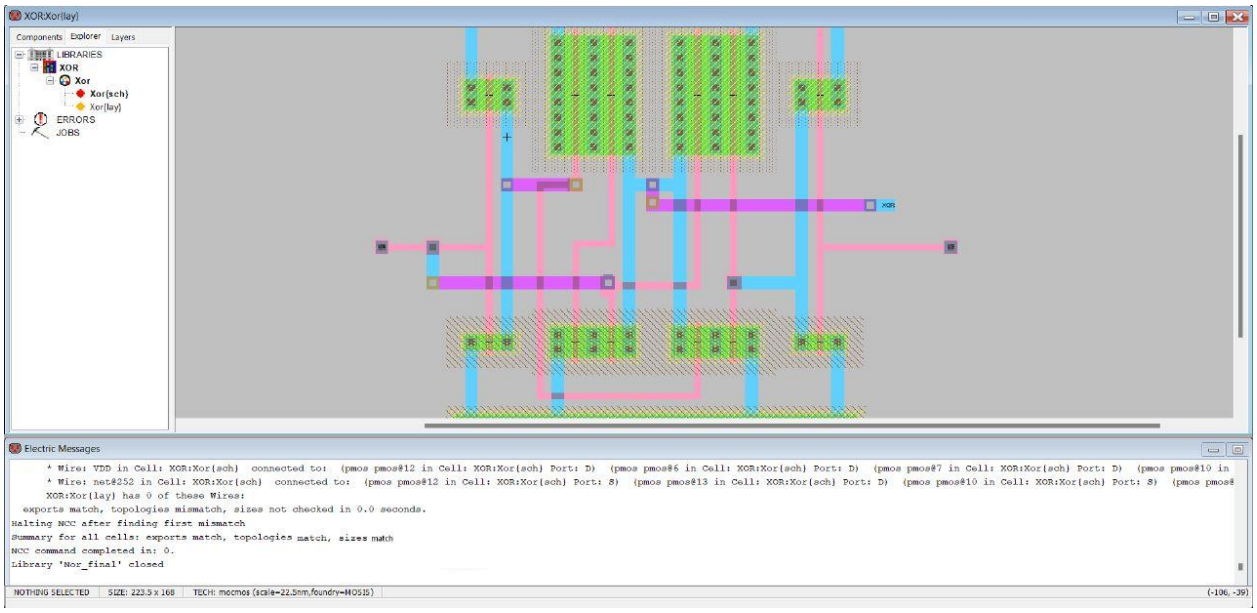
Screenshot of the Layout:



Screenshot with DRC log:



Screenshot with LVS log:



Size of Circuit = 223.5 x 168 nm

Table with the propagation delay values from the schematic and the layout for 5 fF and 50 fF fanout loads :

Capacitor	Propagation delay(Schematic)	Propagation delay(Layout)
5fF	13 ps	17ps
50fF	47ps	17ps

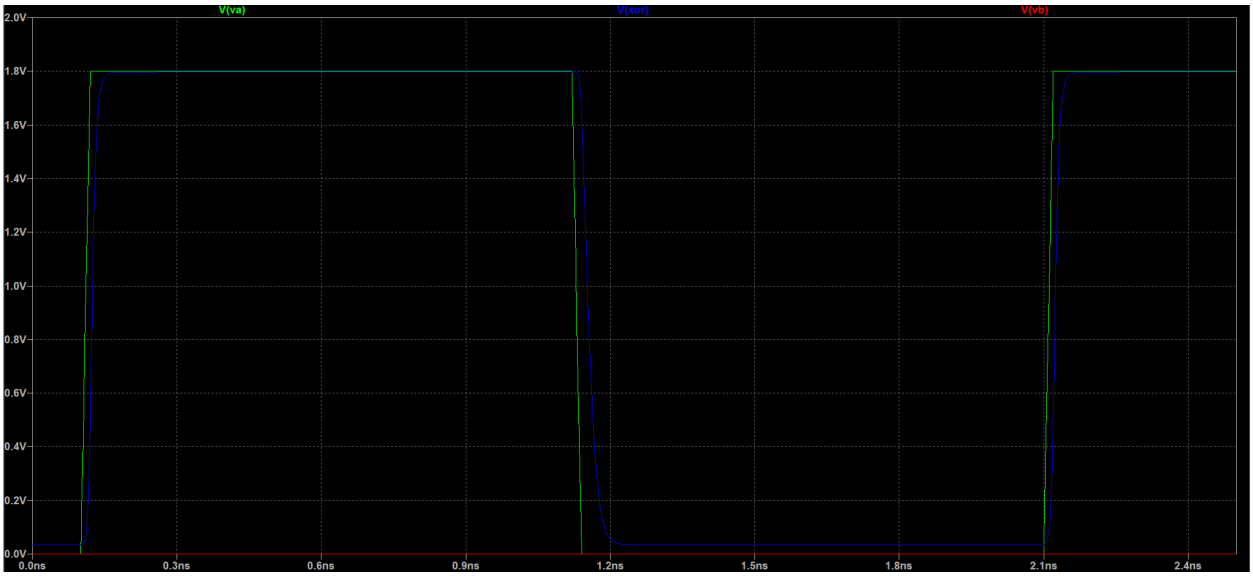
The power consumption from the schematic and layout-extracted simulations :

Simulation	Avg Power Consumption
Schematic	1.4 mW
Layout - extracted	

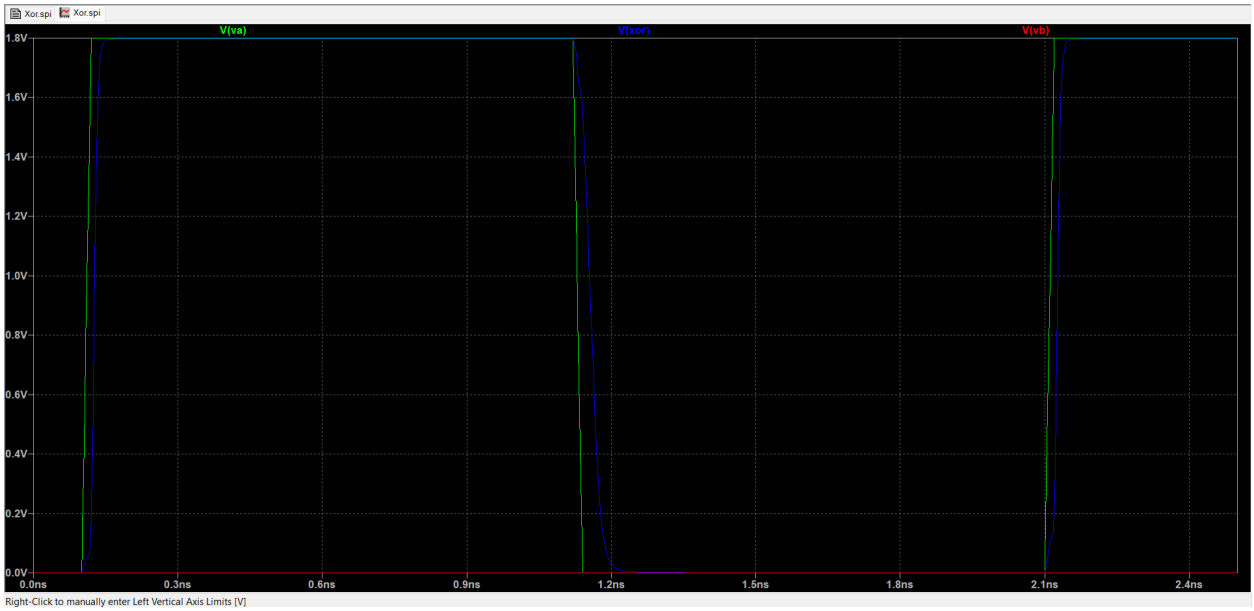
Waveform Analysis:

A(Va)	B(Vb)	Y(Vout)
0	0	0
0	1	1
1	0	1
1	1	0

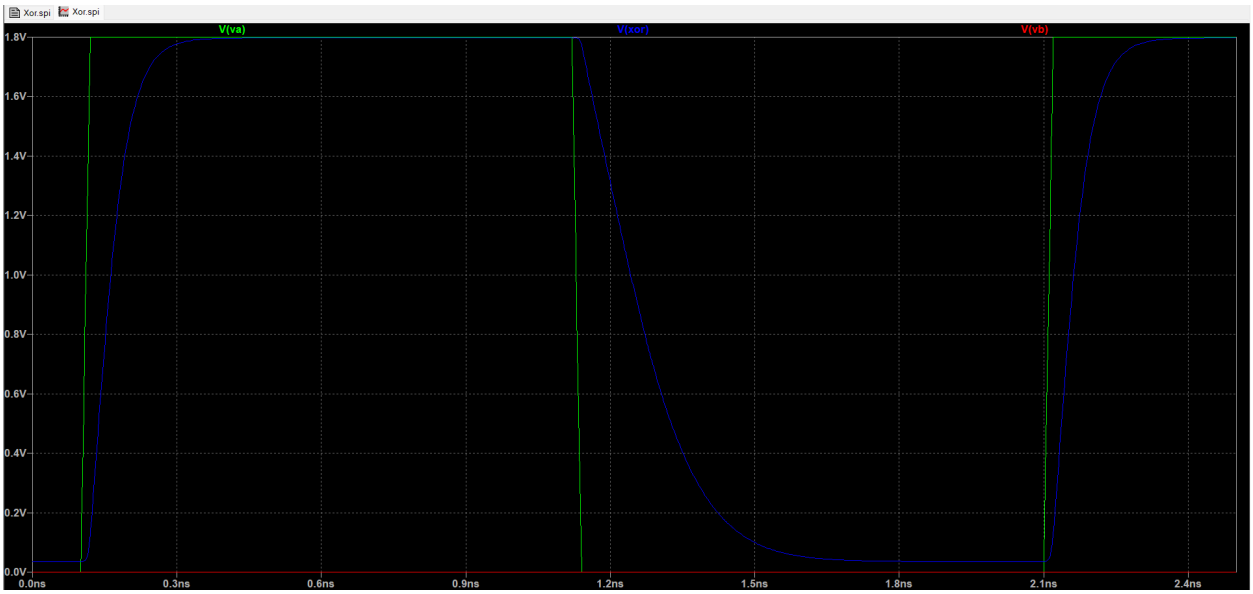
- For C=5fF
  - Schematic:



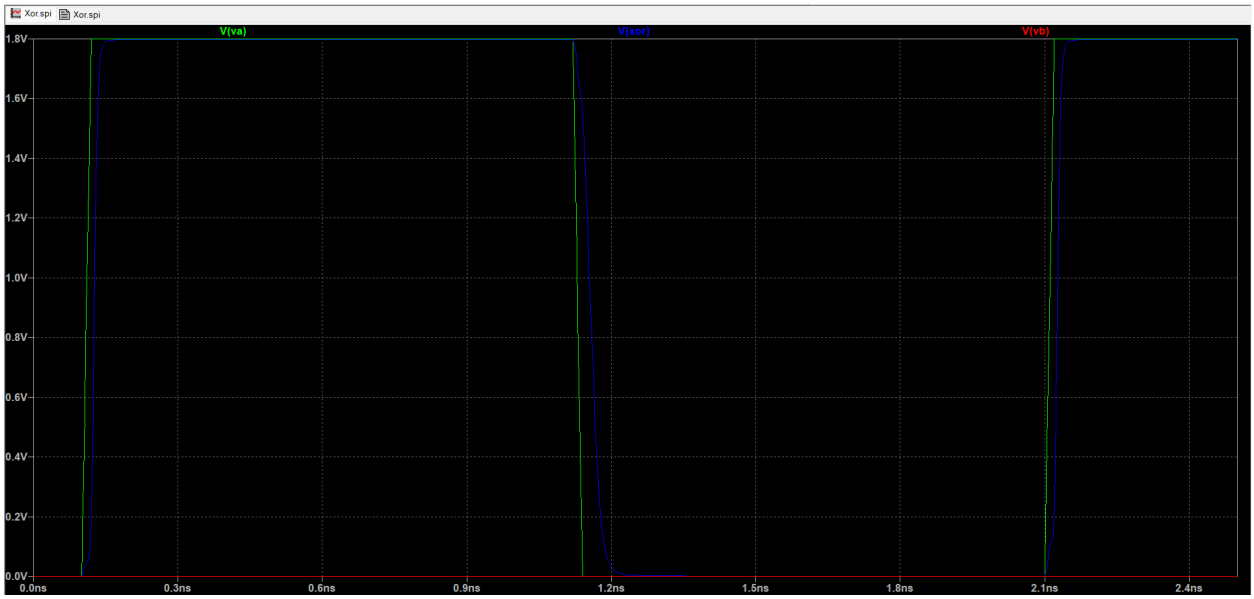
  - Layout:



- **Schematic:**

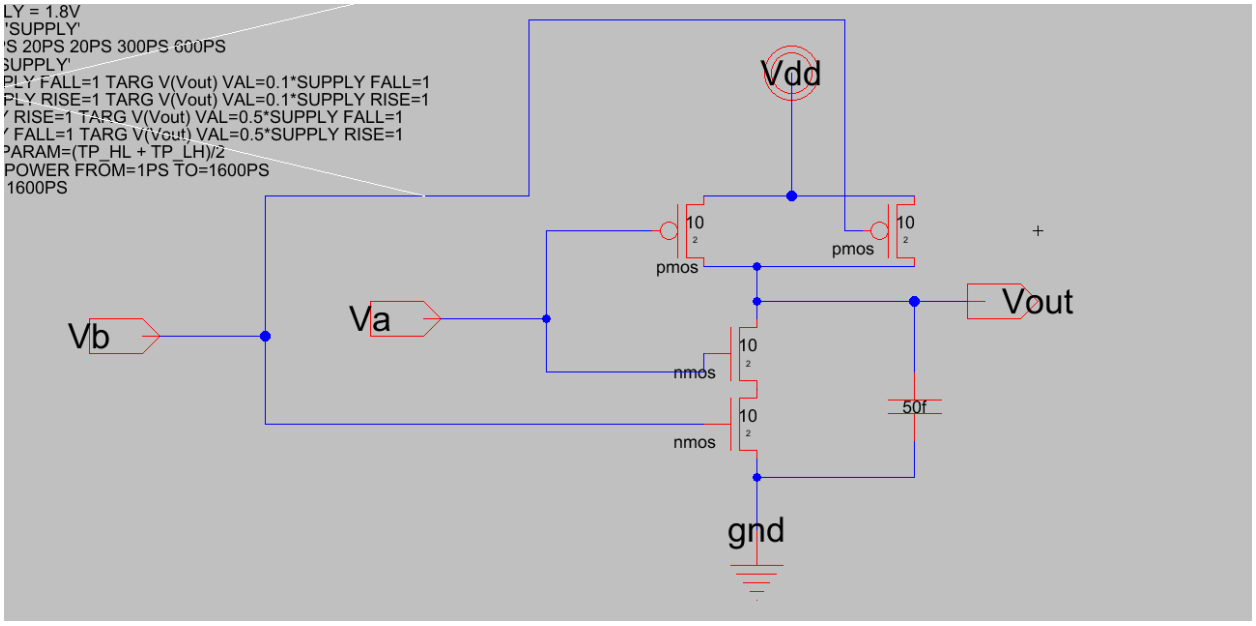


- **Layout:**



2. Second standard cell : 2-input NAND gate

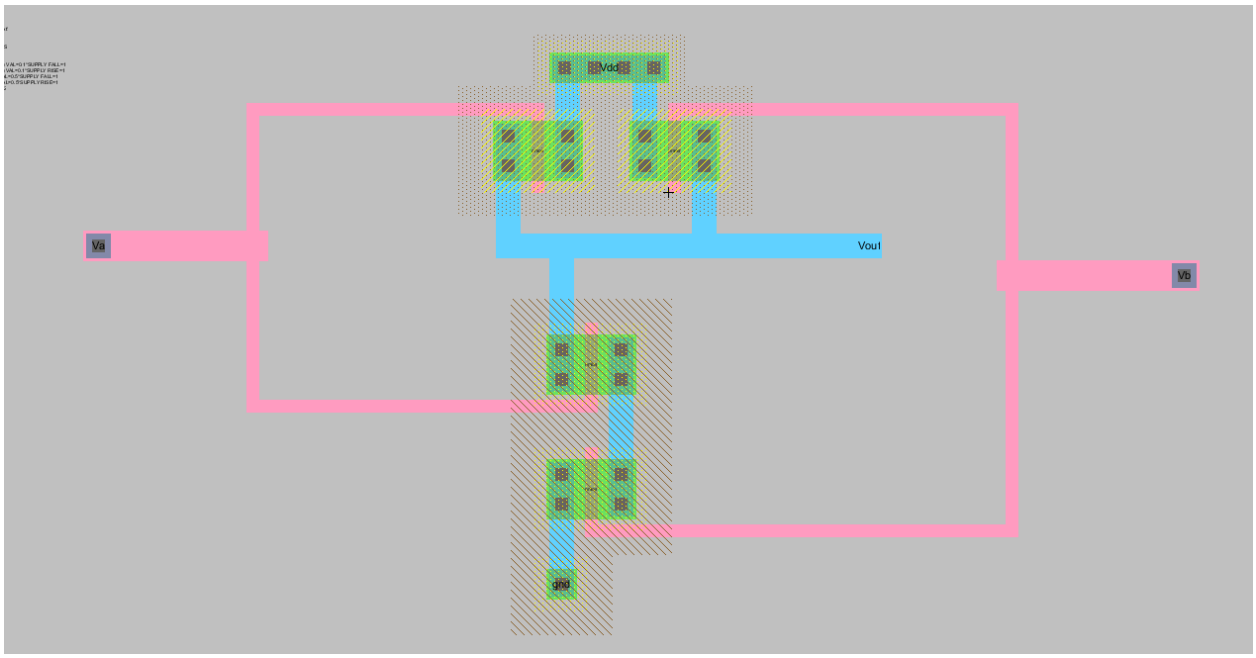
- **Screenshot of the schematic**



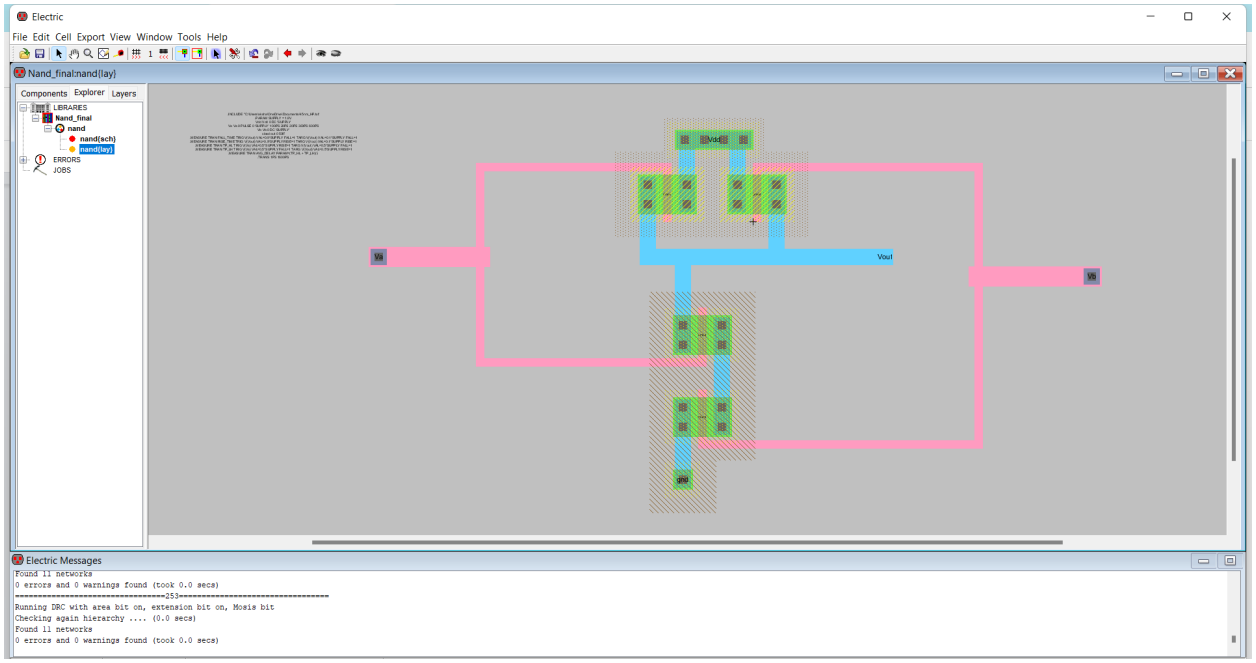
Explanation on how the transistor sizes were chosen

Here, the size of pmos is 10λ & size of nmos is 10λ. Two pmos of 10λ in parallel provide resistance equal to 10λ size pmos. Two nmos of size 10λ will provide worst-case resistance equal to that of 5λ size. If we look at final equivalent sizes, they came up to a ratio of 2:1 (PUN:PDN)

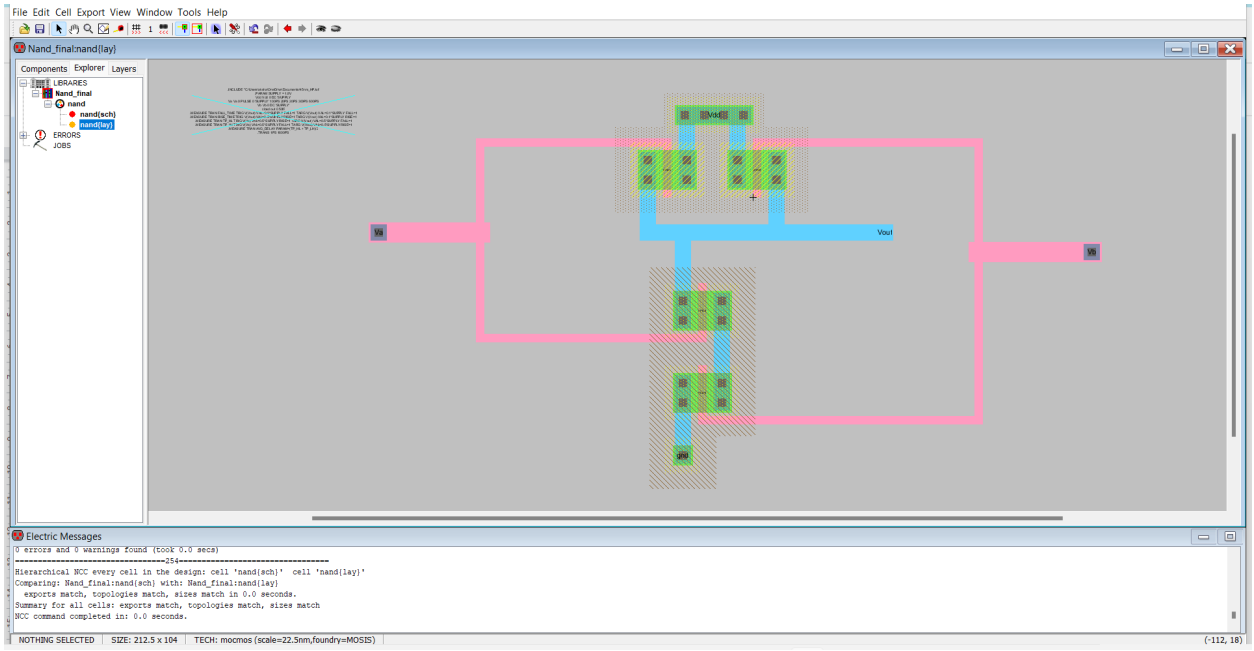
- Screenshot of Layout



- Screenshot of layout with DRC log:



- Screenshot of Layout with LVS log:



Size of Circuit = 212.5 x 104 nm

- Table with the propagation delay values from the schematic and the layout for 5 fF and 50 fF fanout loads :

Capacitor	Propagation delay(Schematic)	Propagation delay(Layout)
5fF	1.32167e-011 s	1.51904e-011 s
50fF	9.60035e-011 s	9.76027e-011 s

- the power consumption from the schematic and layout-extracted simulations :

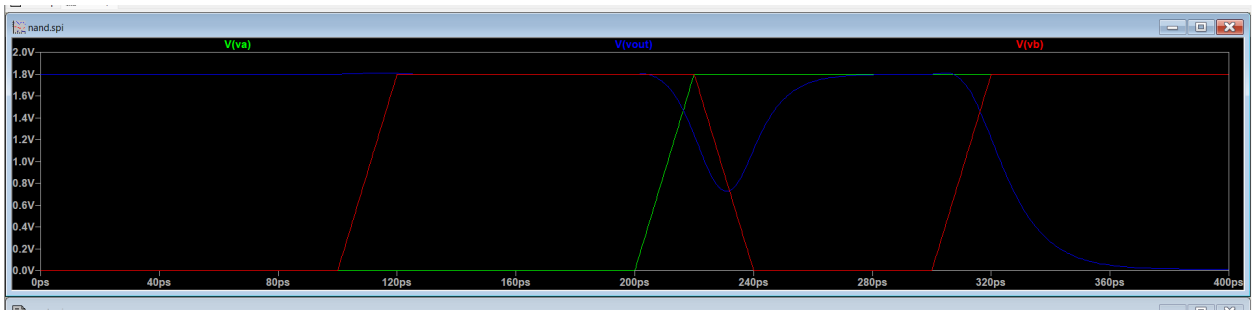
Simulation	Avg Power Consumption
Schematic	10.87234 W
Layout - extracted	10.87209 W

- **Waveform Analysis:**

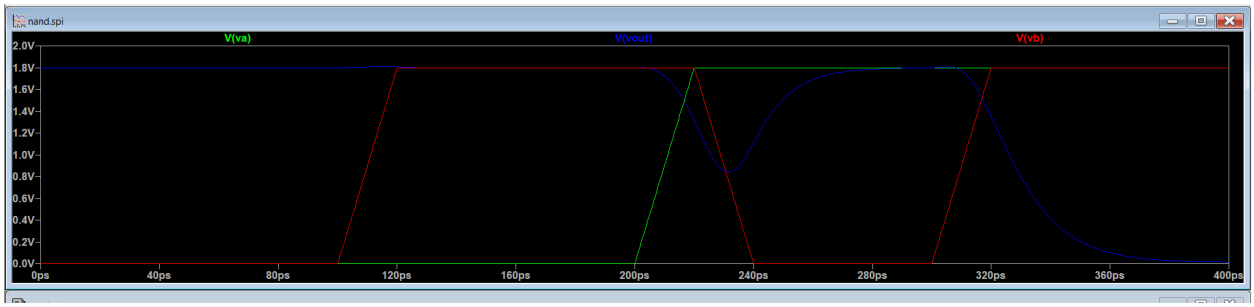
A(Va)	B(Vb)	Y(Vout)
0	0	1
0	1	1
1	0	1
1	1	0

C=5fF

Schematic:

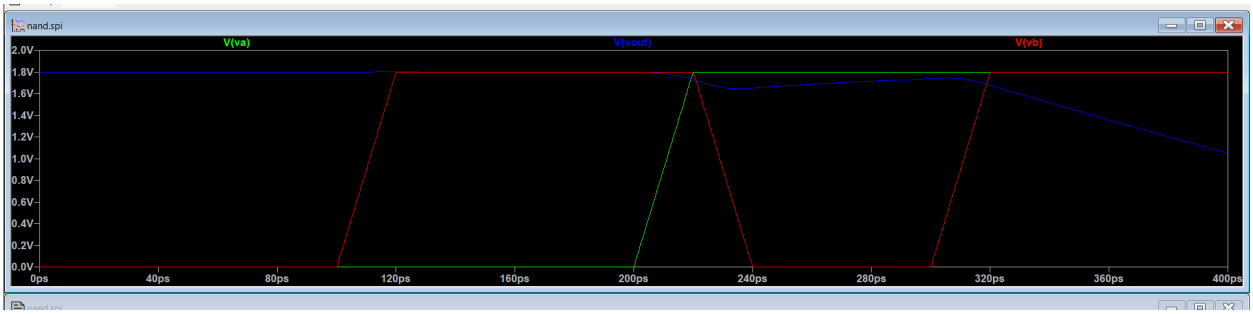


Layout:

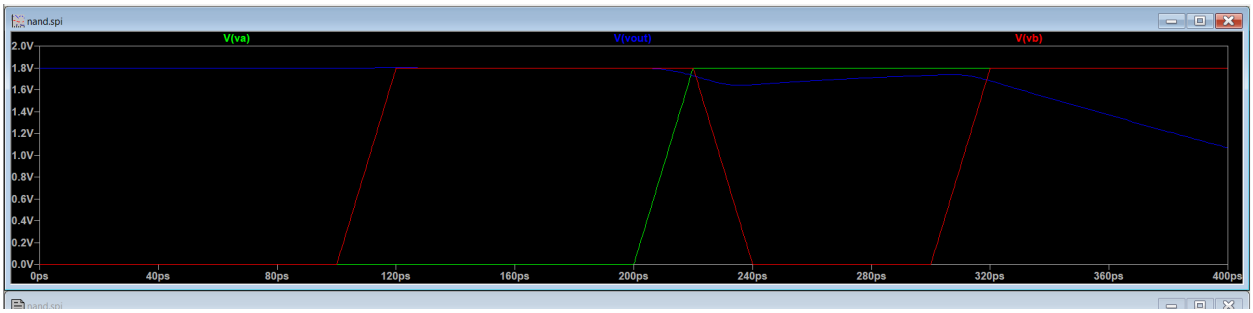


C=50fF

Schematic:

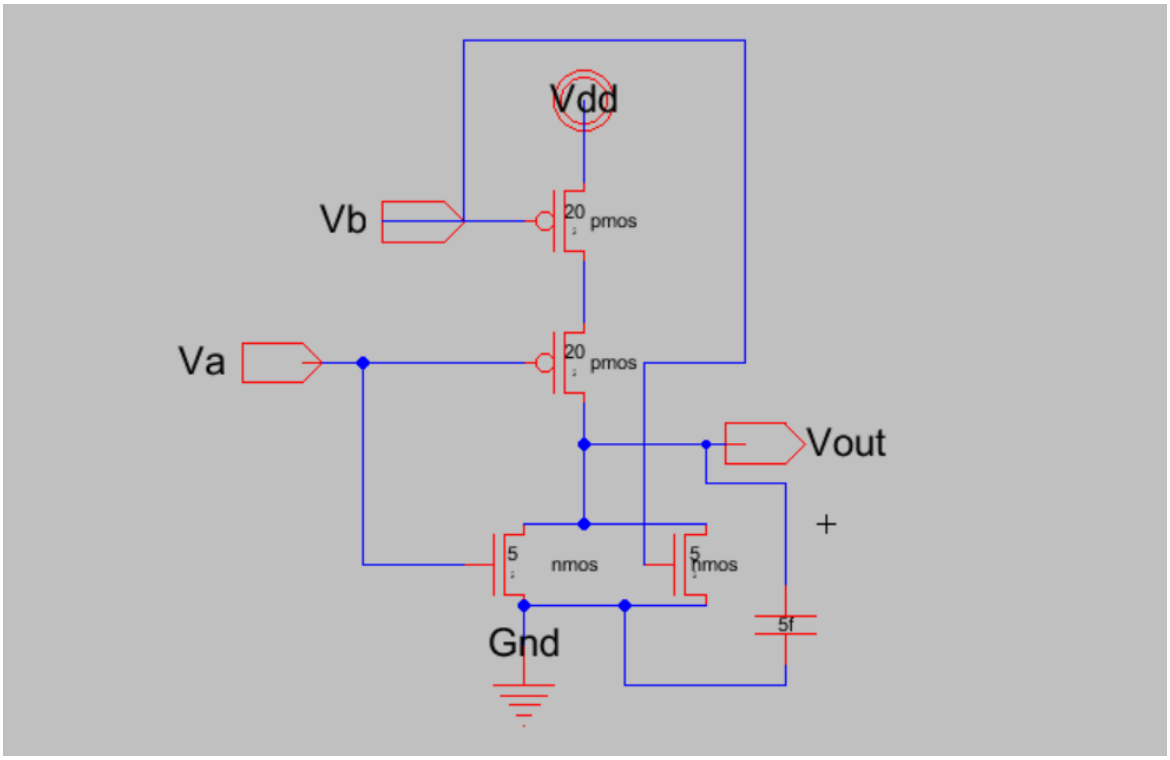


Layout:



3.Third standard cell : 2-input NOR gate

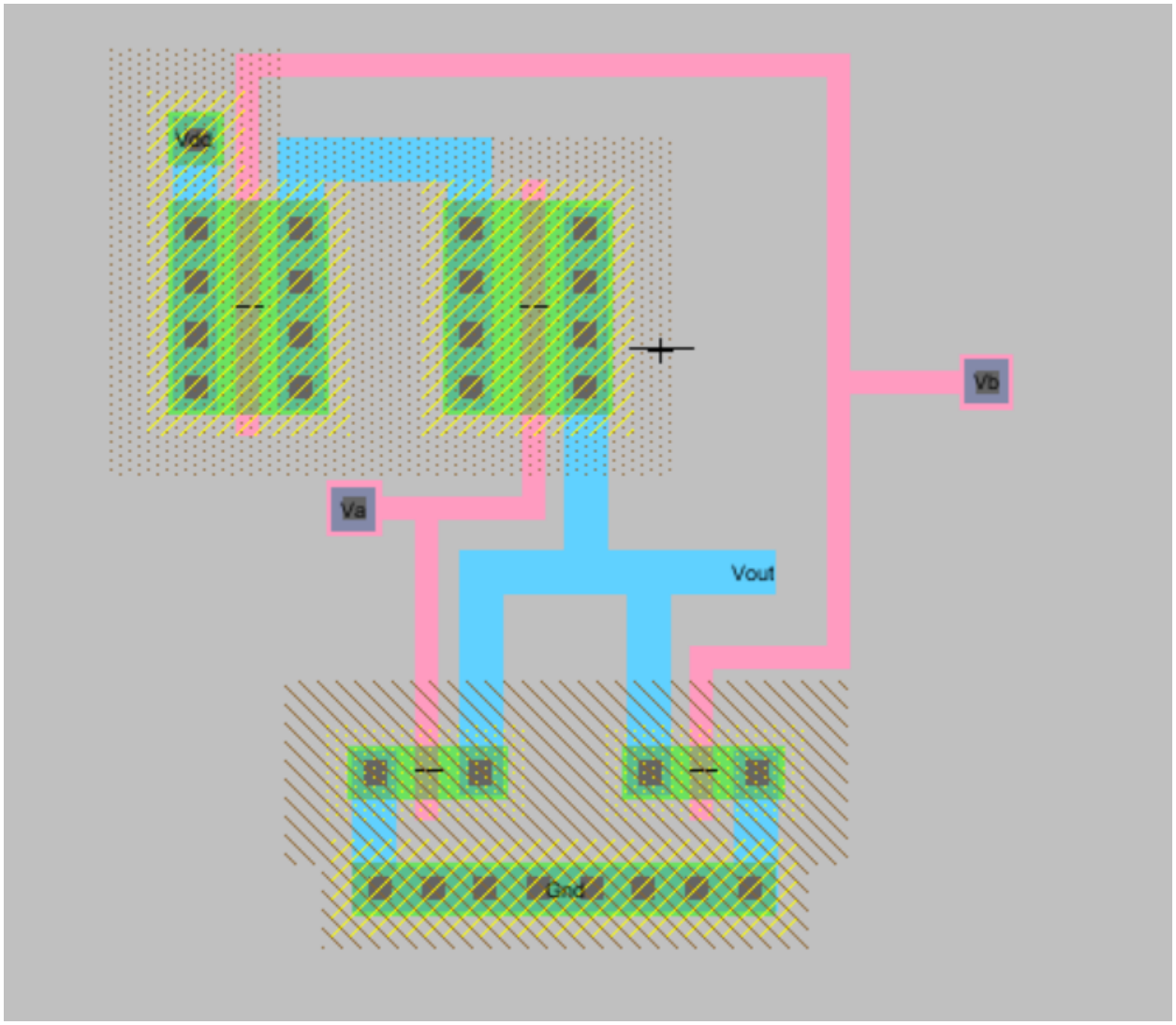
- Screenshot of the schematic

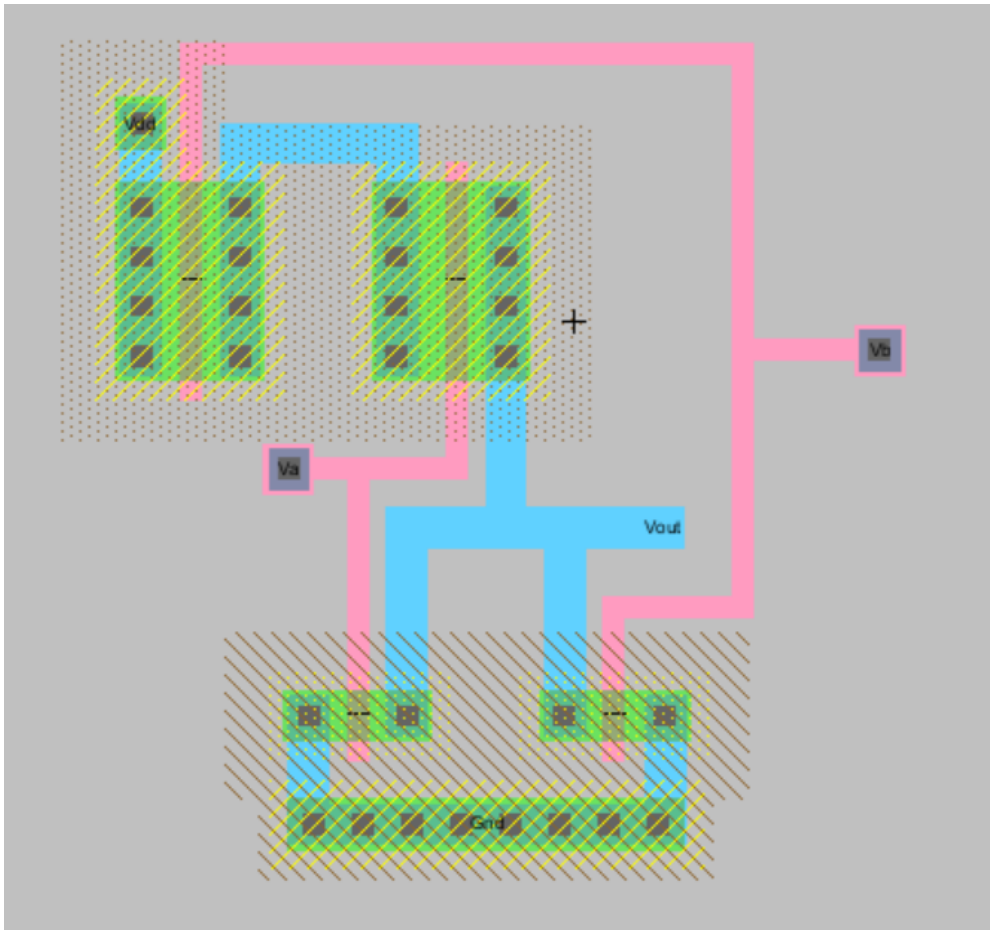


- **Explanation on how the transistor sizes were chosen**

Here, the size of pmos is 20λ & size of nmos is 5λ. Two pmos of 20λ in series provide resistance equal to 10λ size pmos. Two nmos of size 5λ will provide worst-case resistance equal to that of 5λ size nmos. I f we look at final equivalent sizes, they came up to a ratio of 2:1 (PUN:PDN)

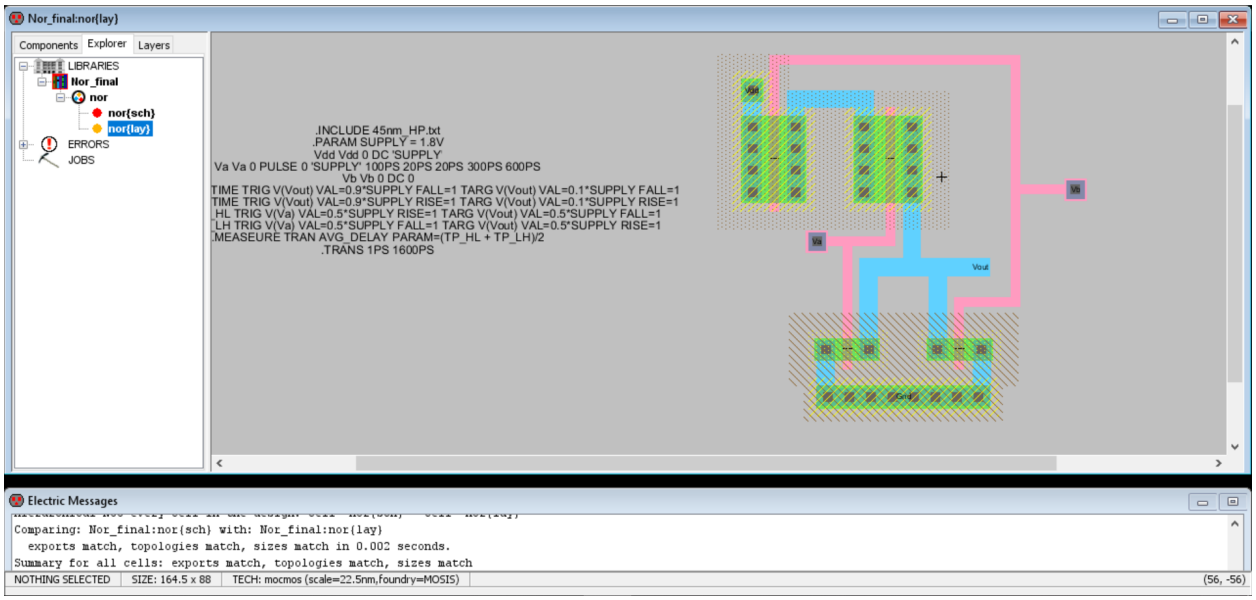
- **Screenshot of Layout**





- **Screenshot of layout with DRC log:**

- **Screenshot of Layout with LVS log:**



Size of Circuit = 164.5 x 88 nm (At the bottom part of the simulation)

- Table with the propagation delay values from the schematic and the layout for 5 fF and 50 fF fanout loads

Capacitor	Propagation delay(Schematic)	Propagation delay(Layout)
5fF	1.47e-11 s	1.66e-11 s
50fF	1.03e-10 s	1.04e-10 s

- the power consumption from the schematic and layout-extracted simulations :

Simulation	Avg Power Consumption
Schematic	10.92508 W
Layout - extracted	10.93279 W

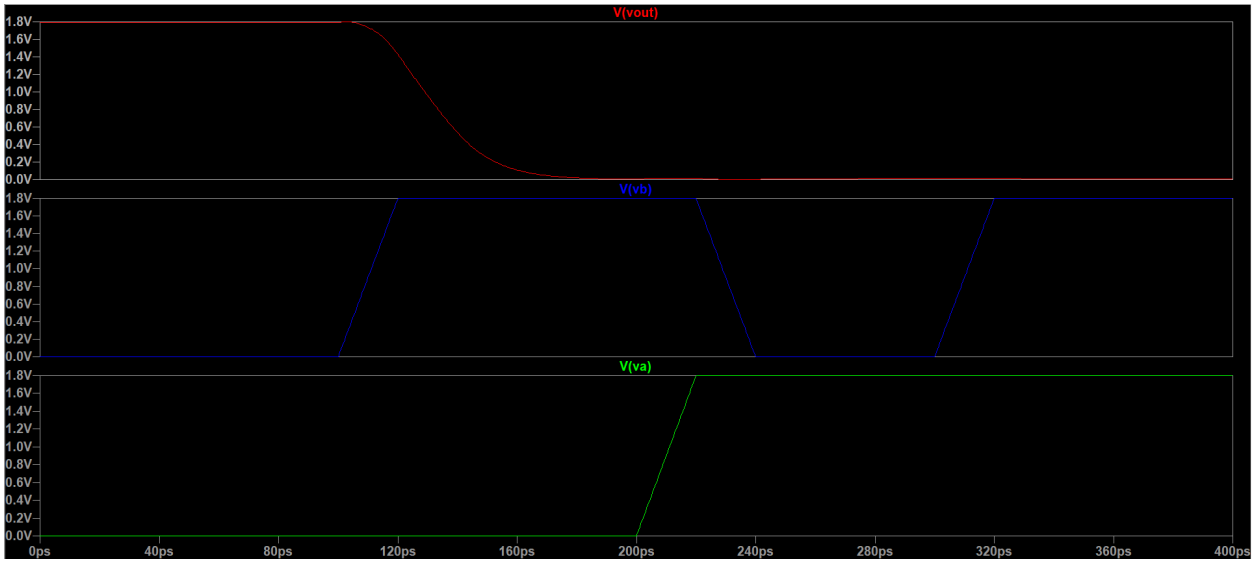
Vdd =1.8 V

Wavefrom Analysis:

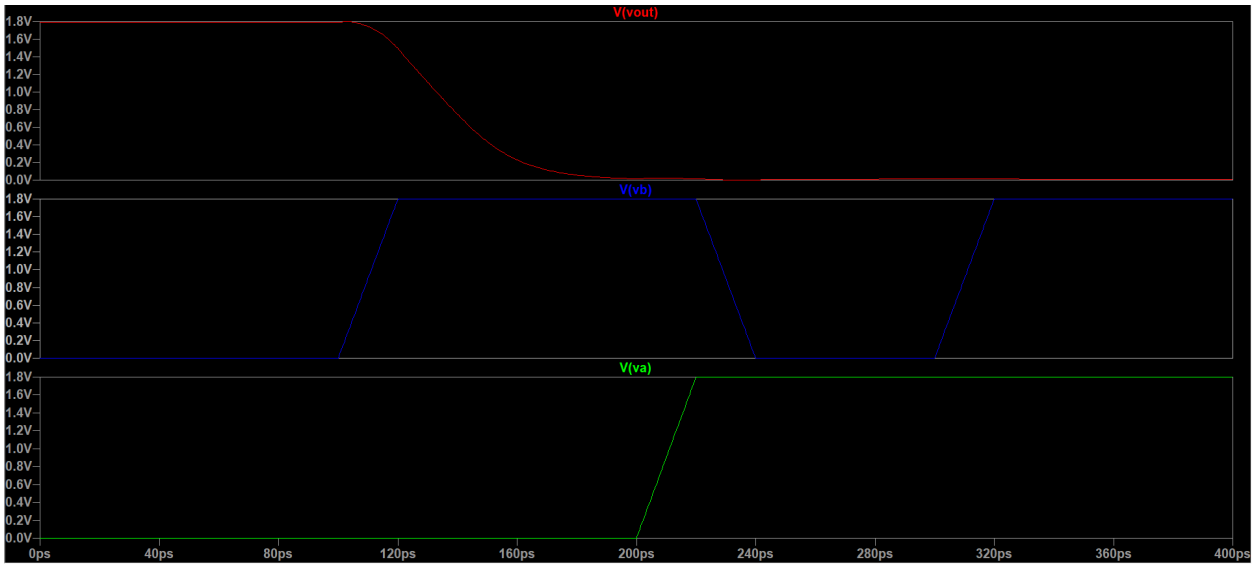
A(Va)	B(Vb)	Y(Vout)
0	0	1
0	1	0
1	0	0
1	1	0

C=5fF:

Schematic

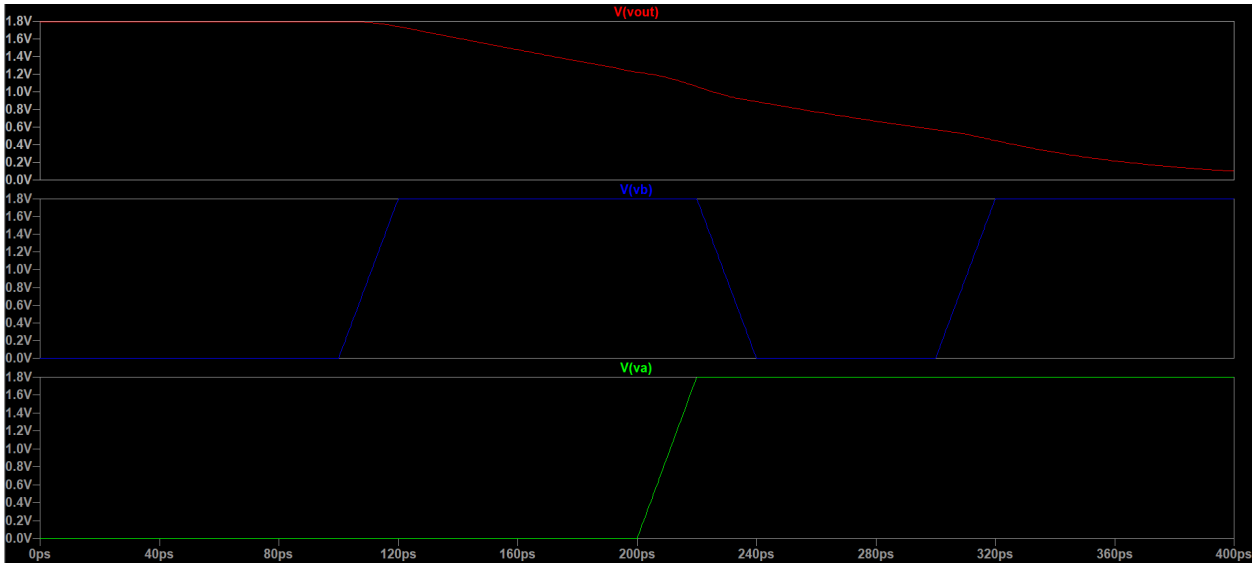


Layout:

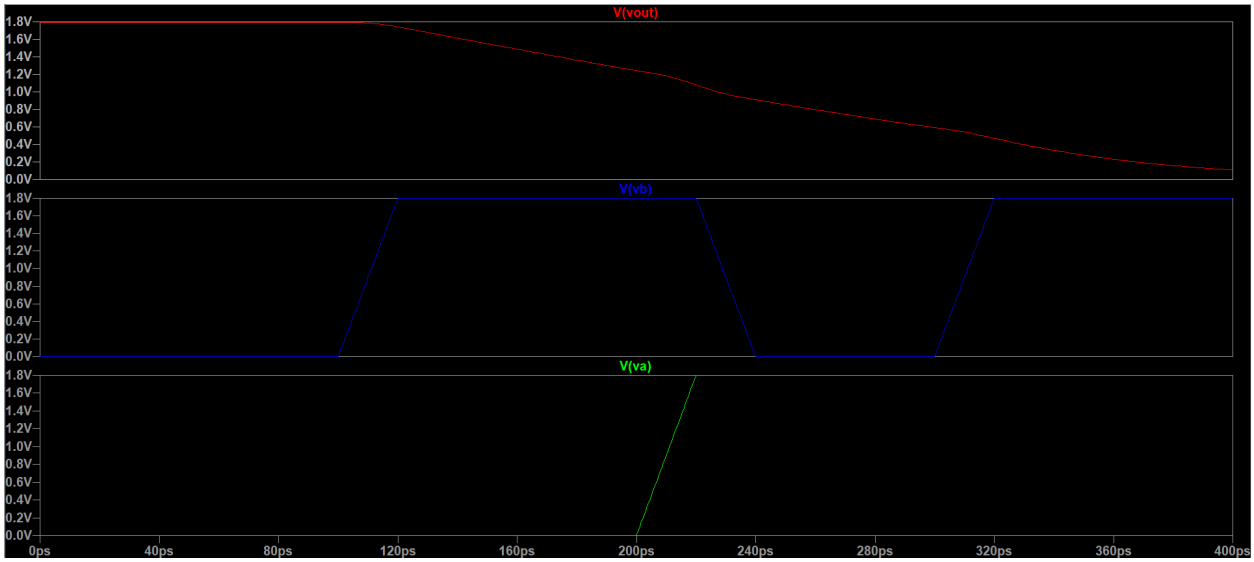


C=50fF

Schematic:



Layout:


V(vout)
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(vb)
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
V(va)
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0ps
40ps
80ps
120ps
160ps
200ps
240ps
280ps
320ps
360ps
400ps