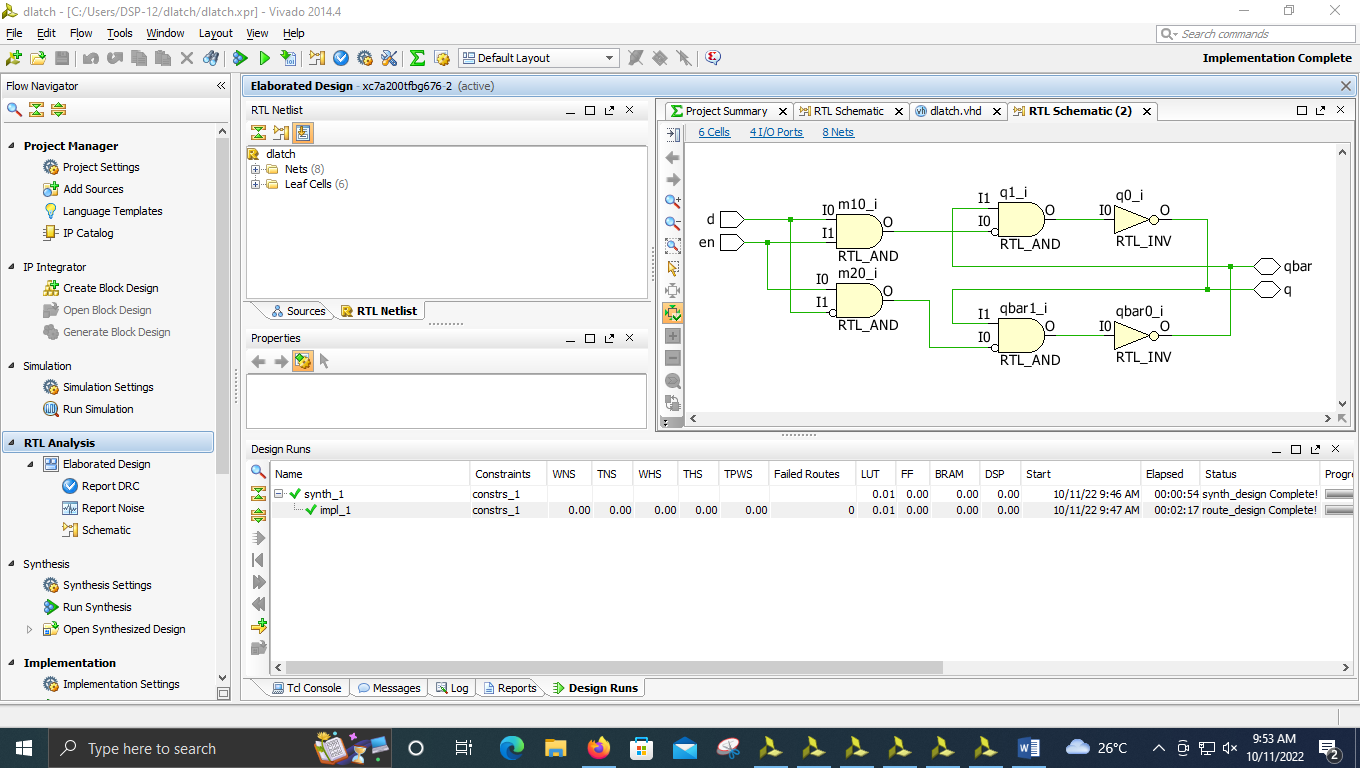
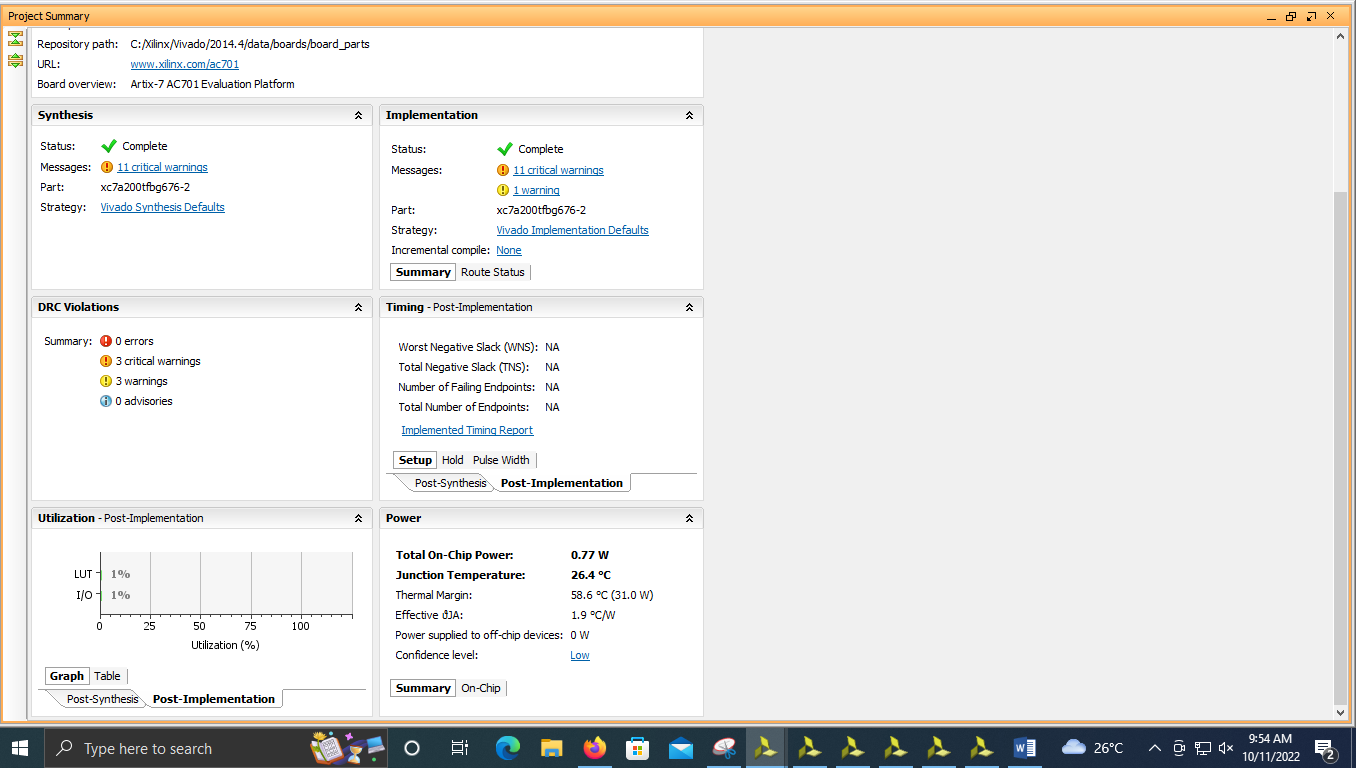
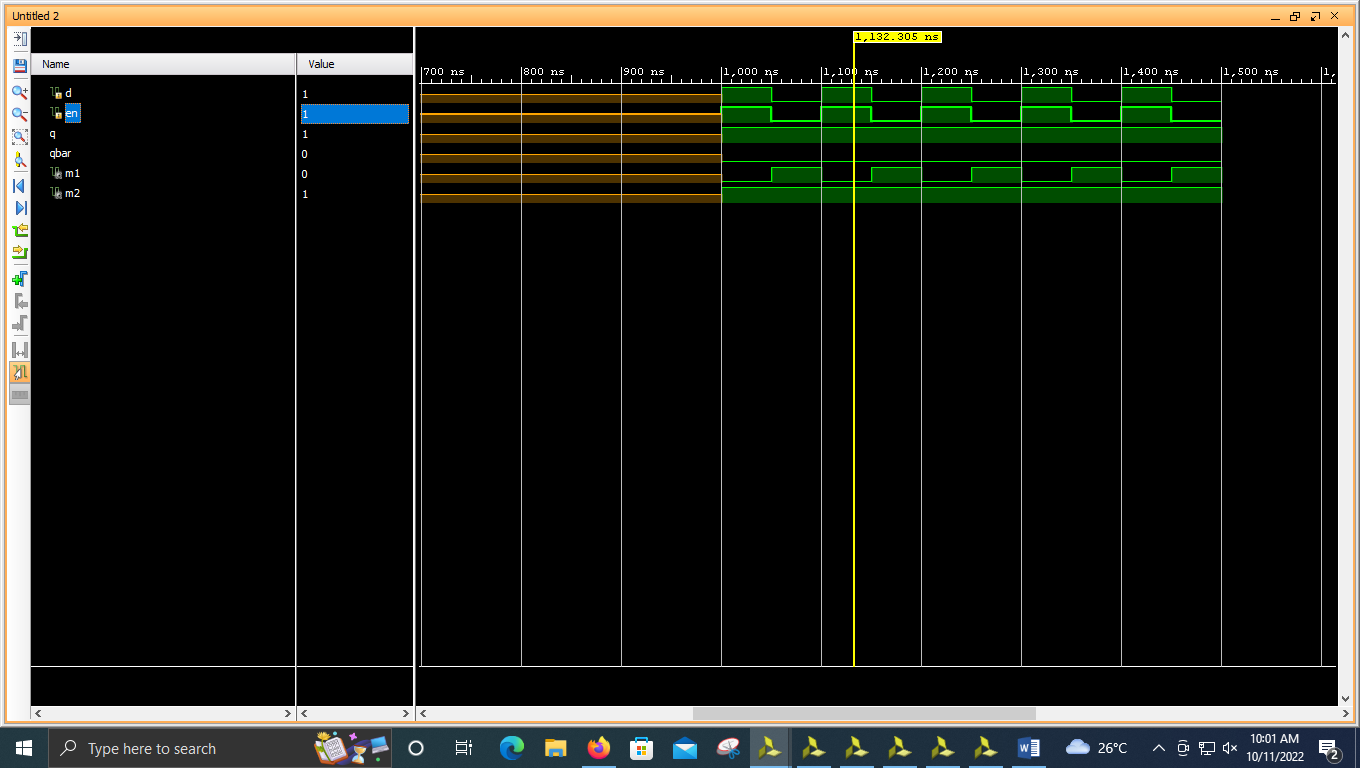
1)







----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 10/11/2022 09:39:50 AM

-- Design Name:

-- Module Name: dlatch - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity dlatch is

Port ( d : in STD\_LOGIC;

en : in STD\_LOGIC;

q : inout STD\_LOGIC;

qbar : inout STD\_LOGIC);

end dlatch;

architecture Behavioral of dlatch is

signal m1,m2:STD\_LOGIC;

begin

m1<= d nand en;

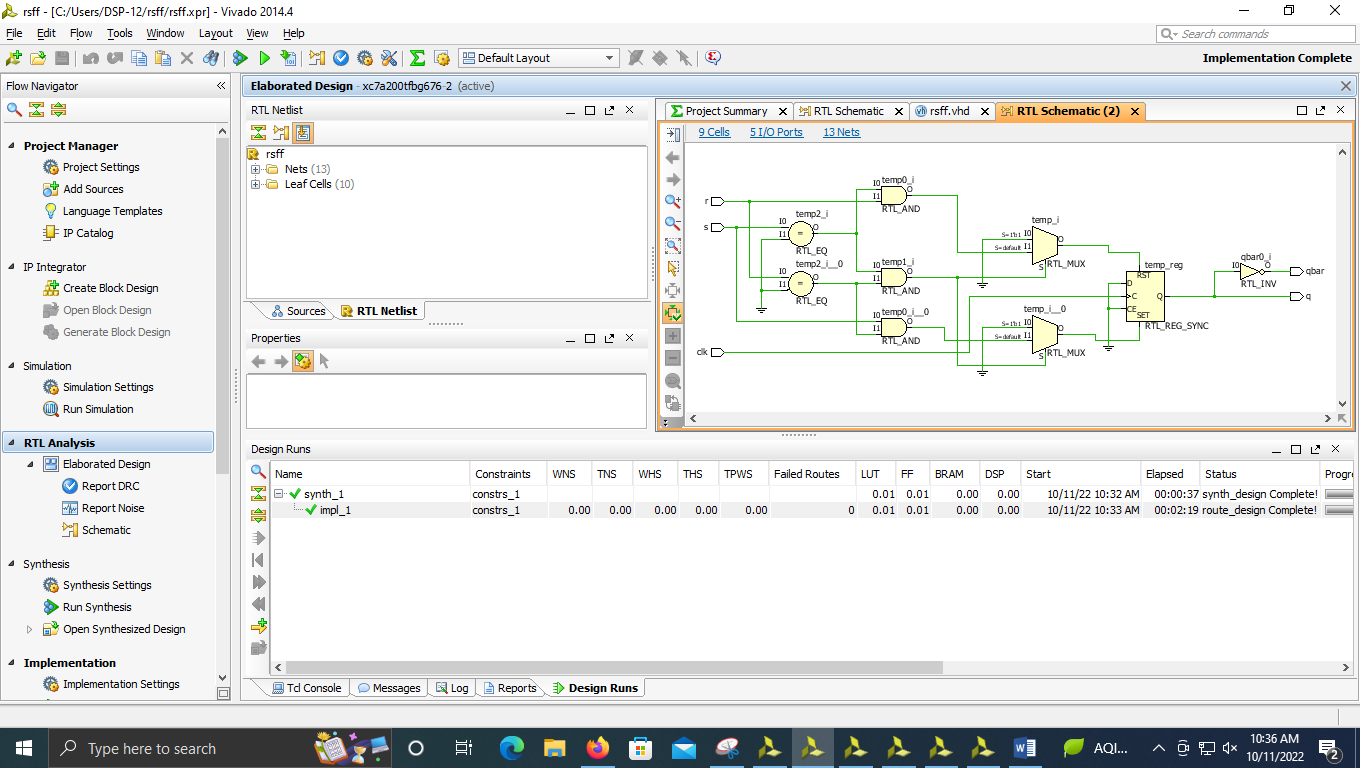
m2 <= en nand (not d);

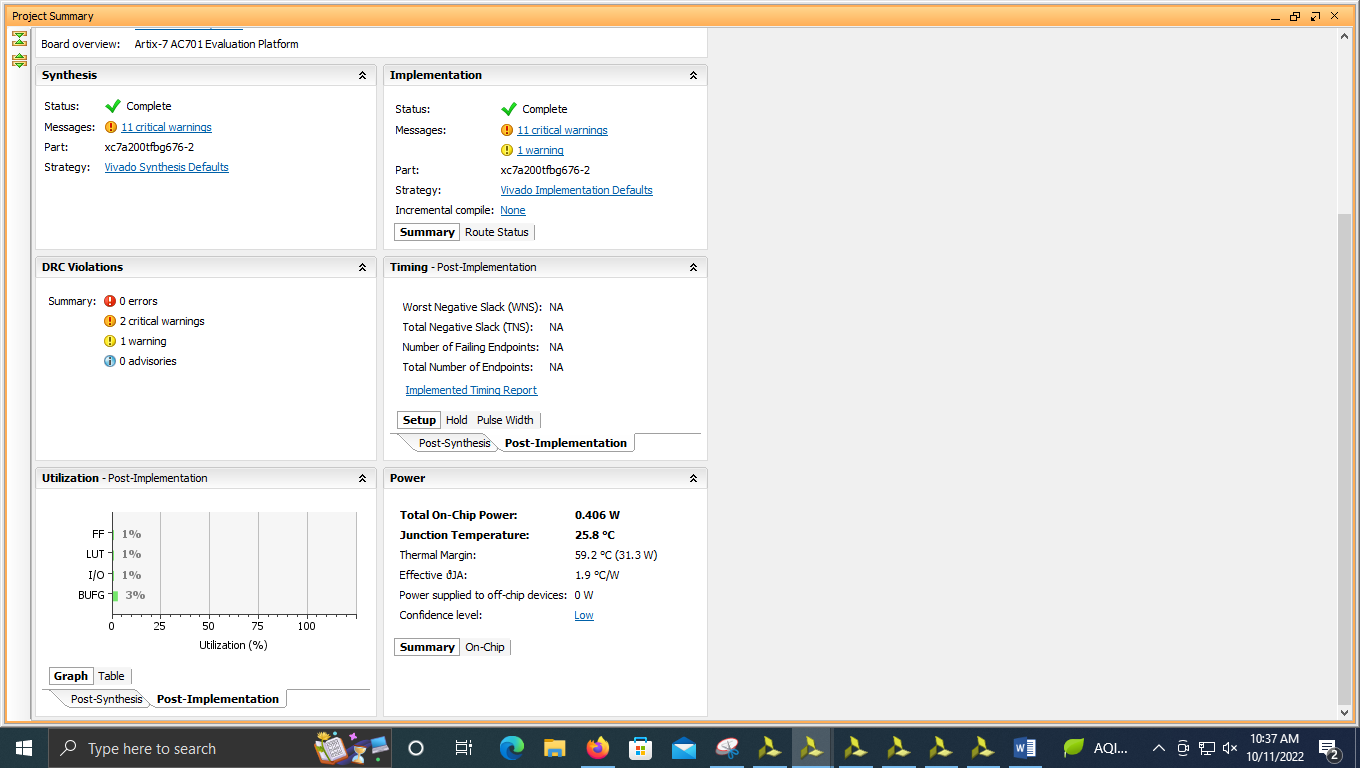
q <= m1 nand qbar;

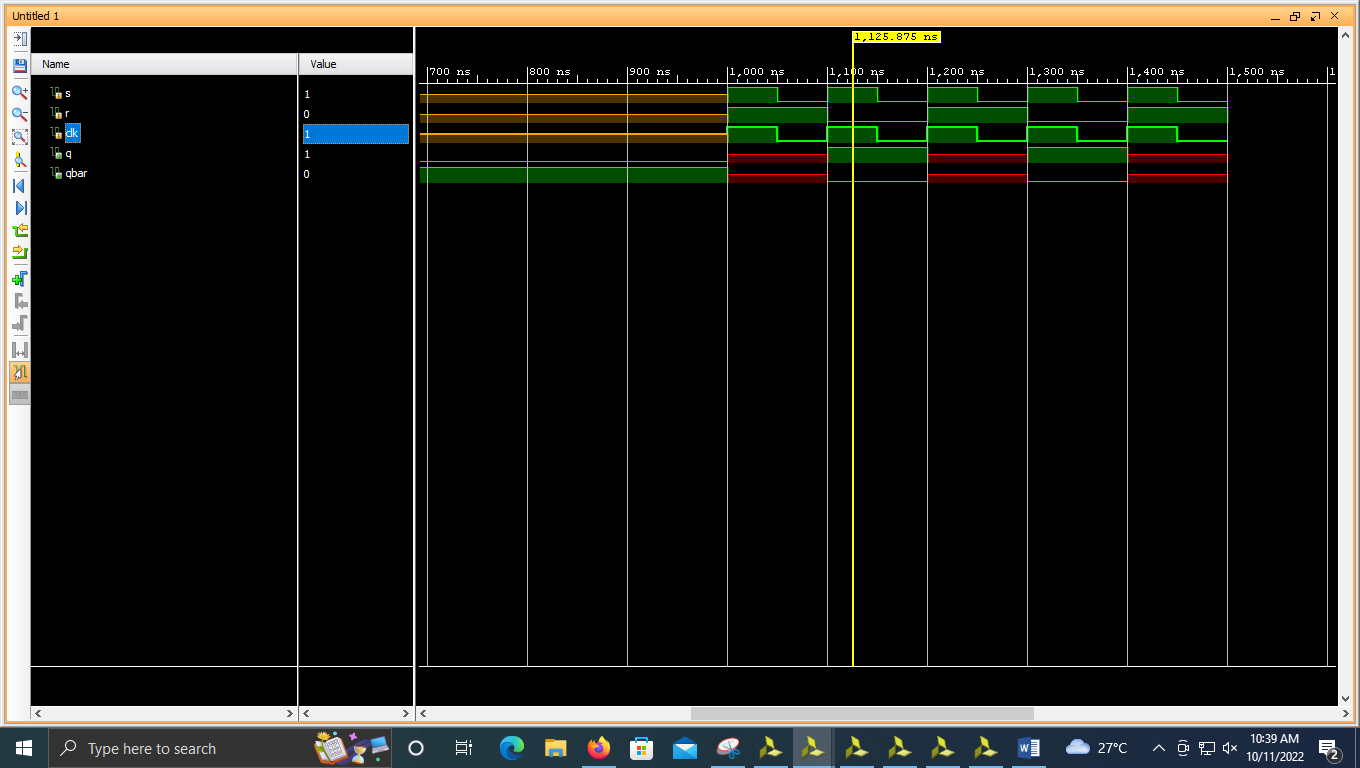
qbar <= m2 nand q;

end Behavioral;

2)







----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 10/11/2022 09:48:53 AM

-- Design Name:

-- Module Name: rsff - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity rsff is

Port ( s : in STD\_LOGIC;

r : in STD\_LOGIC;

clk : in STD\_LOGIC;

q : out STD\_LOGIC;

qbar : out STD\_LOGIC);

end rsff;

architecture Behavioral of rsff is

begin

process(s,r,clk)

variable temp:STD\_LOGIC:='0';

begin

if(clk'event and clk='1') then

if(s='0' and r='0') then

temp :=temp;

elsif(s='0' and r='1') then

temp :='0';

elsif(s='1' and r='0') then

temp :='1';

elsif(s='1' and r='1') then

temp :='X';

end if;

end if;

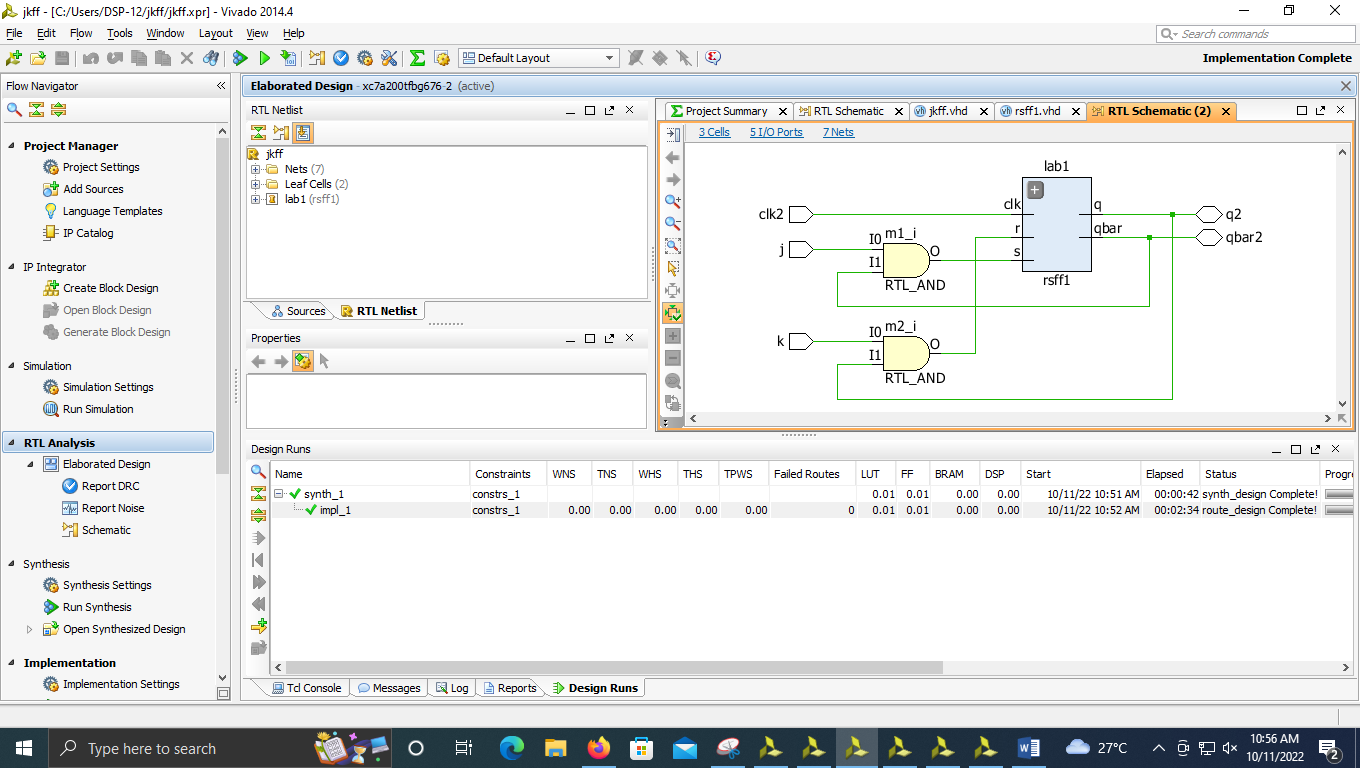
q<=temp;

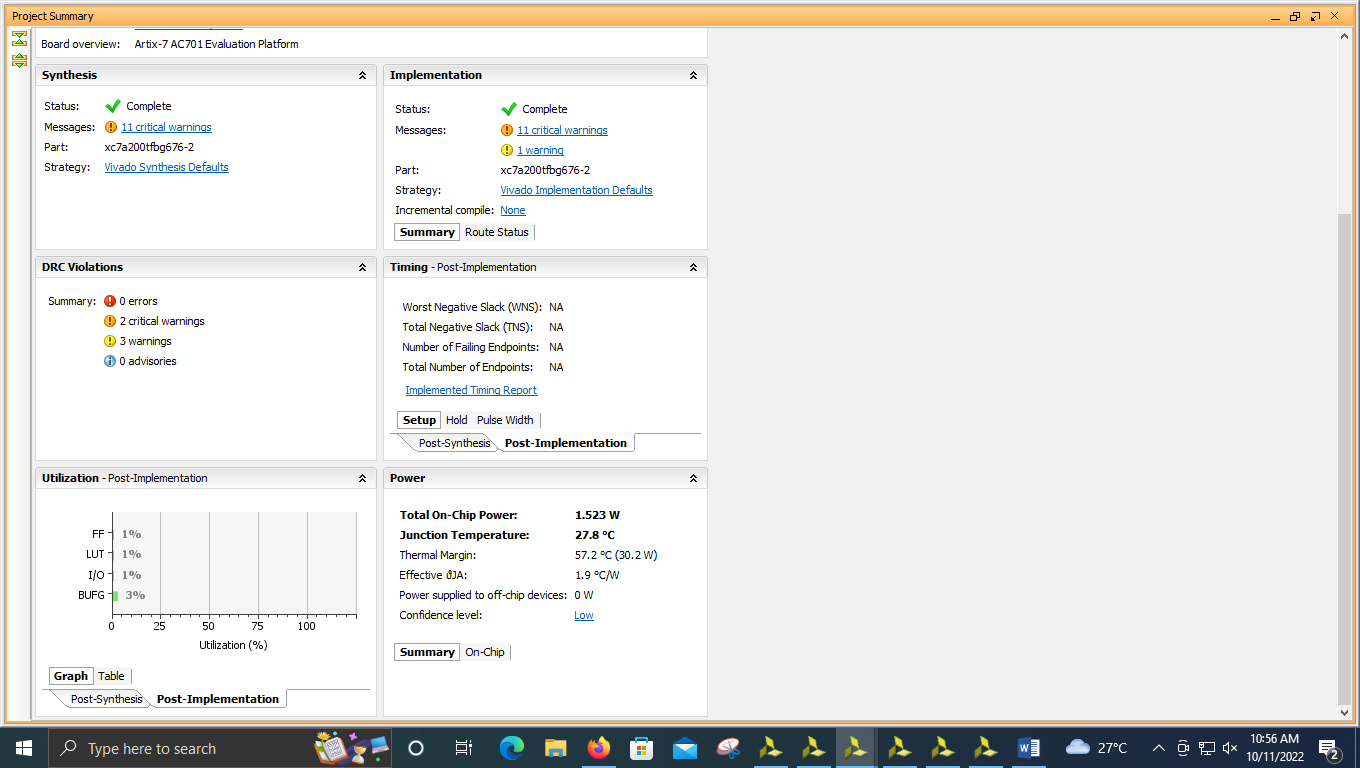
qbar<= not temp;

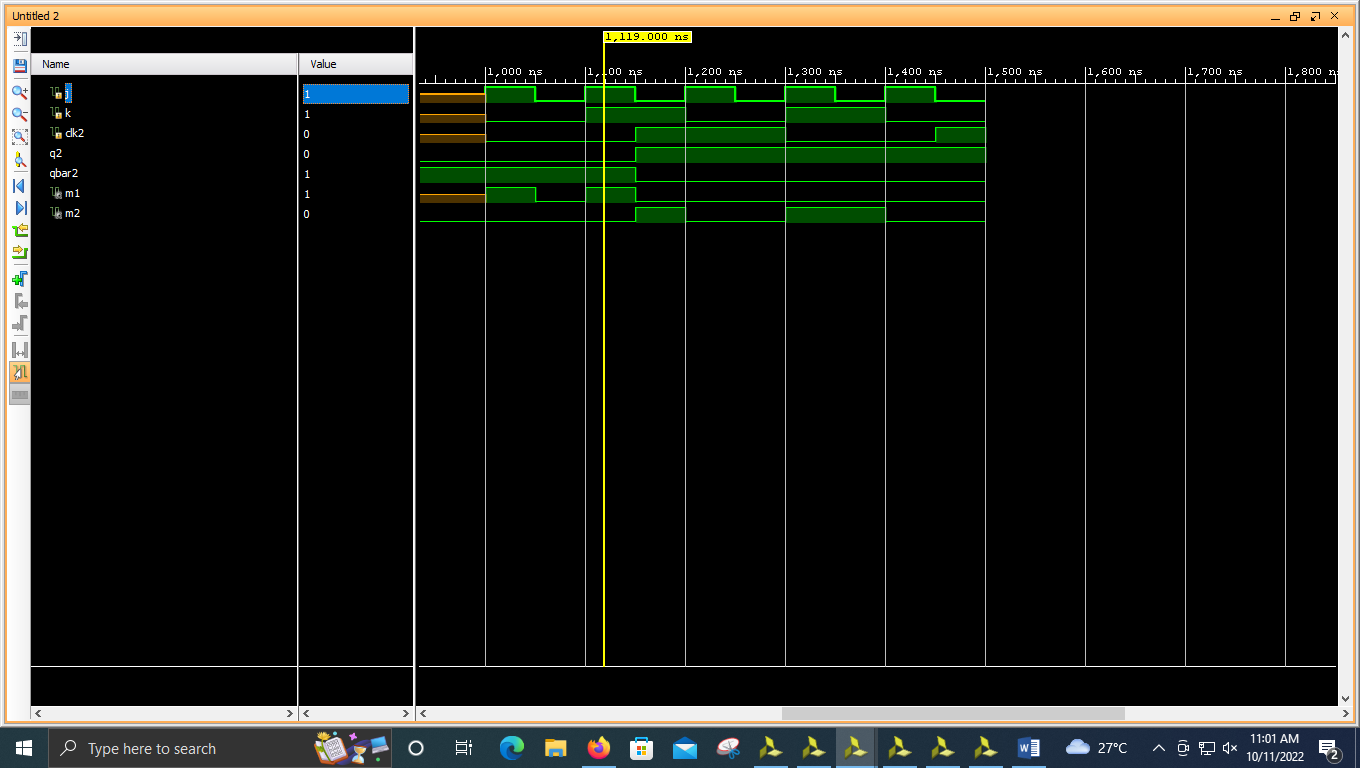
end process;

end Behavioral;

3)







----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 10/11/2022 10:41:00 AM

-- Design Name:

-- Module Name: rsff1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity rsff1 is

Port ( s : in STD\_LOGIC;

r : in STD\_LOGIC;

clk : in STD\_LOGIC;

q : out STD\_LOGIC;

qbar : out STD\_LOGIC);

end rsff1;

architecture Behavioral of rsff1 is

begin

process(s,r,clk)

variable temp:STD\_LOGIC:='0';

begin

if(clk'event and clk='1') then

if(s='0' and r='0') then

temp :=temp;

elsif(s='0' and r='1') then

temp :='0';

elsif(s='1' and r='0') then

temp :='1';

elsif(s='1' and r='1') then

temp :='X';

end if;

end if;

q<=temp;

qbar<= not temp;

end process;

end Behavioral;

----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 10/11/2022 10:35:03 AM

-- Design Name:

-- Module Name: jkff - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity jkff is

Port ( j : in STD\_LOGIC;

k : in STD\_LOGIC;

clk2 : in STD\_LOGIC;

q2 : inout STD\_LOGIC;

qbar2 : inout STD\_LOGIC);

end jkff;

architecture Behavioral of jkff is

component rsff1 is

Port ( s : in STD\_LOGIC;

r : in STD\_LOGIC;

clk : in STD\_LOGIC;

q : out STD\_LOGIC;

qbar : out STD\_LOGIC);

end component;

signal m1,m2:STD\_LOGIC;

begin

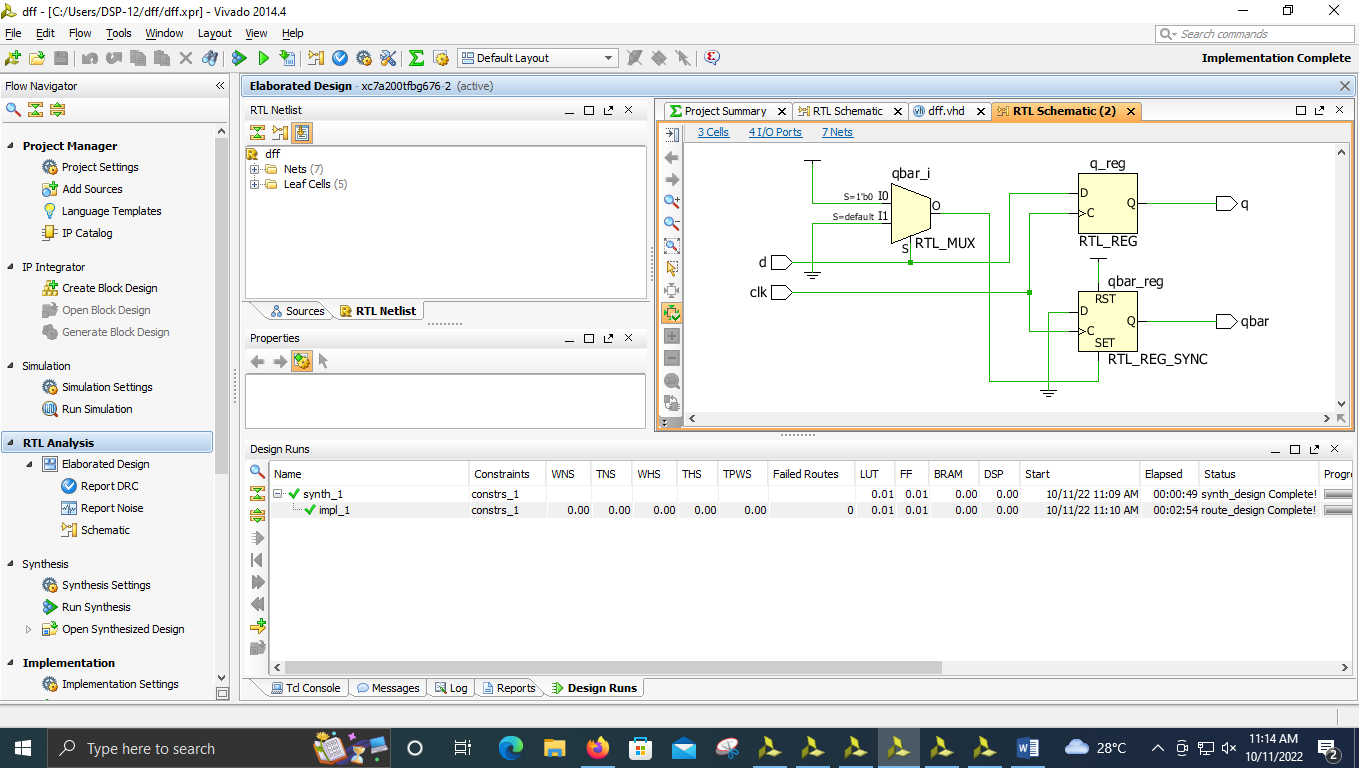
m1<= j and qbar2;

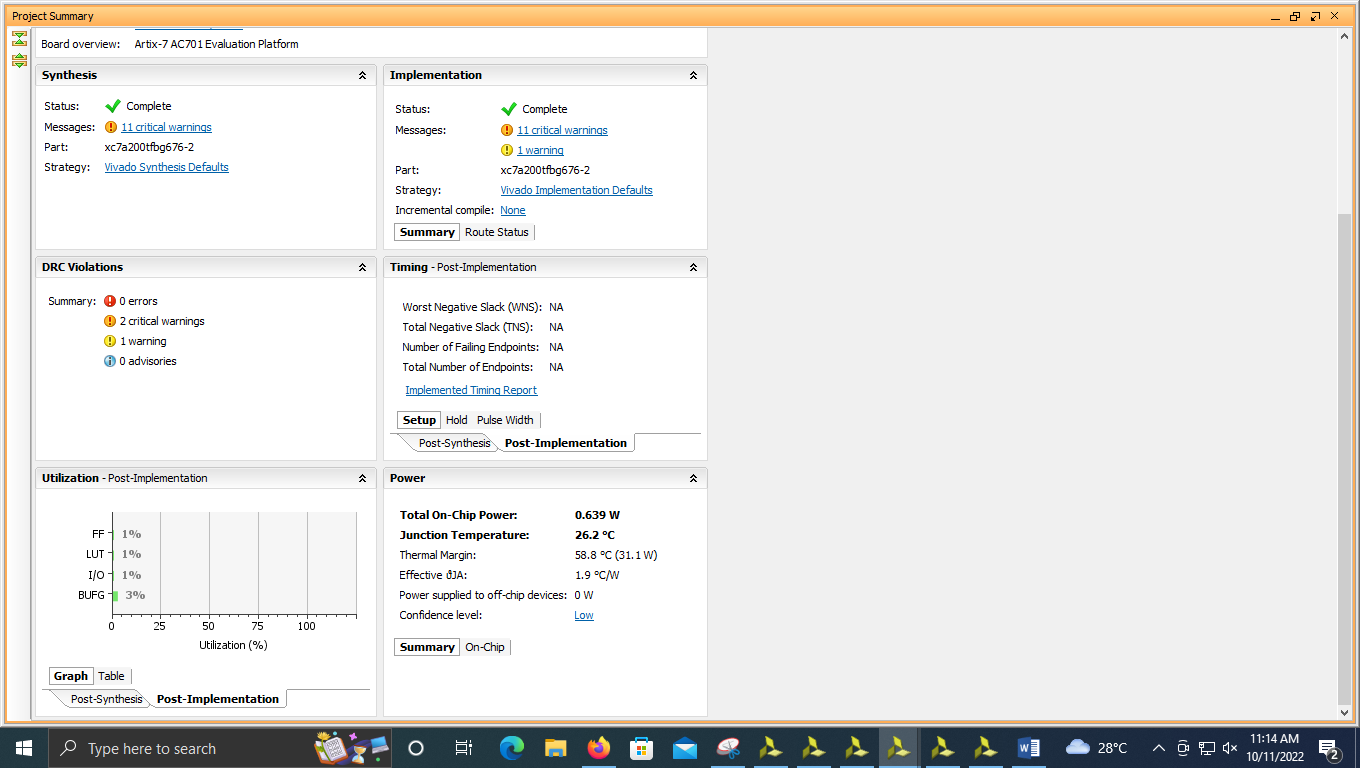
m2<= k and q2;

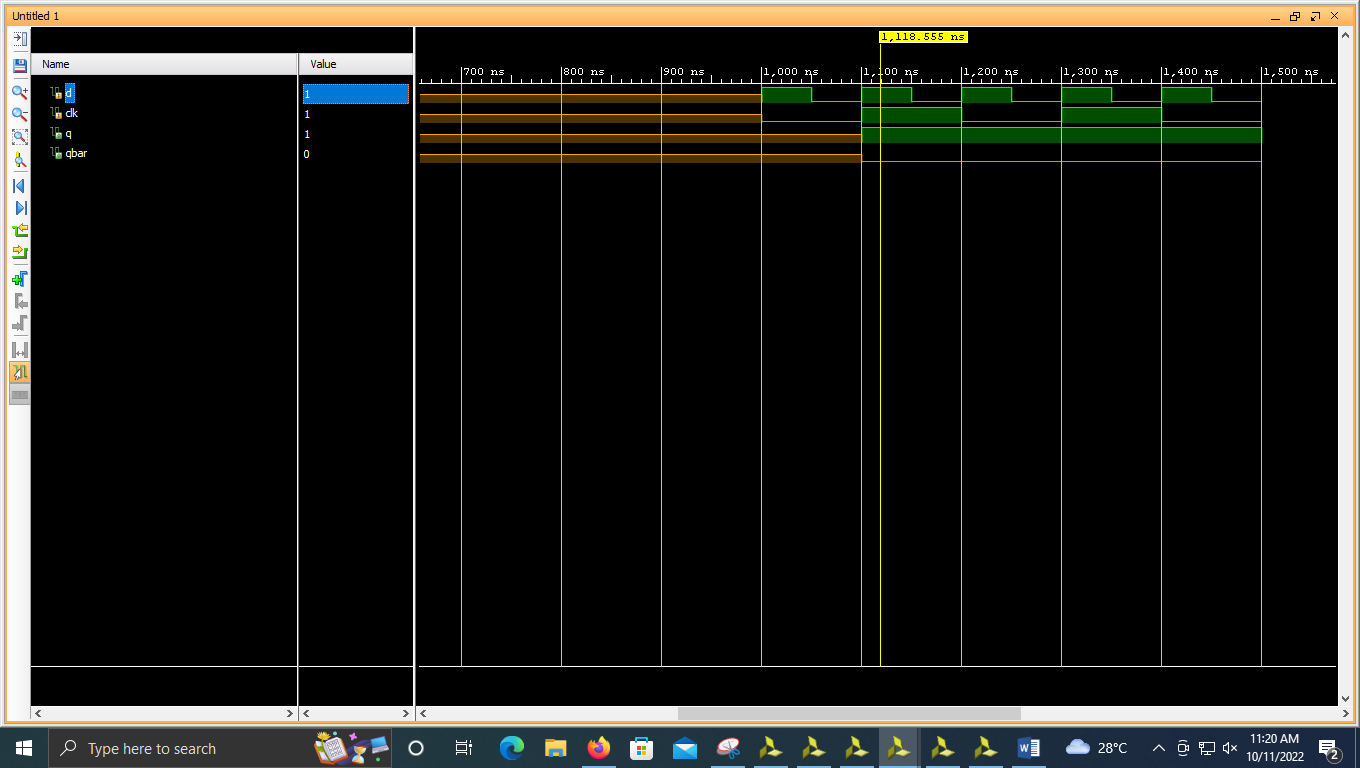
lab1 :rsff1 port map(m1,m2,clk2,q2,qbar2);

end Behavioral;

4)







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-- Company:

-- Engineer:

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-- Create Date: 10/11/2022 11:03:03 AM

-- Design Name:

-- Module Name: dff - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity dff is

Port ( d : in STD\_LOGIC;

clk : in STD\_LOGIC;

q : out STD\_LOGIC;

qbar : out STD\_LOGIC);

end dff;

architecture Behavioral of dff is

begin

process(d,clk)

begin

if(clk'event and clk='1') then

if(d='0')

then

q <= '0';

qbar <= '1';

elsif (d='1')

then

q <= '1';

qbar <= '0';

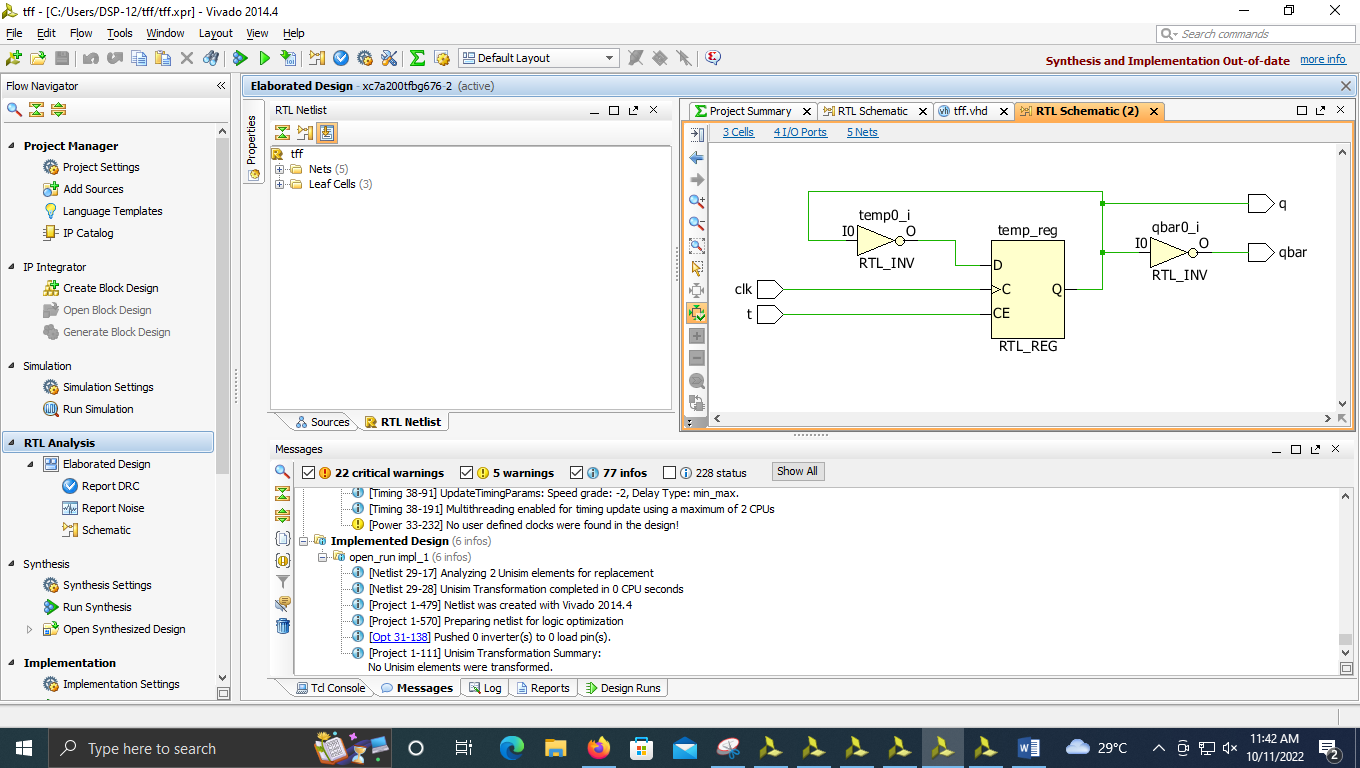
end if;

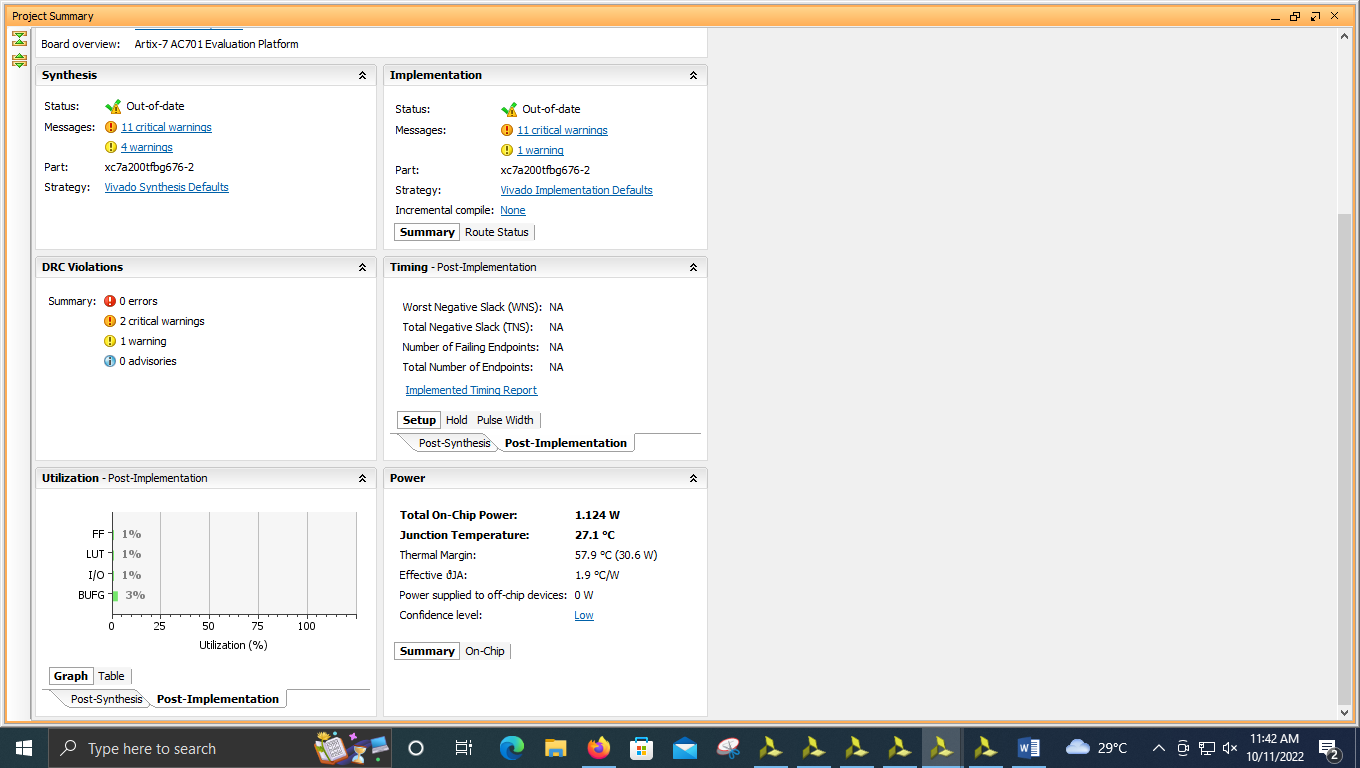
end if;

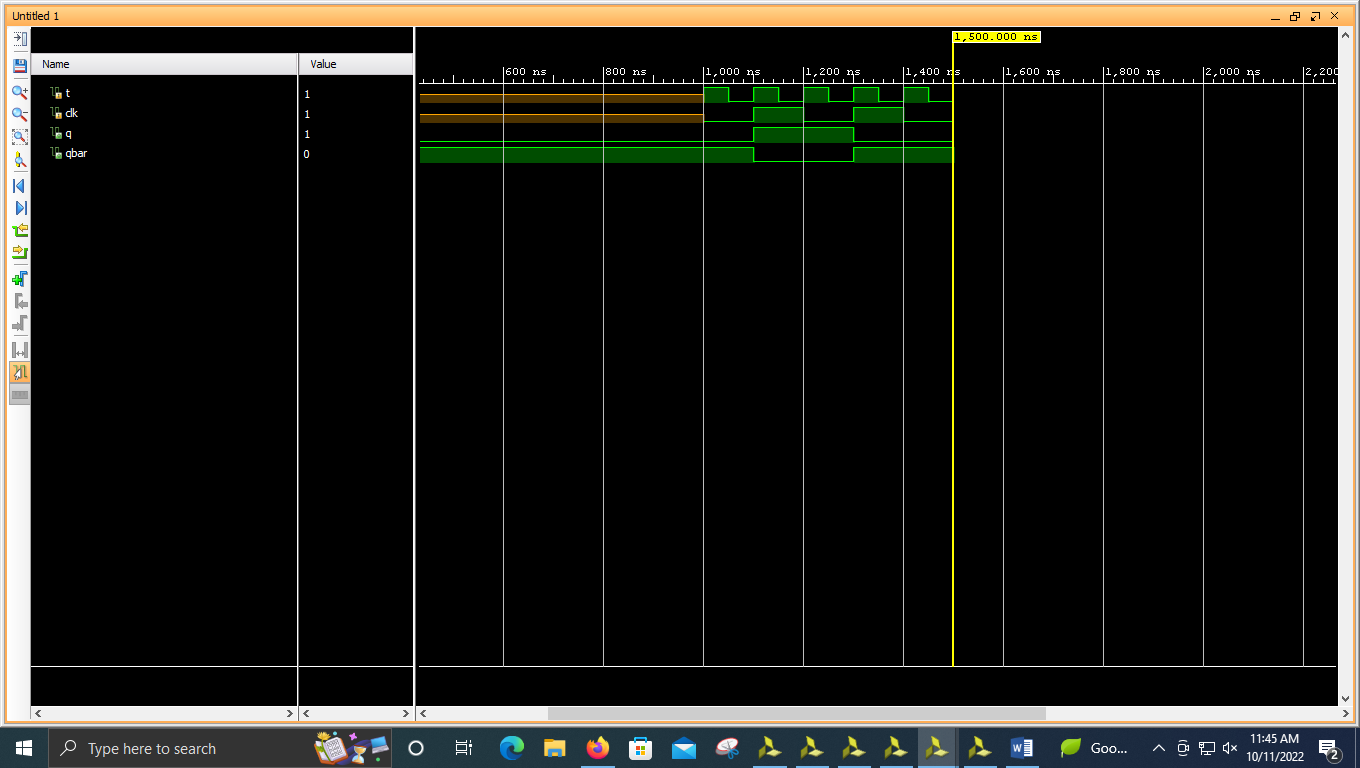
end process;

end Behavioral;

5)







----------------------------------------------------------------------------------

-- Company:

-- Engineer:

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-- Create Date: 10/11/2022 11:10:54 AM

-- Design Name:

-- Module Name: tff - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

--

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity tff is

Port ( t : in STD\_LOGIC;

clk : in STD\_LOGIC;

q : out STD\_LOGIC;

qbar : out STD\_LOGIC);

end tff;

architecture Behavioral of tff is

begin

process(t,clk)

variable temp:STD\_LOGIC := '0';

begin

if(clk'event and clk='1') then

if(t='0') then

temp :=temp;

elsif(t='1') then

temp :=not temp;

end if;

end if;

q<=temp;

qbar<= not temp;

end process;

end Behavioral;